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Systems

IBM 3704, 3705-I, and 3705-II Communications Controllers Principles of Operation

IBM

Preface

This reference publication contains the hardware operation and programming requirements of the IBM 3704 and the IBM 3705 Communications Controllers. The information applies to the IBM 3704, IBM 3705-I and 3705-II except where specifically noted.

The publication is intended for any user of a communications controller who is attempting to write or modify a 3704/3705 control program. The reader should have an understanding of basic data communication and a thorough knowledge of IBM System/360 and System/370 channel operations. The *Introduction to the IBM 3704 and 3705-II Communications Controllers* (GA27-3051) is a prerequisite publication. Related publications are the *IBM 3705 Communications Controller Assembler Language* manual (GC30-3003), the *Synchronous Data Link Control General Information* manual (GA27-3093), the *Guide to Using the IBM 3704 Communications Controller Control Panel* (GA27-3086), and the *Guide to Using the IBM 3705 Communications Controller Control Panel* (GA27-3087).

Other IBM publications concerning the communications controllers are identified and described in the *IBM System/370 Bibliography*, GC20-0001.

This manual is divided into eleven chapters and three appendixes.

Chapter 1: Introduction
Provides a general description of the 3704, 3705-I, and 3705-II.

Chapter 2: System Structure
Describes the registers, interrupt scheme, and levels of the control program.

Chapter 3: Storage and Line Addressing
Describes the basic storage addressing procedure and the format for addressing the individual communication lines.

Chapter 4: Instruction Set
Describes each of the 3704/3705 machine instructions with their format and condition codes.

Chapters 5 through 10:
Describe the operation and programming requirements of the Central Control Unit, the Types 1, 2, 3, and 3HS Communication Scanners, and the Types 1, 2, 3, and 4 Channel Adapters.

Chapter 11: Remote Communications Controller
Describes the hardware and programming required to support a communications controller at a remote location.

The appendixes contain (A) External register functions, (B) Input/Output instruction bit definitions, and (C) Input/Output instruction summary.

Seventh Edition (October 1979)

This is a major revision of and makes obsolete GC30-3004-5, and TNL GN30-3081. The *Summary of Changes* section describes the changes made in this edition.

Changes are periodically made to the information herein; before using this publication in connection with the operation of IBM systems or equipment consult the latest IBM System/370 Bibliography (GC20-0001) and associated Technical Newsletters, for the editions that are applicable and current.

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Contents

Figures

ABAR	attachment buffer address register
ACR	add character register instruction
ACR	abandon call and retry
ACU	automatic calling unit
AHR	add halfword register instruction
ALU	arithmetic logic unit
AR	add register instruction
ARI	add register immediate instruction
ATT	attention
B	branch instruction
BAL	branch and link instruction
BALR	branch and link register instruction
BB	branch on bit instruction
BCL	branch on C latch instruction
BCT	branch on count instruction
BSC	binary synchronous communication
BZL	branch on Z latch instruction
CA	channel adapter
CACHKR	channel adapter check register
CACR	channel adapter control register
CADB	channel adapter data buffer or channel adapter diagnostic busy
CAMR	channel adapter mode register
CASNSR	channel adapter sense register
CASTR	channel adapter status register
CBODR	channel bus out diagnostic register
CCR	compare character register instruction
CCU	central control unit
CE	channel end
CHR	compare halfword register instruction
CMDR	channel adapter command register
COS	call originate status
CPU	central processing unit
CR	compare register instruction
CRC	cyclic redundancy check
CRI	compare register immediate instruction
CRQ	call request
CSAR	cycle steal address register
CTDR	channel tag diagnostic register
CTRL	control
CUCR	cycle utilization counter register
CW	control word
CWAR	control word address register
CWCNTR	control word byte count register
DBAR	diagnostic buffer address register
DE	device end
DLO	data line occupied
DPR	digit present
DTR	data terminal ready
EB	extended-buffer (mode)
EC	Engineering Change
ESC	emulator subchannel
EXIT	exit instruction
FDX	full duplex
HDX	half duplex
HEX	hexadecimal
HIO	halt I/O
IAR	instruction address register
IC	insert character instruction
ICT	insert character and count instruction
ICW	interface control word
IN	input instruction
INCWAR	in-bound control word address register
I/O	input/output
IPL	initial program load
IPR	interrupt priority register
L	load instruction
LA	load address instruction
LAR	lagging address register
LCD	line control identifier
LCOR	load character with offset register instruction
LCR	load character register instruction
LH	load halfword instruction
LHOR	load halfword with offset register instruction
LHR	load halfword register instruction
LIB	line interface base
LOR	load with offset register instruction
LR	load register instruction
LRI	load register immediate instruction
NCR	AND character register instruction
NHR	AND halfword register instruction
NR	AND register instruction
NRI	AND register immediate instruction
NSC	native subchannel
OCR	OR character register instruction
OHR	OR halfword register instruction
OR	OR register instruction
ORI	OR register immediate instruction
OUT	output instruction
OUTCWAR	out-bound control word address register
PCF	primary control field
PCI	program controlled interrupt
PDF	parallel data field
PND	present next digit
RA	register and immediate address operation
RE	register and external register operation
RI	register and immediate operand operation
ROS	read-only-storage
RR	register to register operation
RS	register and storage operation
RSA	register and storage with count operation
RT	branch operation
RTS	request to send
SAR	storage address register
SCF	secondary control field
SCR	subtract character register instruction
SDF	serial data field
SDLC	synchronous data link control

SDR	storage data register
SHR	subtract halfword register instruction
SIO	start I/O
SM	status modifier
SR	subtract register instruction
SRI	subtract register immediate instruction
ST	store instruction
STC	store character instruction
STCT	store character and count instruction
STH	store halfword instruction
SVC	supervisor call
TAR	temporary address register
TIC	transfer in channel
TIO	test I/O
TRM	test register under mask instruction
UC	unit check
UE	unit exception
XCR	exclusive OR character register instruction
XHR	exclusive OR halfword register instruction
XR	exclusive OR register instruction
XRI	exclusive OR register immediate instruction

Summary of Changes–Seventh Edition

The seventh edition contains the following changes:

- Information on the Type 3HS Communication Scanner, which operates at line speeds up to 230,600 bps, has been incorporated into Chapter 8.
- Appendixes B and C are updated to include information on the Type 3HS Communication Scanner.

Other minor clarifications and corrections appear in this edition. Technical changes are denoted by a vertical line at the left of the revised text or illustration.

Summary of Changes– Sixth Edition

The sixth edition contains the following changes:

- Models J, K, and L have been added to the IBM 3705-II product line, and descriptions of each model are included in Chapter 1. The 3705-II Models J--L include as standard features (1) a cycle utilization counter register (CUCR), (2) a cycle time of 900 nanoseconds, and (3) a maximum storage capacity of 512K bytes.
- Appendixes B and C are updated to include the new Input and Output instructions and bit definitions for the cycle utilization counter register, and to show changes resulting from the introduction of 3705-II Models J–L.
- TNL GN30-3081 is incorporated into this. That TNL contained information on multiple Type 4 channel adapters and on the remote program loader.

Other minor clarifications and corrections appear in this edition. Technical changes are denoted by a vertical line at the left of the revised text or illustration.

Chapter 1: Introduction

The IBM 3704 and 3705 Communications Controllers are transmission control units with processing capabilities that offer advantages not available in other IBM transmission control units. A control program residing in the controller storage performs many of the functions previously performed by the central processing unit. The assumption of these functions by the controller increases the availability of the processor unit to process other programs and to perform more involved message-processing functions for the data communication system.

The controller is priority-interrupt driven. This allows the control program to handle service requests at five different priority levels.

The communications controller performs, under program control, the normal transmission control unit functions such as line-control, control character recognition, line time-out, character assembly and disassembly, and redundancy checking. The control program can also (1) handle all polling and addressing of communications lines to determine if a line is ready to send or receive data, (2) take over data link control, (3) add framing characters to the beginning and end of blocks of data and (4) translate from line code into code recognizable to a message-processing program, and vice versa. Most error recovery procedures can be handled by the communications controller, thus relieving the processor unit of a time-consuming and storage-consuming data communication function. The control program can also provide dynamic buffering for incoming data and basic message-processing functions.

Host System Interface

The communications controllers may be attached, via the proper channel adapter (discussed later in this chapter) to a System/360 Model 30, 40, 50, 65, 67 (in 65 mode), 75, or 195, or System/370 Models 125 through 3031. A 3705 with a Type 2, Type 3, or Type 4 Channel Adapter requires only one subchannel address, and the adapter may be connected to a byte multiplexer, block multiplexer, or selector channel. (Operation of a Type 4 Channel Adapter in emulation mode requires that the adapter be on a byte multiplexer channel.) The Type 3 Channel Adapter enables the 3705 to be attached to tightly-coupled multiprocessor systems as a shared symmetrical I/O unit, and to a uniprocessor as an I/O unit with an alternate path capability. The Type 1 Channel Adapter in a 3704 or 3705 operates only on a byte multiplexer channel. The channel may require more than one subchannel address, depending on the mode of operation (2701, 2702, or 2703 emulation requires a range of subchannel addresses).

Note: A remote communications controller that does not interface with the host system has no channel adapter.

System Support Programs

Licensed and nonlicensed control programs are available from IBM for scheduling and controlling 3704 and 3705 Communications Controller system resources. Also available are system support programs. These are host processor programs used primarily to generate or assemble a user's control program and to provide IPL and dump facilities for the controller. The support programs operate under control of the host supervisor.

3704 Description

The 3704 is a low-entry control unit that is upward and downward compatible with a 3705 without Extended Addressing. It is available in four models that are defined by the amount of storage installed. Figure 1-1 lists the models of the 3704 and the storage capacity of each model.

Model	*Maximum Number of Lines Attachable*	*Storage Size (K)*
IBM 3704		
A1	32	16
A2	32	32
A3	32	48
A4	32	64

Figure 1-1. Line Attachment Capacity and Storage Size by Model

The 3704 consists of a single module that can contain a Central Control Unit, a control panel, 16K bytes of storage, a channel adpater, and a communication scanner. Either a Type 1 or a Type 2 Scanner can be installed, but the channel adapter is limited to a Type 1 Channel Adapter. The maximum number of communication lines is 32 when the Type 1 Scanner is installed and 10 (26 with additional capability) when the Type 2 Scanner is installed. Figure 1-2 shows the maximum configuration of the 3704 hardware.

3705 Description

The 3705-I and 3705-II are available in 20 and 44 models, respectively. The different models provide varying combinations of storage size and maximum line attachment capacity. All models of the 3705-I and 3705-II, with their respective line attachment capacities and storage sizes, are shown in Figures 1-3 and 1-4. The actual number of lines the controllers can support depends on such factors as the line speeds (data rates) used and the throughput capacity of the control program.

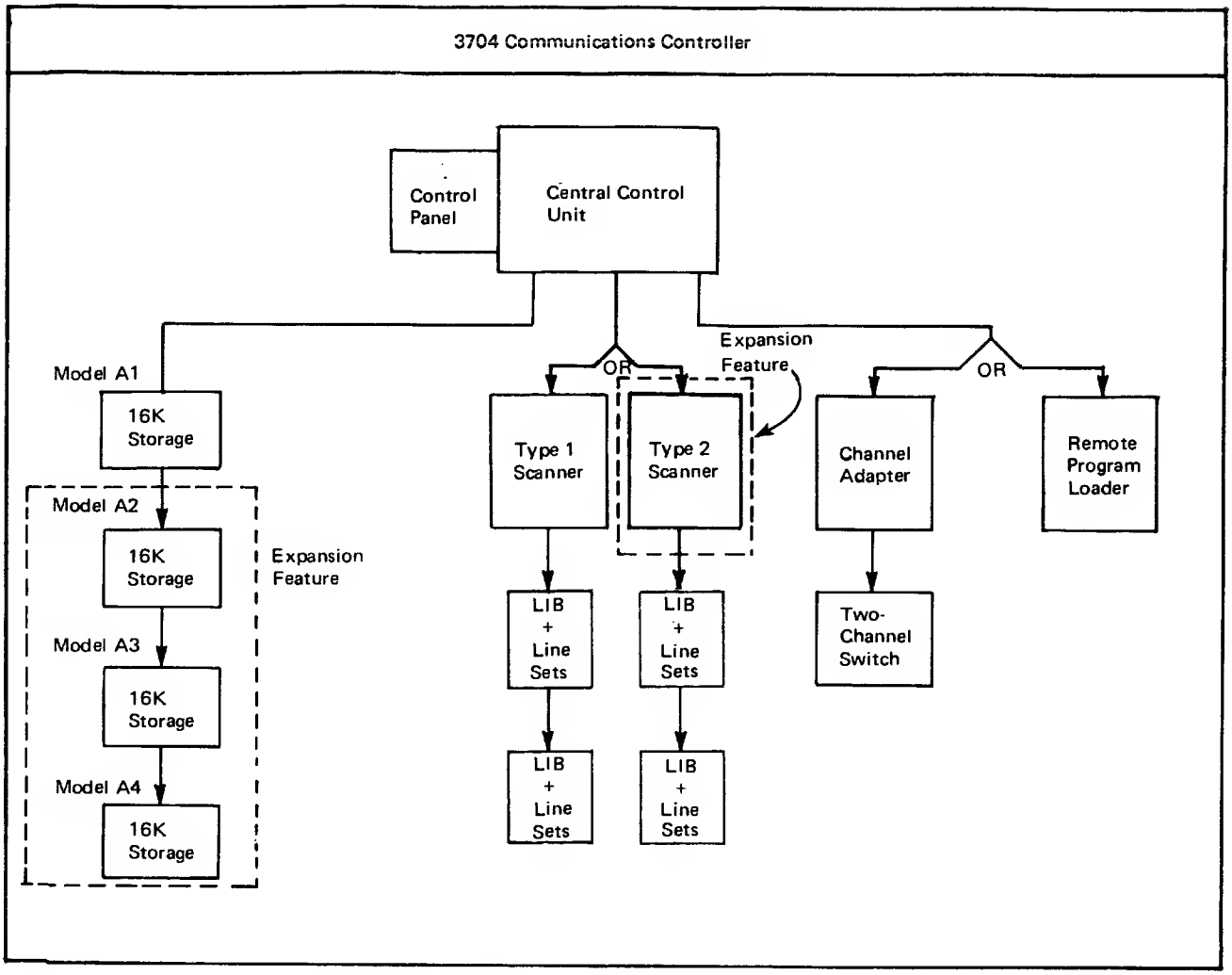


Figure 1-2. Maximum Hardware Configuration of the 3704 Communications Controller

The 'A' and 'E' models of the 3705 consist of a 3705 basic frame containing a central control unit (CCU), a control panel, at least 16K bytes (3705-I) or 32K bytes (3705-II) of storage, and provisions for line interface bases (LIB) and line sets to accommodate up to 64 half-duplex lines. Each LIB can have up to eight line sets (depcnding on line set type), each capable of accommodating one or two half-duplex lines. The 'A' and 'E' models also contain adapters for attaching the controller to communication lines and to the host system. Each higher letter designation (B,C,D,F,G,H,J,K,L) indicates that the controller consists of a basic 3705 frame and one or more attached expansion frames that provide additional storage and line attachment capacity. (Storage increments in a 3705-I may extend into the first, second, or third expansion frame, depending on amount; storage increments in a 3705-II, depending on the model, may extend into the first expansion frame only.) All 'B', 'F', and 'J' models consist of a basic 3705 frame and one expansion frame; all 'C', 'G' and 'K' models consist of a basic 3705 frame and two expansion frames; and all 'D', 'H' and 'L' models consist of a basic 3705 frame and three expansion frames.

Note: The second and third expansion frames of a 3705-II provide additional line attachment capability only.

The basic frame of a 3705-I contains 16K or 48K bytes of storage and a Type 1 or Type 2 Communication Scanner capable of supporting up to four line interface bases (LIB).

Each expansion frame of a 3705-I can contain 0, 32K, or 64K bytes of additional storage and (1) a Type 2 Communication Scanner capable of supporting up to six LIBs, or (2) a Type 3 Communication Scanner and up to four LIBs. The first expansion frame can also contain a Type 2, 3, or 4 Channel Adapter and a two-channel switch.

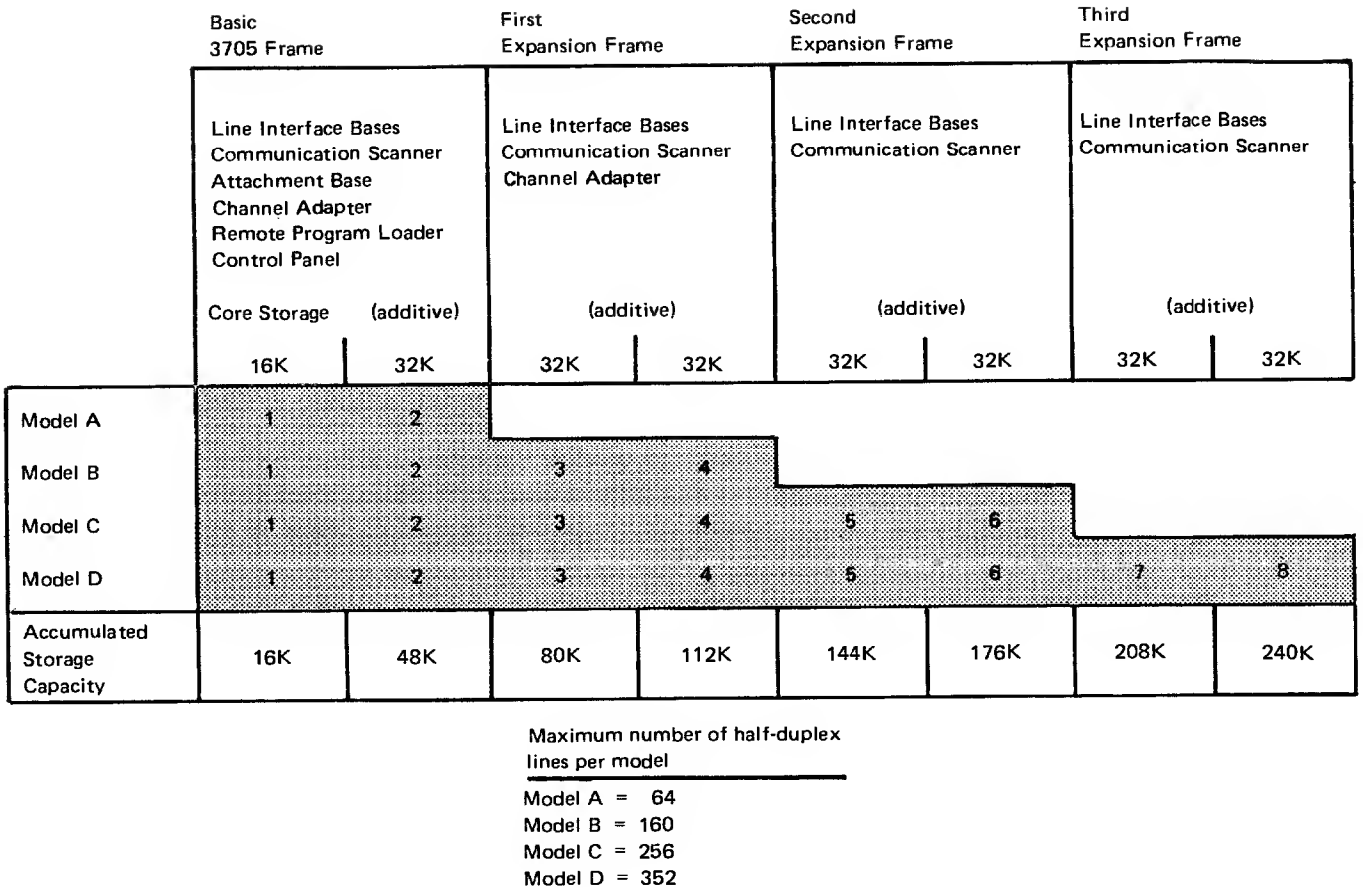


Figure 1-3. IBM 3705-I Line Attachment and Storage Capacity by Model

Storage

The communications controllers, like most central processing units, contain their own internal storage array. This storage provides a residence for the control program and a temporary storage area for data as it is being assembled or disassembled in preparation for transfer to the host processor or a terminal.

3705-I storage ranges from 16K to 240K bytes, in increments of 32K bytes. The read/write storage cycle time is 1.2 microseconds.

3705-II storage ranges from 32K to 256K bytes, in increments of 32K bytes for Models E–H; for Models J–L, 3705-II storage ranges from 320K to 512K bytes in increments of 64K bytes. The read/write storage cycle time is 1.0 microsecond for Models E–H, and 900 nanoseconds for Models J–L.

3704 storage ranges from 16K to 64K bytes in increments of 16K bytes. The read/write storage cycle time is 600 nanoseconds.

Bytes of storage are handled separately or grouped together in fields. A *halfword* is a group of two consecutive bytes and is the basic building block of instructions. A *word* is a group of four consecutive bytes. The location of any field or group of bytes is specified by the address of its leftmost byte.

Central Control Unit

The Central Control Unit (CCU) contains the circuits and data flow paths to execute the instruction set, and to control storage, the communication scanners, and the channel adapters. The CCU operates under control of the programs residing in storage.

Adapters

Two different adapters are required within the communications controller to connect the Central Control Unit with the host channel and the communication lines. These are the *communication scanner* (connection between CCU and communication line), and the *channel adapter* (connection between CCU and host channel). The abbreviation CA is used in this manual to represent channel adapter.

The communication scanners for the communications controllers come in four versions, and the channel adapters come in four versions. Type 1 Scanners, Type 1 CAs, or

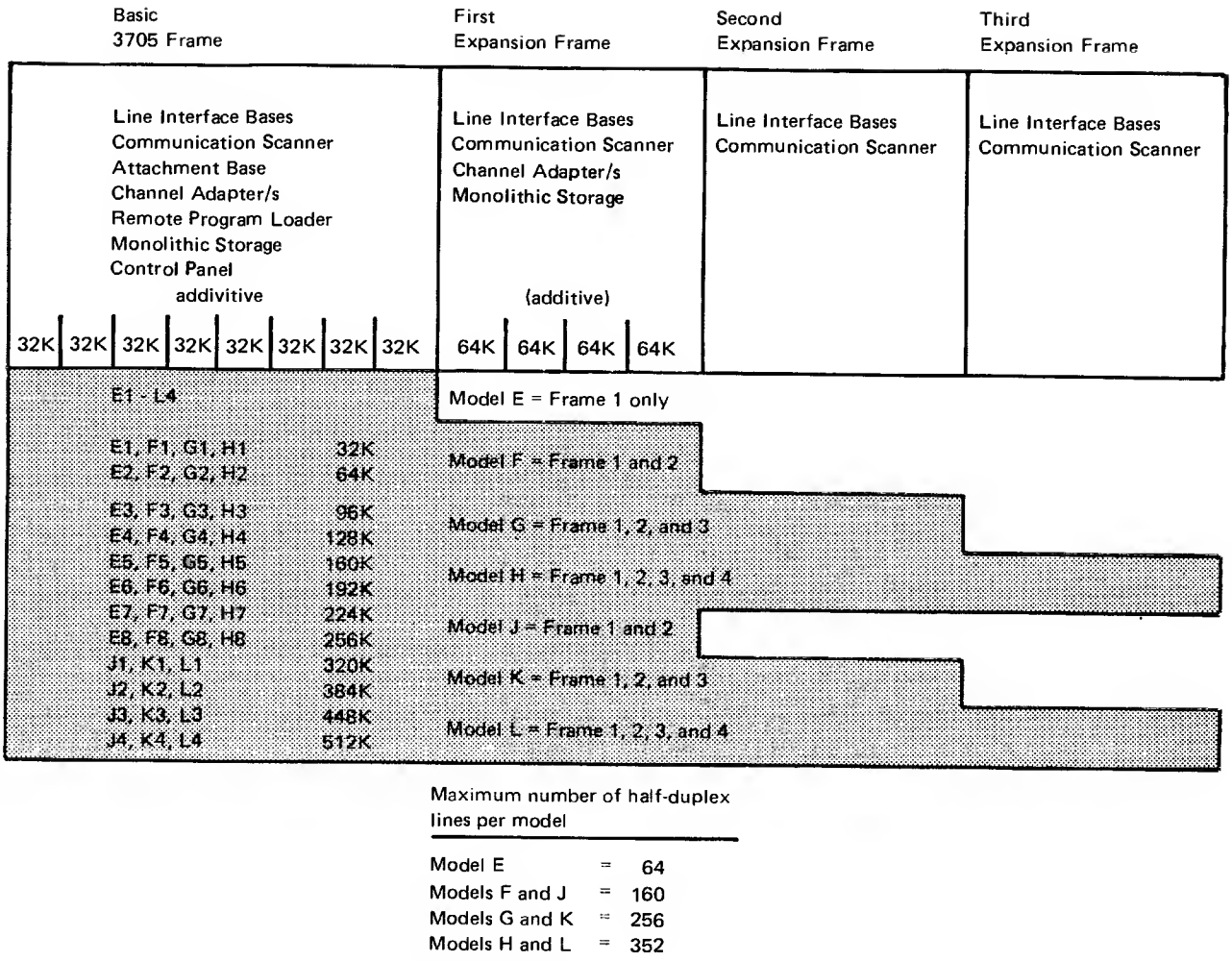


Figure 1-4. IBM 3705-II Line Attachment and Storage Capacity by Model

Type 4 CAs used in Type 1 CA mode or extended buffer mode have low functional hardware capabilities and require more program control than the Type 2, Type 3, and Type 3HS Scanners, Type 2 and Type 3 CAs, or Type 4 CAs used in cycle steal mode. The latter have more functional hardware capabilities and therefore require less program control while providing increased performance as compared to the Type 1 Scanner and Types 1 and 4 Channel Adapters.

Figures 1-5 through 1-8 show all possible combinations of communications scanners and channel adapters, including the maximum number that can be installed for each model of the 3705 controller. The channel adapter in a 3704 is always a Type 1 CA; the scanner may be Type 1 or Type 2.

Channel Adapters

Four types of channel adapters (CAs) are available. The Type 1 and Type 4 CA provide for local attachment to a System/360 or System/370 byte multiplexer channel. These adapters contain the hardware circuits necessary to assist the program in emulating an IBM 2701, 2702, or 2703 as well as to allow operation of the controller in native mode. To operate in emulation mode, the controller requires multiple subchannel addresses: one for each line address and one for native mode IPL.

The Type 1 CA transmits data to and from the byte-multiplexer channel in bursts of up to four bytes. The Type 4 CA transmits data in bursts of up to 32 bytes, if operating in extended buffer mode. When not in this mode, the Type 4 CA transmits to and from the channel in bursts of up to four bytes.

The Type 2 and Type 3 CAs, which are available for the 3705 only, provide for local attachment to a System/370 byte multiplexer, block multiplexer, or selector channel. With the Type 2 or Type 3 CA, the 3705 appears as a single control unit on the host processor channel and uses a single subchannel address. The Type 2 and Type 3 CAs operate in the native (one host subchannel address) mode only.

Channel Adapter Locations on a 3705-I

1st CA Type	2nd CA Type	Frame Location 1st CA	Frame Location 2nd CA
1	–	Frame 1	–
1	2	Frame 1	Frame 2
1	3	Frame 1	Frame 2
2	–	Frame 1	–
2	2	Frame 1	Frame 2
2	3	Frame 1	Frame 2
3	–	Frame 1	–
3	2	Frame 1	Frame 2
3	3	Frame 1	Frame 2
4	–	Frame 1	–
4	2	Frame 1	Frame 2
4	3	Frame 1	Frame 2
4	4	Frame 1	Frame 2

Limitations

1. The first frame of a 3705-I can contain one Type 1, 2, 3, or 4 Channel Adapter.
2. The second frame of a 3705-I can contain one Type 2, 3, or 4 Channel Adapter.
3. No channel adapters are allowed in the third or fourth frame of a 3705-I.
4. No channel adapters are allowed in a 3705-I with a Remote Program Load Feature.

Figure 1-5. Channel Adapter Locations on a 3705-1

All data transfer between 3705 storage and the Type 2 and Type 3 Channel Adapters is by cycle steal operation. That is, when the CA has data to put in storage, it pre-empts (under hardware control) the necessary machine cycles to transfer the data. Data transfers from storage to the channel adapter also use the cycle steal technique. A cycle steal operation by a Type 2 or 3 Channel Adapter is accomplished by hardware circuits and does not affect the logical operation of the program. With a Type 4 CA, cycle steal operations can be accomplished by hardware circuits only, or under program control.

A 3705 can contain up to two (for 3705-I) or up to four (for 3705-II) channel adapters in various combinations of CA types. The 3705 basic frame and the first expansion frame can each contain one or two CAs. The 3705 basic frame can alternatively contain a remote program loader (RPL) (see "Remote Communications Controller" in this chapter) or both a channel adapter and a RPL. Figures 1-5 through 1-8 show the possible combinations.

Two-Channel Switch Feature

A two-channel switch can be installed for the Type 1, Type 2 and Type 4 Channel Adapters. With this feature, the communications controller can be attached to two host processor channels through a single channel adapter. (Both channels can be on the same host processor, or they can be on two different host processors.) However, only one of the channels can be enabled for operation at a time. The enabled channel is selected by means of a manual switch on the control panel.

If two channel adapters are installed, both can have a two-channel switch. This allows the controller to be attached to four host processor channels. The two-channel switch can be installed in a 3705-II having two channel adapters only if the adapters are located in separate frames. The switch is not available if two CAs are installed in the same frame.

Communication Scanners

The communication scanners provide the connection between the communication-line attachment hardware (line interface bases and line sets) and the Central Control Unit via the appropriate attachment base. The primary function of the scanner is to periodically scan the hardware associated with each communication line for service requests.

Four types of communication scanner are available.

Channel Adapter Locations on a 3705-II

1st CA Type	2nd CA Type	3rd CA Type	4th CA Type	Frame Location 1st CA	2nd CA	3rd CA	4th CA
1	–	–	–	Frame 1	–	–	–
1	2	–	–	Frame 1	Frame 2	–	–
1	3	–	–	Frame 1	Frame 2	–	–
2	–	–	–	Frame 1	–	–	–
2	2	–	–	Frame 1	Frame 2	–	–
2	3	–	–	Frame 1	Frame 2	–	–
3	–	–	–	Frame 1	–	–	–
3	2	–	–	Frame 1	Frame 2	–	–
3	3	–	–	Frame 1	Frame 2	–	–
4	–	–	–	Frame 1	–	–	–
4	2	–	–	Frame 1	Frame 1	–	–
4	2	–	–	Frame 1	Frame 2	–	–
4	3	–	–	Frame 1	Frame 2	–	–
4	4	–	–	Frame 1	Frame 1	–	–
4	4	–	–	Frame 1	Frame 2	–	–
4	4	4	–	Frame 1	Frame1	Frame 2	–
4	4	4	–	Frame 1	Frame 2	Frame 2	–
4	4	4	4	Frame 1	Frame 1	Frame 2	Frame 2

Limitations:

1. For the 3705-II, if two channel adapters are in the same frame, then no two-channel switch feature is allowed.
2. If two channel adapters are in the first frame of 3705-II at least one of the adapters must be a Type 4 CA.
3. For the 3705-II, the Remote Program Load feature can co-exist with a channel adapter in frame 1.
4. No channel adapters are allowed in the third or fourth frame of a 3705-II.
5. For the 3705-II, only Models E–H can contain a Type 1 Channel Adapter.

Figure 1-6. Channel Adapter Locations on a 3705-II

Type 1 Scanner: When installed in a 3705, the Type 1 Scanner supports four line interfaces (LIB) with a maximum capability of 64 half-duplex lines and can transfer only one bit at a time to the CCU. The LIBs within this scanner are specified as LIB-1, LIB-2, LIB-3, and LIB-4. Only one Type 1 Scanner can be installed in a 3705, which also prohibits installation of a Type 2 Scanner. This limits the communications controller to a maximum of 64 lines. LIBs are described below under *Line Interface Bases and Line Sets.*

When installed in a 3704, the Type 1 Scanner is capable of supporting only two LIBs (LIB position 1 and LIB position 2). This limits the controller to a maximum of 32 lines.

Type 2 Scanner: The Type 2 Scanner in a 3705 supports either four or six LIBs with a maximum capability of 64 or 96 half-duplex lines, respectively. This scanner transfers a full byte to or from the CCU. Depending on the model of 3705, from one to four Type 2 Scanners can be installed. These scanners are specified as Scanner-1, Scanner-2, Scanner-3, and Scanner-4. Scanner-1 is located in the base module and can support up to four LIBs with 64 lines. Scanners-2, -3, and -4 are located in the expansion modules, and each can support up to six LIBs with 96 lines. The LIBs are specified as LIB-1, LIB-2, LIB-3, LIB-4, LIB-5, and LIB-6 in each scanner, with the exception of Scanner-I, which has only four LIBs.

When installed in a 3704, the Type 2 Scanner is capable of supporting one LIB Type A1, which limits the controller to a maximum of ten lines. Additional capability is available that enables the scanner to support two LIBs in any combination with the exception of two Type 1 LIBs. With this additional capability, the maximum number of lines supported is increased to 26.

Type 3 Scanner: The Type 3 Scanner in a 3705 supports either three or four LIBs with a maximum capacity of 48 or 64 half-duplex lines, respectively. Depending upon program buffering options used, the Type 3 Scanner transfers up to 255 bytes of data to or from the Central Control Unit (CCU) before interrupting the control program for more data or buffers.

Up to four Type 3 Scanners can be installed in a 3705-II. These are specified as Scanner-1, Scanner-2, Scanner-3, and Scanner-4; the base module contains Scanner-1 and the third expansion module contains Scanner-4.

Channel Adapter Type and Quantity	*Communication Scanner Type and Quantity*	*3705-I Model #*	
1 2 3 4	1 2 3	A B C D	
1	1	* x x x	
1	1 2 3 4	* x x x * x x * x *	
1	1 2 3 4	* x x x * x x * x *	
2	1 2 3 4	* x x * x x * x *	
1	1 1 1 2 1 3 2 1 2 2 3 1	* x x * x * * x * *	(Note 6)
2	1 1 1 2 1 3 2 1 2 2 3 1	* x x * x * * x * *	(Note 6)
1	1 2 3 4	* x x x * x x * x *	
2	1 2 3 4	* x x * x x * x *	

Up to three Type 3 Scanners can be installed in a 3705-I. These are specified as Scanner-2, Scanner-3, and Scanner-4; installation of Type 3 Scanners in these positions requires that the Scanner-1 position (base module) contain a Type 2 Scanner.

Scanner-1 can support up to three LIBs and 48 lines; each of the remaining scanners can support up to four LIBs and 64 lines. The LIBs within each scanner are designated LIB-1, LIB-2, LIB-3, and LIB-4 (the latter is not available in a Type 3 Scanner in the Scanner-1 position).

Type 3HS Scanner: The Type 3HS Scanner allows only two line interfaces on a Type 1 LIB. Up to four Type 3HS Scanners can be installed in a 3705-II (the Type 3HS Scanner is not available for the 3705-I or 3704). A Type 3HS Scanner operates at line speeds up to 230,400 bps.

Channel Adapter Type and Quantity	*Communications Scanner Type and Quantity*	*3705-I Model #*	
1 2 3 4	1 2 3	A B C D	
1	1 1 1 2 1 3 2 1 2 2 3 1	* x x * x * * x * *	(Note 6)
2	1 1 1 2 1 3 2 1 2 2 3 1	* x x * x * * x * *	(Note 6)
1	1 2 3 4	* x x x * x x * x *	
2	1 2 3 4	* x x * x x * x *	
1	1 1 1 2 1 3 2 1 2 2 3 1	* x x * x * * x * *	(Note 6)
2	1 1 1 2 1 3 2 1 2 2 3 1	* x x * x * * x * *	(Notes 3 and 6)

Figure 1-7. Channel Adapter and Communication Scanner Combinations

Channel Adapter Type and Quantity	Communication Scanner Type and Quantity	3705-I Model #	
1 2 3 4	1 2 3	A B C D	
1 1	1	* x x	
1 1	1	* x x	
	2	* x x	
	3	* x	(Note 1)
	4	*	
1 1	1	* x x	(Note 1)
1 1	1	* x x	
	2	* x x	
	3	* x	
	4	*	
1 1	1	* x x	
	2	* x x	
	3	* x	
	4	*	
1 1	1 1	* x x	
	1 2	* x	
	1 3	*	
	2 1	* x	(Note 6)
	2 2	*	
	3 1	*	

Channel Adapter Type and Quantity	Communication Scanner Type and Quantity	3705-I Model #	
1 2 3 4	1 2 3	A B C D	
1 1	1	* x x	
	2	* x x	
	3	* x	(Note 4)
	4	*	
1 1	1 1	* x x	
	1 2	* x	
	1 3	*	(Notes 1,
	2 1	* x	4, and 6)
	2 2	*	
	3 1	*	
1 1	1	* x x	
	2	* x x	(Notes 1
	3	* x	and 4)
	4	*	
1 1	1 1	* x x	
	1 2	* x	
	1 3	*	(Notes 1,
	2 1	* x	4, and 6)
	2 2	*	
	3 1	*	

#A 3705-I can contain a remote program loader (RPL) if it does not contain any channel adapters. See Note 5.

*Indicates, for a 3705-I, the smallest model of 3705 required to accommodate the number of channel adapters and communication scanners shown at left.

xIndicates other models of 3705-I that can accommodate the number of channel adapters and communication scanners shown at left; the larger model so indicated may be required if the storage size required exceeds the capacity of the model indicated by *.

Note 1: Communication over both CAs can occur only when the control program is performing emulation subchannel operations over the Type 1 or 4 CA and native subchannel operations over the other CA.

Note 2: A 3705-I cannot contain only Type 3 Scanners; it can contain Type 3 Scanners in each expansion frame if the basic frame contains a Type 2 Scanner.

Note 3: Communication over both Type 4 CAs can occur when the control program performs (1) native subchannel operations over both CAs or (2) native subchannel operations over one CA and Emulation subchannel operations over both CAs.

Note 4: The Type 4 CA must be installed in the basic frame when the controller contains a Type 4 and a Type 2 CA or a Type 4 and a Type 3 CA.

Note 5: The RPL in a 3705-I can co-reside with any combination of Type 1 or Type 2 communication scanners but not with a Type 3 scanner or any channel adapter.

Note 6: The Type 2 Scanner must be in frame 1.

Figure 1-7. Channel Adapter and Communication Scanner Combinations for the 3705-I (Part 2 of 2)

Channel Adapter and Communication Scanner Combinations for the 3705-II (Part 1 of 2)

Channel Adapter Type and Quantity	*Communication Scanner Type and Quantity*	*3705-II Model #*	
1 2 3 4	2 3/3HS *		
1	1	E	
	2	F	
	3	G	(Note 5)
	4	H	
1	1	E and J	
	2	F and J	
	3	G and K	
	4	H and L	
2	1	F and J	
	2	F and J	
	3	G and K	
	4	H and L	
1	1	E and J	
	2	F and J	
	3	G and K	
	4	H and L	
2	1	F and J	
	2	F and J	
	3	G and K	
	4	H and L	
1	1 1	F and J	
	1 2	G and K	
	1 3	H and L	
	2 1	G and K	
	2 2	H and L	
	3 1	H and L	
2	1 1	F and J	
	1 2	G and K	
	1 3	H and L	
	2 1	G and K	
	2 2	H and L	
	3 1	H and L	
1	1	E and J	
	2	F and J	
	3	G and K	
	4	H and L	
2	1	F and J	
	2	F and J	
	3	G and K	
	4	H and L	
1	1	E and J	
	2	F and J	
	3	G and K	
	4	H and L	
2	1	F and J	
	2	F and J	
	3	G and K	
	4	H and L	
1	1 1	F and J	
	1 2	G and K	
	1 3	H and L	
	2 1	G and K	
	2 2	H and L	
	3 1	H and L	

Channel Adapter Type and Quantity	*Communication Scanner Type and Quantity*	*3705-II Model #*	
1 2 3 4	2 3/3HS *		
2	1 1	F and J	
	1 2	G and K	
	1 3	H and L	
	2 1	G and K	
	2 2	H and L	
	3 1	H and L	
1	1	E and J	
	2	F and J	
	3	G and K	
	4	H and L	
2	1	E, F, and J	
	2	F and J	
	3	G, and K	
	4	H and L	
3	1	F and J	
	2	F and J	
	3	G and K	
	4	H and L	
4	1	F and J	
	2	F and J	(Note 4)
	3	G and K	
	4	H and L	
1	1	E and J	
	2	F and J	
	3	G and K	
	4	H and L	
2	1	E, F, and J	
	2	F and J	
	3	G and K	(Note 2)
	4	H and L	
3	1	F and J	
	2	F and J	
	3	G and K	
	4	H and L	
4	1	F and J	
	2	F and J	(Note 4)
	3	G and K	
	4	H and L	
1	1 1	F and J	
	1 2	G and K	
	1 3	H and L	
	2 1	G and K	
	2 2	H and L	
	3 1	H and L	
2	1 1	F and J	
	1 2	G and K	
	1 3	H and L	
	2 1	G and K	(Note 2)
	2 2	H and L	
	3 1	H and L	

Figure 1-8. Channel Adapter and Communication Scanner Combinations for the 3705-II (Part 1 of 2)

Channel Adapter and Communication Scanner Combinations for the 3705-II (Part 2 of 2)

Channel Adapter Type and Quantity	*Communication Scanner Type and Quantity*	*3705-II Model #*	
1 2 3 4	2 3/3HS *		
3	1 1	F and J	
	1 2	G and K	
	1 3	H and L	
	2 1	G and K	
	2 2	H and L	
	3 1	H and L	
4	1 1	F and J	
	1 2	G and K	
	1 3	H and L	(Note 4)
	2 1	G and K	
	2 2	H and L	
	3 1	H and L	
1 1	1	F	
	2	F	
	3	G	(Notes 1 and 5)
	4	H	
1 1	1	F	
	2	F	
	3	G	(Note 5)
	4	H	
1 1	1	F and J	
	2	F and J	
	3	G and K	
	4	H and L	
1 1	1	F and J	
	2	F and J	
	3	G and K	
	4	H and L	

Channel Adapter Type and Quantity	*Communication Scanner Type and Quantity*	*3705-II Model #*	
1 2 3 4	2 3/3HS *		
1 1	1 1	F and J	
	1 2	G and K	
	1 3	H and L	
	2 1	G and K	
	2 2	H and L	
	3 1	H and L	
1 1	1	E, F, and J	
	2	F and J	(Notes 1
	3	G, and K	and 3)
	4	H and L	
1 1	1	E, F, and J	
	2	F and J	(Notes 1
	3	G, and K	and 3)
	4	H and L	
1 1	1 1	F and J	
	1 2	G and K	
	1 3	H and L	(Notes 1
	2 1	G and K	and 3)
	2 2	H and L	
	3 1	H and L	
1 1	1	F and J	
	2	F and J	(Notes 1
	3	G and K	and 3)
	4	H–L	
1 1	1	F and J	
	2	F and J	(Notes 1
	3	G and K	and 3)
	4	H and L	
1 1	1 1	F and J	
	1 2	G and K	
	1 3	H and L	(Notes 1
	2 1	G and K	and 3)
	2 2	H and L	
	3 1	H and L	

*For allowable configurations and attachment capability of Type 3HS Communication Scanners, contact your IBM Marketing Representative.

#Any model of 3705-II may contain a remote program loader (RPL) in addition to channel adapters shown except as indicated by note 4. (The RPL is always located in the first frame of the 3705-II.)

Note 1: Communication over both CAs can occur only when the control program is performing emulation subchannel operations over the Type 1 or 4 CA and native subchannel operations over the other CA.

Note 2: Communication over both Type 4 CAs can occur when the control program performs (1) native subchannel operations over both CAs or (2) native subchannel operations over one CA and emulation subchannel operations over both CAs.

Note 3: The Type 4 CA must be installed in the base module when the controller contains a Type 4 and a Type 2 CA or a Type 4 and and a Type 3 CA.

Note 4: Remote program loader (RPL) for this configuration (four channel adapters) not available.

Note 5: Type 1 CAs cannot be installed on 3705-II, Models J, K, and L.

Figure 1-8. Channel Adapter and Communication Scanner Combinations for the 3705-II (Part 2 of 2)

Type 1 and Type 2 scanners support both synchronous and asynchronous communication lines. Type 3 and Type 3HS scanners support only synchronous lines (SDLC and BSC). The line type (SDLC, BSC, start-stop), character length, bit clocking mechanism (business machine or modem), installed business machine clock speed, and interrupt priority are selected by the program for each line interface.

Attachment Bases

An attachment base is a required feature for support of the 3705 adapters. Two types of attachment bases are available: the Type 1 Attachment Base and the Type 2 Attachment Base. The 3704 does not require an attachment base.

The Type 1 Attachment Base provides common controls to the Central Control Unit for the Type 1 Scanner and the Type 1 Channel Adapter. The Type 2 Attachment Base provides common controls to the Central Control Unit and line addressing controls for the Type 2, Type 3, and Type 3HS Scanners.

One or both of the attachment bases are required, depending on the type of scanner and channel adapter installed in the 3705. The requirements are as follows:

Hardware Installed	*Attachment Base Required*
Type 1 Scanner/Type 1 CA	Type 1 Attachment Base
Type 2 Scanner/Type 1 CA	Type 1 & Type 2 Attachment Base
Type 2, 3, or 3HS Scanner/ Type 2, 3, or 4 CA	Type 2 Attachment Base

Line Interface Bases and Line Sets

Communication lines to and from the teleprocessing stations are attached to the communications controller through a *line interface base* (LIB). The primary functions of the LIB are to drive and terminate all signals between the communication scanners and the line sets and to provide bit clocking.

The line interface base is transparent to the data transferred and has no effect on the control program except for bit clock control.

Several different LIB types are available to meet the needs of a wide variety of line and terminal types. Each LIB type operates identically and is controlled by the communication scanner to which it is attached. However, the design of the various LIB types differs in order to support the many line sets and line configurations that can be attached to them. Refer to *Introduction to the 3704 and 3705 Communications Controllers* (GA27-3051) for a description of the individual LIB and line set types.

The *line set* is the hardware connection between the LIB and the communication line. A given line set type may support attachment of many different terminals and devices; therefore, different data sets or modems may be required. A single line set provides the interface for one or two half-duplex communication lines, depending on the type of interface.

Remote Communications Controller

A controller may be attached directly to a host processor channel via a channel adapter, or it may be located many miles distant from the host processor. In the latter case, the controller (called a *remote* communications controller) requires a remote program loader instead of a channel adapter. The remote controller is connected by a *local/remote communication link* to another controller that is attached to a host processor channel. The same controller (3705-II only) may be equipped with both a remote program loader and one or more channel adapters, allowing it to function either as a local or a remote controller.

Remote Program Loader

The remote program loader consists of a read-only-storage bootstrap program, and an IBM disk storage drive and disk controller that provides the remote controller with an IPL capability. Chapter 11 describes the remote program loader and its capabilities.

SDLC

Synchronous data link control (SDLC) is the line discipline required for the local/remote communication link. The Type 2, Type 3, and Type 3HS Communication Scanners are capable of handling SDLC communications channels. The Type 1 Scanner, with proper program support, can emulate the Type 2 Scanner's SDLC capability. More information on SDLC can be obtained from Chapter 7 of this mannal and from the *Synchronous Data Link Control General Information* manual.

General Programming Concepts

The control program that resides in 3704/3705 storage controls the transfer of data as it passes through the controller between the stations in the teleprocessing network and the host processor.

The primary functions of the control program are related to transmitting and receiving data. But it can also edit and process the data as it passes through the controller.

System Data Flow

In performing its functions, the control program interacts with the communication scanners and the channel adapters to control the flow of data through the data communication system.

Data entered at a terminal is received by the line set and line interface base. The communication scanner recognizes that service is required and receives data from the LIB. The program places the data in storage, where it is then available to the channel adpater to be sent to the host processor channel.

When data is to be transmitted from the host processor to a terminal, the process is reversed. The host channel sends the data to the controller's channel adapter which, under hardware or program control depending on the type of adapter, places the data in storage. An interrupt request to send the data to the LIB and finally to the terminal is then signaled to the control program.

Some processing of the data may be accomplished while the data is in storage. Interaction between the controller adapters is through interrupts and input/output instructions. Figure 1-9 illustrates the data flow to and from the terminal and the host processor through the various parts of the controller.

Input/Output Instructions

The 3704 and 3705 use input and output instructions as the primary link between the hardware and the control program.

All control information and data as it enters or exits the controller passes through the CCU and adapter external registers. These external registers are not directly accessible by the control program; therefore, input and output instructions are used to obtain or change the external register contents. When the control program executes an input instruction, the contents of the specified external register are loaded into a general register. The program then has direct access to that information and can act accordingly.

In the same manner, the control program can load a general register with control information or data for a particular adapter. When that general register is used with the specified external register and an output instruction is executed, the contents of the general register are transferred into the external register. The subject adapter can then take the action specified by the settings of the register bits.

Any data-transfer and adapter-control operations that the control program can perform within the controller are accomplished through input and output instructions.

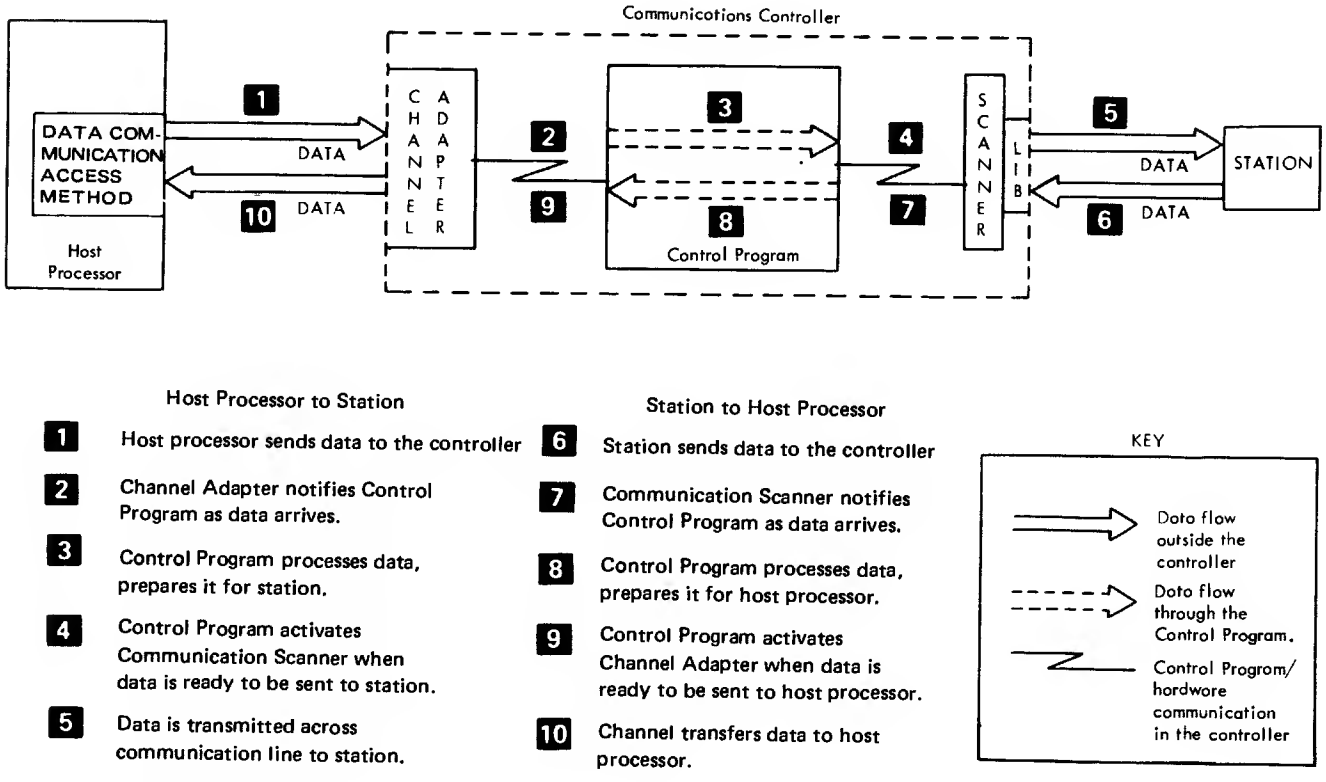


Figure 1-9. System Data Flow

Chapter 2: System Structure

This chapter describes the registers, interrupt scheme, and program levels used in the 3704 and the 3705. The user needs a thorough understanding of these facilities in order to program the controller efficiently.

Note: *Except for Extended Addressing, the text of this chapter applies to the 3704, 3705-I, and 3705-II controllers. The Extended Addressing feature is not available in the 3704.*

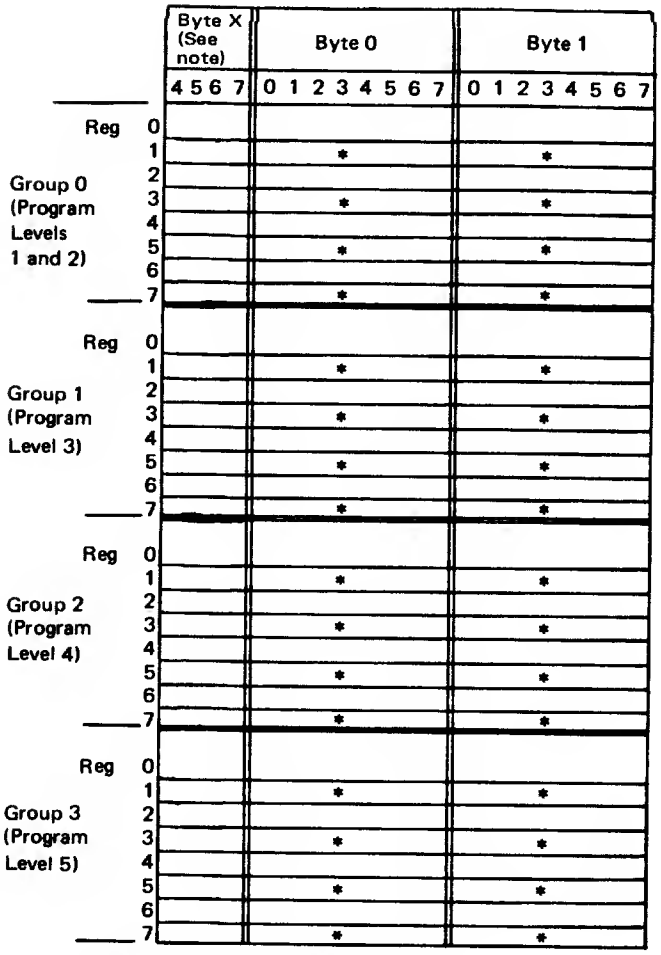
Registers

The controller has two types of registers—general and external. These registers vary in size and location according to how they are used. They can range from one bit to twenty bits. The following paragraphs briefly describe the types, size, and usage of the registers.

General Registers

Thirty-two general registers are available in the controller for program use. These registers are located in a local storage array so as not to occupy usable storage locations. The basic size of each register is one halfword (16 bits). The bits are designated from left to right as byte 0, bits 0-7 and byte 1, bits 0-7. In a 3705 with Extended Addressing (see Chapter 3), each register contains up to four addtional information bits. The information bits are designated from left to right as byte X, bits 4-7; byte 0, bits 0-7; and byte 1, bits 0-7. Without Extended Addressing, byte X is not present, and any reference to it is ignored.

As shown in Figure 2-1, the 32 general registers are divided into four groups of eight registers each. Each group is assigned to a specific program level, except for group 0, which is shared by program levels 1 and 2. (See *Program Levels* in this chapter.) This allows the control program at one level to be interrupted by another level without the need to save registers. The general registers are numbered 0-7 within each group. Only one group of general registers is active at a time—the group associated with the active program level. The registers within the currently active group are directly addressable with program instructions. The control program can gain access to the general registers in a nonactive group by specifying them as external registers in input and output instructions.



*Indicates selectable bytes of general registers

Note: This byte present only in a 3705 with 18 or 20-bit Extended Addressing

Figure 2-1. General Register Groups

Instruction Address Register

General register 0 in each group is the instruction address register (IAR). This register is an implied base register and contains the address of the next instruction to be executed for the associated program level.

Register 0 of the active group is always incremented to point to the next sequential instruction before the current instruction is executed. In most cases, the next halfword is the next instruction to be executed. Sometimes, however, the contents of the instruction address register are changed as the result of the instruction being executed. Execution of a branch instruction, for example, can cause the IAR to be loaded with a storage address other than the one immediately following the current instruction. Refer to the individual instruction definitions in Chapter 4 for the precautions and results of the use of register 0.

External Registers

Each functional unit of the communications controller (Central Control Unit, communication scanner, channel adapter) has a number of hardware registers that are used to store information required for communication between the control program and hardware circuits. These registers are called external registers.

Many of the external registers contain information pertinent to the operation of the hardware and/or the program. By using an input instruction, the control program can load the contents of an external register into a general register where it can operate on the data. Output instructions load an external register with the contents of the general register specified in the instruction.

The external registers that the control program can use are described in the Central Control Unit chapter and in each of the communication scanner and channel adapter chapters in this publication. Appendix A contains a summary of the external register addresses and functions and/or operations associated with each register.

Program Levels

The controller hardware has five operational program levels. Each program level operates similarly to a subroutine and is responsible for particular phases of the system operation. Figure 2-2 shows (1) the program levels in order of priority, (2) the interrupt requests causing entry, and (3) the general register group associated with each level. Program level 1 has the highest priority, and program level 5 has the lowest. Program levels 1, 2, 3, and 4 (referred to as interrupt program levels) provide the program interface between the hardware functional units and program level 5 (referred to as the background program level).

The following is a brief description of each of the five program levels.

- Background Program Level 5: This level is the lowest priority level and is normally active when none of the other four levels requires program cycles. Functions performed by this level should normally include (1) line management (host command interpretation, control of polling and addressing), (2) data and message handling, and (3) control command decoding and execution. This level cannot interrupt another program level.
- Interrupt Program Level 4: The functions performed by this level should normally include (1) overall management of the system resources, (2) buffer management, (3) queue manipulation, and (4) the dispatching of program level 5 tasks. Certain program-controlled interrupt requests and the supervisor call request (generated when the Exit instruction is executed at level 5) are assigned to this program level.
- Interrupt Program Level 3: Level 3 should be used for most of the host processor/channel adapter interaction. This level handles interrupt requests from the channel adapter(s), the interval timer, the control panel Interrupt push button, and the communication processing that can be deferred from level 2. In addition to hardware interrupts, level 3 can be called by program controlled interrupts (PCI) for initiating I/O and for any other services desired by the user. Level 3 interrupts are less critically time-dependent than those assigned to program level 2.
- Interrupt Program Level 2: Because of its high priority, this level services only interrupts from the communication lines for buffer, character or bit service. The control program can request a level 2 interrupt, but for the most part, it is entirely hardware interrupt driven. Normal operational interrupt requests from the communication scanner include (1) Type 1 Scanner bit service interrupts, (2) Type 1 Scanner character service interrupts, (3) Type 2 Scanner character service interrupts and (4) Type 3 or Type 3HS Scanner buffer service interrupts. Only critically time-dependent processing should be done at this level.
- Interrupt Program Level 1: This is the highest-priority program level. It can be masked for channel adapter and scanner checks only when the Central Control Unit is in the test mode. A level 1 interrupt is invoked mainly to service "trouble" indications and is hardware-interrupt driven. Conditions that cause a level 1 request include all critical check conditions, such as (1) program checks, (2) addressing exceptions, (3) Central Control Unit (CCU) checks, and (4) scanner and channel adapter checks. Initial program load (IPL) procedures and address compare interrupts are also handled in this level.

  Because the same group of general registers is used for both level 1 and level 2, the level 1 program should take precautions to save the group 0 registers. A Store instruction with register 0 specified in the R field must be the first instruction executed in program level 1. For this special case, the Store instruction is modified (by hardware) to allow the contents of register 0 to be stored at the second operand location.

Interrupts

The communications controller operates in response to requests from either the control program or the hardware. Since these requests may have varying degrees of urgency, a priority system is used. Each program, CCU, and adapter request is assigned a particular priority level. A request for use of the controller by the

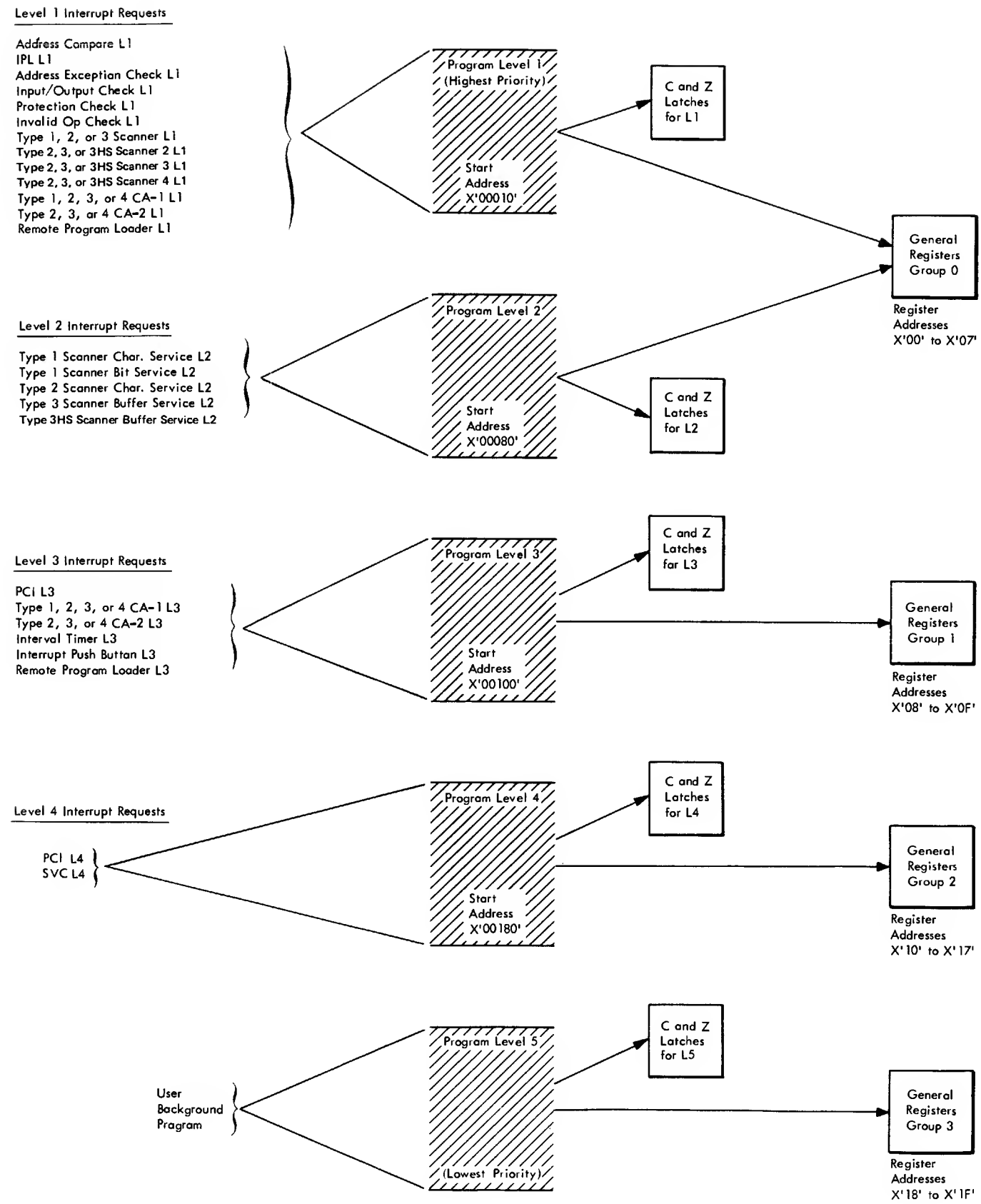


Figure 2-2. Program Levels

control program or hardware functions is called an *interrupt request.*

Each interrupt request is assigned to a *program level.* These program levels are numbered from one to five and determine the priority structure. Program level 1 has the highest priority, and the priority level decreases as the program number increases.

The machine priority controls determine when an interrupt can occur. If the interrupt request is to be allowed, the change from the active program level to the interrupting program level takes place immediately after completion of the current instruction. If several interrupt requests having different priorities are present at the same time, the one with the highest priority obtains use of the controller. When an interrupt request is granted use of the controller, it can be interrupted in that use by another request having a higher priority.

When an interrupt occurs, instruction execution at the lower-priority program level is suspended until instruction execution is completed at the higher-priority level. An interrupt to a specific program level prevents future interrupt requests assigned to either that level or to lower-priority program levels from causing another interrupt until the servicing of the first interrupt is complete.

The controller does not allow a particular interrupt if any of the following conditions exist.

- A higher-priority interrupt request is present.
- The program level to be interrupted is already entered ('interrupt entered' latch is on).
- The interrupt request or the program level to be interrupted is masked.
- A cycle-steal request exists for a Type 2, 3, or 4 Channel Adapter or a Type 3 or 3HS Communication Scanner.

At the time an interrupt is honored, the 'interrupt entered' latch for that program level is turned on. The 'interrupt entered' latch is a hardware latch that signals the controller that the associated program level has been entered. As long as this latch is on, no other interrupt requests to that level are honored. This prohibits interrupts that could destroy necessary information. The 'interrupt entered' latch is not turned off when its associated program level is interrupted by a higher priority level. It is turned off only by an Exit instruction or by a reset condition to the controller.

For an example of the interrupt facility, refer to Figure 2-3. The program at level 4 is being executed, and a level 2 interrupt request occurs (1). The controller hardware forces a branch to the starting address of program level 2 (2), and the program at that level begins servicing the interrupt. A level 3 interrupt request occurs (3), but it is not honored because program level 2 has a higher priority. When the level 2 interrupt has been serviced, the program executes an Exit instruction (4). The controller now allows the next highest-priority interrupt to be serviced. In this example, control is passed to program level 3 at its starting address (5). If, before the level 3 interrupt has been completely serviced another level 3 interrupt request occurs (6), no action is taken because the level 3 'interrupt entered' latch is on. However, as soon as program level 3 executes an Exit instruction (7), signaling the completion of processing and turning off its 'interrupt entered' latch, the controller can honor the second level 3 interrupt request and return control to the starting address of program level 3 (8). When servicing of the latest interrupt is complete and the Exit instruction is executed (9), control is again passed to the highest-priority level that is able to execute. In this case program level 4 is the highest-priority level requiring service (10), so control is returned to it at the instruction following the point of interruption.

At times it may be desirable not to interrupt a particular operation by a higher-priority request. For such cases, a mask can be set to prevent interrupts to a particular program level. See *Masking Program Level Priorities* in Chapter 5.

When an interrupt occurs, instruction execution at that level begins with the instruction located at the starting address of that level. The starting address of each interrupt level is a permanently assigned storage location. The instruction(s) beginning at these fixed locations must direct the control program to the correct routine(s) to handle the particular interrupt. The remainder of the instructions for a particular program level need not be located in any specific storage area. In addition, some routines may be used by more than one program level. However, in this case, the execution of that routine will be at the priority level of the currently active program level.

The starting addresses for the four program levels that can cause an interrupt are:

Level	*Starting Address (Hex)*
Program Level 1	X'00010'
Program Level 2	X'00080'
Program Level 3	X'00100'
Program Level 4	X'00180'

When a program level has completed its interrupt servicing, it must execute an Exit instruction. The Exit instruction causes the 'interrupt entered' latch for that level to be reset and allows control to be passed to the next higher-priority program level requiring service.

When the Exit instruction is executed at program level 5, a supervisor call interrupt request for level 4 (SVC L4) is set. This is the only manner in which program level 5 can generate an interrupt request.

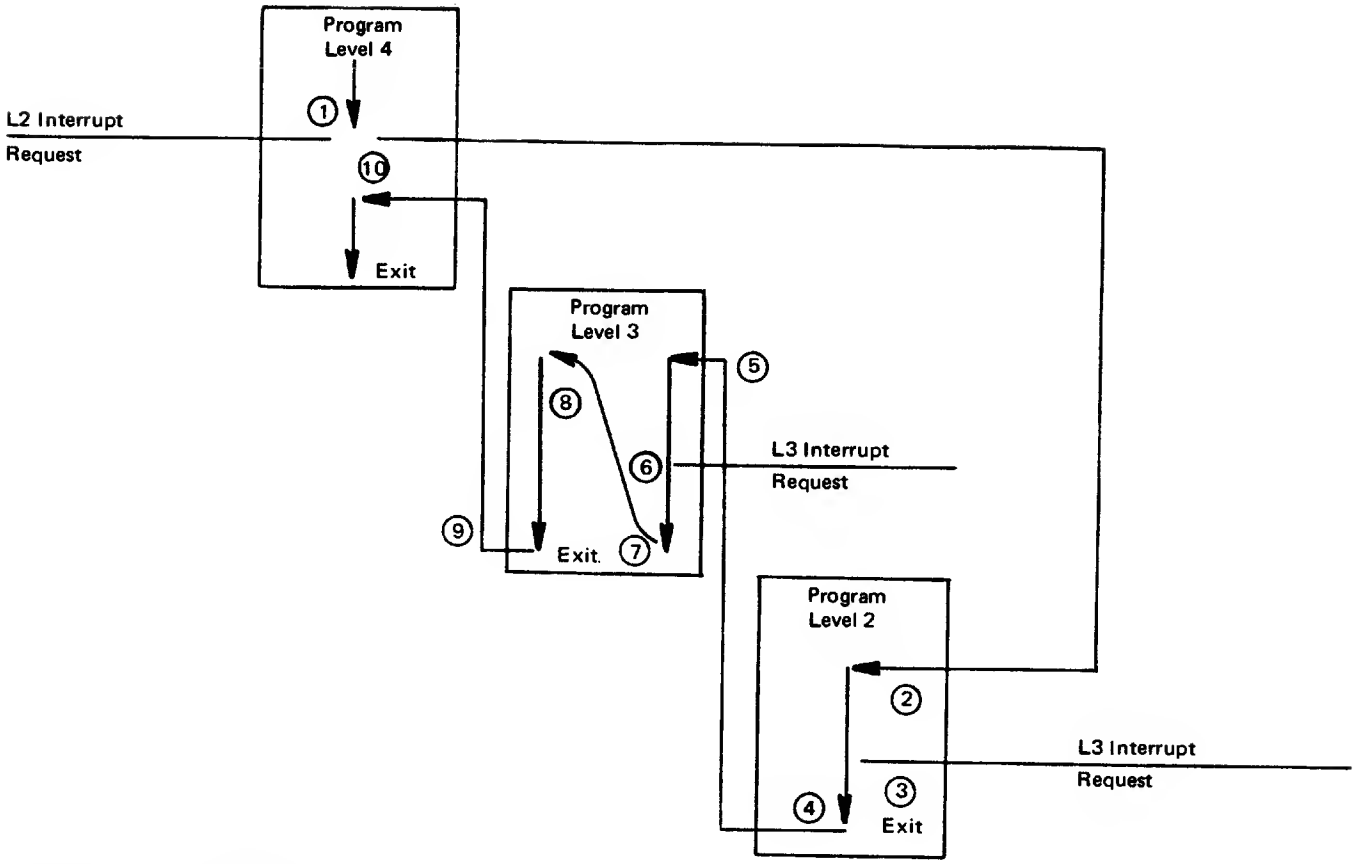


Figure 2-3. Interrupt Priority Example

Chapter 3: Storage and Line Addressing

This chapter describes the storage addressing scheme and the format for addressing the individual communication lines.

Storage Addressing

Byte locations in storage are consecutively numbered starting with 0; each number is considered the address of the corresponding byte. A group of bytes in storage is addressed by the high-order byte of the group. The number of bytes in the group is either implied or explicitly defined by the operation.

The basic addressing scheme uses a 16-bit binary address to accommodate a maximum byte address of 65,535. The two bytes of the halfword used for addressing are specified from left to right as byte 0 and byte 1. The bits within these two bytes are numbered left to right from 0 to 7. All general registers and the CCU external registers involved in addressing storage are two bytes in length and the bit positions correspond to the basic addressing scheme.

Figure 3-1 shows the storage address bit positions as they are used in the basic addressing scheme.

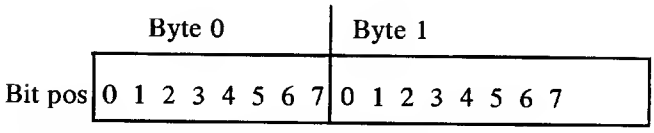


Figure 3-1. Storage Address Bit Positions (Without Extended Addressing)

Storage addressing wraps at the maximum byte address of 65,535. This means that if, in the formation of a storage address, the binary representation of the address is *greater* than 16 bits in length, the actual address used will be only the address formed in the low-order 16 bits. For example, if the formation of a storage address uses a base address of X'A080' and a displacement of X'6010', the combined address does not include the carry of the high-order bit and therefore generates an effective address of X'0090'.

An addressing exception is recognized if the storage address is greater than the number of installed storage locations but less than the point of storage wrap. For example, in the 3705-I controller, any attempt to address storage between 16,384 (or 49,152, whichever model is installed) and 65,535 results in an addressing exception. See *Program Checks* in Chapter 5.

Instructions and halfword operands must be located on integral halfword boundaries in storage. A boundary is called integral for a unit of information when its storage address is a multiple of the length of the unit in bytes. For example, a word (four bytes) must be located in storage so that its address is a multiple of the number 4. A halfword (two bytes) must have an address that is a multiple of the number 2.

Storage addresses are expressed in binary form. In binary, integral boundaries for halfwords and words can be specified only by an address in which one or two low-order bits, respectively, are zero. For example, the integral boundary for a word is a binary address in which the two low-order positions are zero.

Extended Addressing

When a controller contains more than 64K bytes of storage, the basic 16-bit address structure is not sufficient. To address the storage positions above 64K, additional address bits are required. Two bits, designated as byte X, bits 6 and 7, allow address generation up to the maximum of 245,760 bytes, for a 3705-I, or 262,144 bytes, for 3705-II, Models E–H. In addition (for 3705-II, Models J–L only), byte X, bit 5 allows address generation up to the maximum of 524,288 bytes. The use of byte X is referred to as Extended Addressing. Figure 3-2 illustrates the storage address bit positions used by the affected registers with Extended Addressing.

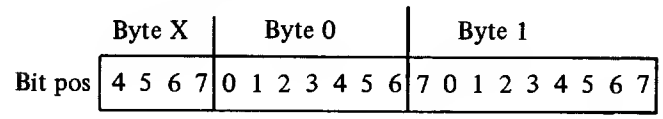


Figure 3-2. Storage Address Bit Positions (With Extended Addressing)

With Extended Addressing, the Central Control Unit data flow registers and all general registers are expanded to 18 bits (20 bits for 3705-II, Models J–L). The additional bits (byte X, bits 4-7) must be handled as an integral part of the register regardless of the address being operated on. The only exceptions are: (1) byte X is ignored for output instructions not involved in addressing storage and can be set to either 1 or 0, and (2) byte X is set to zeros for input instructions not involved in addressing storage.

Storage wrap and addressing exception also apply to Extended Addressing. However, with 18-bit Extended Addressing, the point of storage wrap is 262,144, and a carry from the value wraps back to zero. The range of addresses that cause an addressing exception is from the maximum of storage locations installed to the point of storage wrap. For example, if the storage installed in a 3705-I is 180,224 bytes, then any address generated between 180,224 and 262,144 causes an addressing exception. Addressing exceptions also apply to the 3705-II.

Note: *This manual is based primarily on the basic 16-bit addressing scheme. However, any exceptions in operation due to Extended Addressing are pointed out and explained by programming notes. The 3704 does not have the Extended Addressing capability.*

Interface Addressing

The lines attached to a communication scanner are assigned interface addresses when the machine is installed. The interface address assigned to a given line is determined by the physical location of the line interface hardware and by the type of scanner (Type 1, Type 2, Type 3, or Type 3HS) installed in the controller.

Sixteen interface addresses are assigned to each Line Interface Base position, permitting a total of 352 lines on the 3705 with the maximum configuration. To uniquely address each of these lines requires nine address bits. Figures 3-3 and 3-4 show the address bits and their interpretation. The S field specifies which scanner the interface is attached to and is used when one or more Type 2, Type 3, or Type 3HS Scanners are installed. The S field is not used with a Type 1 Scanner, since only one Type 1 Scanner can be installed in a controller. The L field specifies the Line Interface Base number within the specified scanner. Only two bits of the L field (bits 3 and 4) are used with a Type 1 Scanner since four is the maximum number of LIBs that can be installed in a Type 1 Scanner. The I field is the position of the interface attachment in the specified LIB.

Whether all 16 interface addresses assigned to a given LIB position are usable depends on the type of LIB installed in that LIB position, and the type and number of line sets installed in that LIB.

With a Type 1 Scanner: When an interface address is passed to the program by an Input X'41' instruction, the interface address bits 3-8 are placed in byte 0, bits 6-7, and byte 1, bits 0-3, of the general register specified in the instruction. Byte 0, bit 4 is set to 1, and the remaining bits are set to 0.

This alignment associates a specific 2-byte storage address with each interface address. These storage addresses point to consecutive 16-byte blocks in storage. This area of storage can be directly addressed and contains a control block for control information and data handling routine addresses required for servicing an interface. Figure 3-5 shows the specific storage address associated with each interface position.

For consistency, when the program provides an interface address to the Type 1 Scanner via an Output X'47' instruction, the same alignment must be maintained.

With a Type 2, 3, or 3HS Scanner: When an interface address is passed to the program by an Input X'40' instruction, the interface address bits 0-8 are placed in byte 0, bits 6-7, and byte 1, bits 0-6, of the specified general register. Byte 0, bit 4 is set to 1 and the remaining bits of the register are set to 0.

This alignment associates a specific 2-byte storage address with each interface address. These storage addresses are aligned on halfword boundaries and are arranged so that this area in storage can be used as a vector table to direct the control program to a routine that is designed to service the particular interface type. Figure 3-5 shows the storage address for each specific interface position.

For consistency, when the program provides an interface address to the Type 2, 3, or 3HS Scanner via an Output X'40' instruction, the same alignment must be maintained.

Note: *Interface addressing in the 3704 with a Type 2 Scanner follows the same addressing scheme as a 3705 Type 2 Scanner-1, LIB position 1. Interface address bits 5, 6, 7, and 8 specify lines 0-F in LIB Type A1. However, addresses 0 and 2 are reserved for high-speed line sets only, and addresses 1, 3, C, D, E, and F are not used.*

LIB and Line Addressing

Each line or autocall interface must be addressable for the following:

1. Scan addressing
2. Program addressing

Scan addressing and program addressing are performed differently for the Type 1, Type 2, Type 3, or Type 3HS Communication Scanners. These functions are described in detail in the communication scanner chapters.

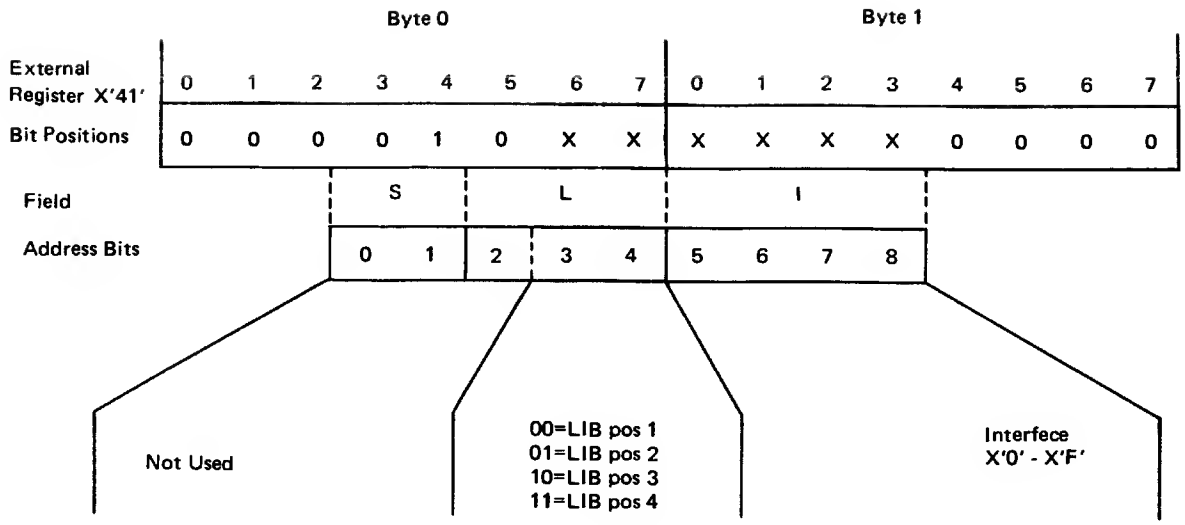


Figure 3-3. Type 1 Scanner Interface Address Bits

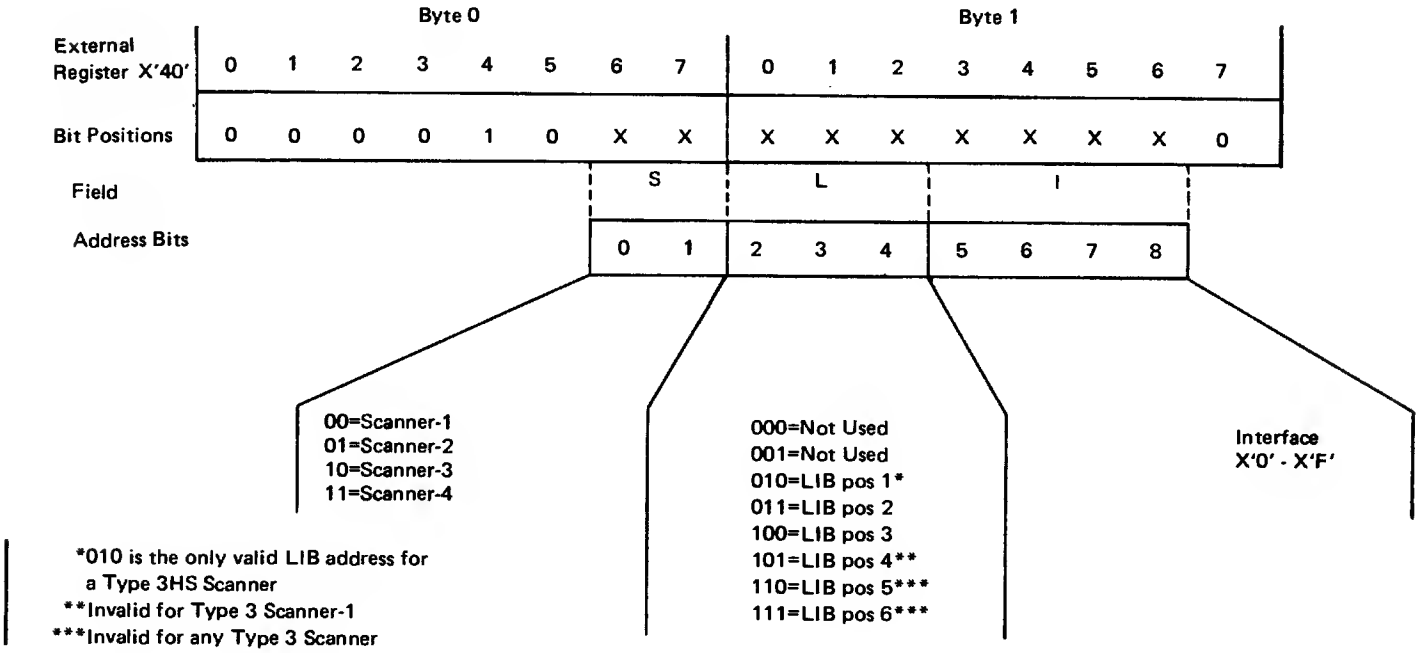


Figure 3-4. Types 2, 3, and 3HS Scanner Interface Address Bits

Type 1, 2, and 3 Communication Scanners

		S/L (HEX) I→	INTERFACE ADDRESS ASSIGNMENTS (HEX) 0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
			STORAGE ADDRESSES (HEX) *															
Type 1 Scanner	LIB position 1	00 —	800	810	820	830	840	850	860	870	880	890	8A0	8B0	BC0	BD0	BE0	BF0
	2	01 —	900	910	920	930	940	950	960	970	980	990	9A0	9B0	9C0	9D0	9E0	9F0
	3	02 —	A00	A10	A20	A30	A40	A50	A60	A70	A80	A90	AA0	AB0	AC0	AD0	AE0	AF0
	4	03 —	B00	B10	B20	B30	B40	B50	B60	B70	B80	B90	BA0	BB0	BC0	BD0	BE0	BF0
	3705 BASIC FRAME		STORAGE ADDRESSES (HEX)															
Type 2 or Type 3 Scanner-1	LIB position 1	02 —	840	842	844	846	848	84A	84C	84E	850	852	854	856	858	85A	85C	85E
	2	03 —	860	862	864	866	868	86A	86C	86E	870	872	874	876	878	87A	87C	87E
	3	04 —	880	882	884	886	888	88A	88C	88E	890	892	894	896	898	89A	89C	89E
	4**	05 —	8A0	8A2	8A4	8A6	8A8	8AA	8AC	8AE	8B0	8B2	8B4	8B6	8B8	8BA	8BC	8BE
	FIRST EXPANSION FRAME		STORAGE ADDRESSES (HEX)															
Type 2 or Type 3 Scanner-2	LIB position 1	0A —	940	942	944	946	948	94A	94C	94E	950	952	954	956	958	95A	95C	95E
	2	0B —	960	962	964	966	968	96A	96C	96E	970	972	974	976	978	97A	97C	97E
	3	0C —	980	982	984	986	988	98A	98C	98E	990	992	994	996	998	99A	99C	99E
	4	0D —	9A0	9A2	9A4	9A6	9A8	9AA	9AC	9AE	9B0	9B2	9B4	9B6	9B8	9BA	9BC	9BE
	5**	0E —	9C0	9C2	9C4	9C6	9C8	9CA	9CC	9CE	9D0	9D2	9D4	9D6	9DB	9DA	9DC	9DE
	6**	0F —	9E0	9E2	9E4	9E6	9E8	9EA	9EC	9EE	9F0	9F2	9F4	9E6	9E8	9FA	9FC	9FE
	SECOND EXPANSION FRAME		STORAGE ADDRESSES (HEX)															
Type 2 or Type 3 Scanner-3	LIB position 1	12 —	A40	A42	A44	A46	A48	A4A	A4C	A4E	A50	A52	A54	A56	A5B	A5A	A5C	A5E
	2	13 —	A60	A62	A64	A66	A68	A6A	A6C	A6E	A70	A72	A74	A76	A7B	A7A	A7C	A7E
	3	14 —	A80	A82	A84	A86	A88	A8A	A8C	ABE	A90	A92	A94	A96	A9B	A9A	A9C	A9E
	4	15 —	AA0	AA2	AA4	AA6	AA8	AAA	AAC	AAE	AB0	AB2	AB4	AB6	ABB	ABA	ABC	ABE
	5**	16 —	AC0	AC2	AC4	AC6	AC8	ACA	ACC	ACE	AD0	AD2	AD4	AD6	AD8	ADA	ADC	ADE
	6**	17 —	AE0	AE2	AE4	AE6	AE8	AEA	AEC	AEE	AF0	AF2	AF4	AF6	AFB	AFA	AFC	AFE
	THIRD EXPANSION FRAME		STORAGE ADDRESSES (HEX)															
Type 2 or Type 3 Scanner-4	LIB position 1	1A —	B40	B42	B44	B46	B48	B4A	B4C	B4E	B50	B52	B54	B56	B58	B5A	B5C	B5E
	2	1B —	B60	B62	B64	B66	B68	B6A	B6C	B6E	B70	B72	B74	B76	B78	B7A	B7C	B7E
	3	1C —	B80	B82	B84	B86	B88	B8A	B8C	BBE	B90	B92	B94	B96	B98	B9A	B9C	B9E
	4	1D —	BA0	BA2	BA4	BA6	BA8	BAA	BAC	BAE	BB0	BB2	BB4	BB6	BB8	BBA	BBC	BBE
	5**	1E —	BC0	BC2	BC4	BC6	BCB	BCA	BCC	BCE	BD0	BD2	BD4	BD6	BD8	BDA	BDC	BDE
	6**	1E —	BE0	BE2	BE4	BE6	BEB	BEA	BEC	BEE	BF0	BF2	BF4	BF6	BF8	BFA	BFC	BFE

* Storage address X'6F0' is used for character service **Type 2 Scanner only

Type 3HS Communication Scanner		INTERFACE ADDRESS ASSIGNMENTS (HEX) S/L (HEX) I→ 0	1	2
		STORAGE ADDRESSES (HEX)		
Scanner-1	3705 BASIC FRAME LIB position 1	02 — 840	N/A	B44
Scanner-2	FIRST EXPANSION FRAME LIB position 1	0A — 94D	N/A	944
Scanner-3	SECOND EXPANSION FRAME LIB position 1	12 — A4D	N/A	A44
Scanner-4	THIRD EXPANSION FRAME LIB position 1	1A — B4D	N/A	B44

Figure 3-5. Storage Address Assignments

The communications controller contains 51 executable instructions that can be used to tailor a control program to meet the specific needs of the data communication system. The instruction set provides the greatest possible program flexibility within a minimum amount of storage.

This chapter gives the general instruction formats, and describes each individual instruction.

Note: *Except for the functions provided by the Extended Addressing feature, the instruction and operand descriptions in this chapter apply to both the 3704 and the 3705.*

Figure 4-1 shows the op code bit structures, operand fields, and instruction execution times (in number of storage cycles). A storage cycle for the 3704 (read *or* write) is 600 nanoseconds, for the 3705-I (read *and* write) is 1.2 microseconds. The 3705-II storage cycle time (read *and* write) is 1.0 microsecond or 900 nanoseconds. The asterisks in the C, Z column designate the instructions that can alter the C and Z condition latches.

Figure 4-2 shows the basic mnemonic designations and assembler operand field designations for the various instructions.

Any attempt at program levels 2, 3, 4, or 5 to execute an operation code other than one of the 51 specified instructions results in a level 1 interrupt with the invalid op check bit set on in the CCU interrupt request group 1 register. An attempt to execute an invalid op code in program level 1 sets the program check in L1 bit in the CCU check register along with the invalid op check bit and is handled as a CCU check. In all cases, instruction execution is suppressed. See *CCU Checks* in Chapter 5.

Instruction Format

The instruction length can be either one or two halfwords. All instructions must be located in storage on integral halfword boundaries.

The eight basic instruction formats are denoted by the format codes RR, RS, RT, RA, RSA, RE, RI and EXIT. The format codes express, in general terms, the operation to be performed. RR denotes a register-to-register operation; RS, a register-storage operation; RSA, a register-to-storage with addition operation; RT, a branch operation; RA, a register-to-immediate address operation; RE, a register-to-external register operation; RI, a register-to-immediate operand operation; and EXIT, a program level exit operation.

To help describe the execution of instructions, operands are designated as either first or second operands. For RR format instructions, the first and second operands are denoted by the number following the name of the field (for example R1, R2).

Instruction Operand Fields

Instruction operands are in four classes: (1) immediate operands in the instructions themselves, (2) operands in external registers, (3) operands in the active group of general registers, and (4) explicitly addressed operands in storage.

The following fields represent the operands in the instruction format.

Immediate Operands

I Field: The I field in RI format instructions contains an 8-bit immediate data field.

A Field: With Extended Addressing, the A field in RA format instructions contains an 18-bit (20-bit for 3705-II, Models J–L) immediate data field. Without Extended Addressing, the A field is treated as a 16-bit immediate data field, and bits 12, 13, 14, and 15 of the instruction are ignored.

External Register Operands

E Field: The E field in RE format instructions specifies the hexadecimal address of an external register operand. This field is used only for input and output instructions. Throughout this text, many references are made to input and output instructions. These references specify the value of the E field in the form X'*nn*', where *nn* is the hexadecimal address of the external register. Appendix A shows the external register addresses and functions.

General Register Operands

R Field: The R field in RI, RS, RE, RR, RA, RSA and some RT format instructions specifies the general register in the active group that contains the first operand. For byte operations, the register specified by this field must be an odd-numbered register. For all other operations, any one of the eight general registers in the active group may be specified.

For STH and ST instructions, if the R field is zero, a constant of all zeros is selected as the operand, rather than the contents of register 0.

Notes:

1. *Use 18-bit operands when addressing storage locations above 64K bytes up to and including 256K bytes.*
2. *Use 20-bit operands when addressing storage locations above 256K byte up to and including, 512K bytes. (3705-II Models J–L only.)*

Name	Instruction	C, Z	3704 Cycles	3705 Cycles	FORMAT 0 1 2 3	4 5 6 7	8 9 10 11	12 13 14 15
B	Branch		2	1	1 0 1 0			
BCL	Branch on C Latch		2	1	1 0 0 1	T		± ✱
BZL	Branch on Z Latch		2	1	1 0 0 0			
BCT	Branch on Count		3	1	1 0 1 1	R N	1 T	±
BB	Branch on Bit		3	1	1 1 M M		M T	✱
LRI	Load Register Immediate	*	3	1	1 0 0 0 0			
ARI	Add Register Immediate	*	3	1	1 0 0 1 0			
SRI	Subtract Register Immediate	*	3	1	1 0 1 0 0			
CRI	Compare Register Immediate	*	3	1	1 0 1 1 0	R N	I	
XRI	Exclusive Or Register Immediate	*	3	1	1 1 0 0 0			
ORI	Or Register Immediate	*	3	1	1 1 0 1 0			
NRI	And Register Immediate	*	3	1	1 1 1 0 0			
TRM	Test Register under Mask	*	3	1	1 1 1 1 0			
LCR	Load Character Register	*	3	1	0	0	0 0 0 0 1 0 0 0	
ACR	Add Character Register	*	3	1	0	0	0 0 0 1 1 0 0 0	
SCR	Subtract Character Register	*	3	1	0	0	0 0 1 0 1 0 0 0	
CCR	Compare Character Register	*	3	1	0 R_2 N_2	0 R_1 N_1	0 0 1 1 1 0 0 0	
XCR	Exclusive Or Character Register	*	3	1	0	0	0 1 0 0 1 0 0 0	
OCR	OR Character Register	*	3	1	0	0	0 1 0 1 1 0 0 0	
NCR	And Character Register	*	3	1	0	0	0 1 1 0 1 0 0 0	
LCOR	Load Character with Offset Register	*	3	1	0	0	0 1 1 1 1 0 0 0	
ICT	Insert Character and Count		5	2	0	0	0 0 0 1 0 0 0 0	
STCT	Store Character and Count		5	2	0	0 R N	0 0 1 1 0 0 0 0	
IC	Insert Character	*	4	2	0	1	0 D	
STC	Store Character		4	2	0 B	1	1 D	
LH	Load Halfword	*	4	2	0	0	0 D	1
STH	Store Halfword		4	2	0	0 R	1 D	1
L	Load	*	5	2#	0	0	0 D	1 0
ST	Store		5	2#	0	0	1 D	1 0
LHR	Load Halfword Register	*	3	1	0	0	1 0 0 0 0 0 0 0	
AHR	Add Halfword Register	*	3	1	0	0	1 0 0 1 0 0 0 0	
SHR	Subtract Halfword Register	*	3	1	0	0	1 0 1 0 0 0 0 0	
CHR	Compare Halfword Register	*	3	1	0	0	1 0 1 1 0 0 0 0	
XHR	Exclusive Or Halfword Register	*	3	1	0	0	1 1 0 0 0 0 0 0	
OHR	OR Halfword Register	*	3	1	0	0	1 1 0 1 0 0 0 0	
NHR	And Halfword Register	*	3	1	0	0	1 1 1 0 0 0 0 0	
LHOR	Load Halfword with Offset Register	*	3	1	0 R_2	0 R_1	1 1 1 1 0 0 0 0	
LR	Load Register	*	3	1	0	0	1 0 0 0 1 0 0 0	
AR	Add Register	*	3	1	0	0	1 0 0 1 1 0 0 0	
SR	Subtract Register	*	3	1	0	0	1 0 1 0 1 0 0 0	
CR	Compare Register	*	3	1	0	0	1 0 1 1 1 0 0 0	
XR	Exclusive Or Register	*	3	1	0	0	1 1 0 0 1 0 0 0	
OR	OR Register	*	3	1	0	0	1 1 0 1 1 0 0 0	
NR	And Register	*	3	1	0	0	1 1 1 0 1 0 0 0	
LOR	Load with Offset Register	*	3	1	0	0	1 1 1 1 1 0 0 0	
BALR	Branch & Link Register		4	2	0	0	0 1 0 0 0 0 0 0	
IN	Input		2	1	0	0 R	− E	1 1 0 0
OUT	Output		2	1	0 E	0	E	0 1 0 0
BAL	Branch & Link		3	2	1 * 0 1 1 1		0 0 0 0	16 A 31
LA	Load Address		3	2	1 0 1 1 1		0 0 1 0	A
EXIT	Exit		2	1	1 0 1 1 1	0 0 0 0	1 0 0 0	0 0 0 0

* = Instructions that can alter condition latches.
✱1 = −
0 = +
# = 3 Cycles with Extended Addressing

Figure 4-1. Instruction Bit Structure

Instruction	Format Code	Mnemonic	Operand Field Format
Add Character Register	RR	ACR	R1(N1),R2(N2)
Add Halfword Register	RR	AHR	R1,R2
Add Register	RR	AR	R1,R2
Add Register Immediate	RI	ARI	R(N),I
AND Character Register	RR	NCR	R1(N1),R2(N2)
AND Halfword Register	RR	NHR	R1,R2
AND Register	RR	NR	R1,R2
AND Register Immediate	RI	NRI	R(N),I
Branch	RT	B	T
Branch and Link	RA	BAL	R,A
Branch and Link Register	RR	BALR	R1,R2
Branch on Bit	RT	BB	R(N,M),T
Branch on Count	RT	BCT	R(N),T
Branch on C Latch	RT	BCL	T
Branch on Z Latch	RT	BZL	T
Compare Character Register	RR	CCR	R1(N1),R2(N2)
Compare Halfword Register	RR	CHR	R1,R2
Compare Register	RR	CR	R1,R2
Compare Register Immediate	RI	CRI	R(N),I
Exclusive OR Character Register	RR	XCR	R1(N1),R2(N2)
Exclusive OR Halfword Register	RR	XHR	R1,R2
Exclusive OR Register	RR	XR	R1,R2
Exclusive OR Register Immediate	RI	XRI	R(N),I
Exit	EXIT	EXIT	——
Input	RE	IN	R,E
Insert Character	RS	IC	R(N),D(B)
Insert Character and Count	RSA	ICT	R(N),B
Load	RS	L	R,D(B)
Load Address	RA	LA	R,A
Load Character Register	RR	LCR	R1(N1),R2(N2)
Load Character with Offset Reg.	RR	LCOR	R1(N1),R2(N2)
Load Halfword	RS	LH	R,D(B)
Load Halfword Register	RR	LHR	R1,R2
Load Halfword with Offset Reg.	RR	LHOR	R1,R2
Load Register	RR	LR	R1,R2
Load Register Immediate	RI	LRI	R(N),I
Load with Offset Register	RR	LOR	R1,R2
OR Character Register	RR	OCR	R1(N1),R2(N2)
OR Halfword Register	RR	OHR	R1,R2
OR Register	RR	OR	R1,R2
OR Register Immediate	RI	ORI	R(N),I
Output	RE	OUT	R,E
Store	RS	ST	R,D(B)
Store Character	RS	STC	R(N),D(B)
Store Character and Count	RSA	STCT	R(N),B
Store Halfword	RS	STH	R,D(B)
Subtract Character Register	RR	SCR	R1(N1),R2(N2)
Subtract Halfword Register	RR	SHR	R1,R2
Subtract Register	RR	SR	R1,R2
Subtract Register Immediate	RI	SRI	R(N),I
Test Register Under Mask	RI	TRM	R(N),I

Figure 4-2. Instruction Format

R1 Field: The R1 field in RR format instructions specifies the general register containing the first operand. For byte operations, the register specified by this field must be an odd-numbered register. For all other operations, any one of the eight general registers in the active group may be specified.

R2 Field: The R2 field in the RR format instructions specifies the general register containing the second operand. For byte operations, the register specified by this field must be an odd-numbered register. For all other operations, any one of the eight general registers in the active group may be specified.

N Field: Except for ARI, SRI, and BCT instructions, the N field in RS, RI, and RT format instructions specifies whether byte 0 (N=0) or byte 1 (N=1) of the register specified in the R field is to be treated as the eight-bit first operand. For ARI, SRI and BCT instructions, the N field specifies whether byte 0 (N=0), or both byte 0 and byte 1 (N=1) are to be treated as the operand.

Programming Note
With Extended Addressing, byte X is also part of the first operand in an ARI or SRI instruction.

N1 Field: Except for ACR and SCR instructions, the N1 field in RR format instructions specifies whether byte 0 (N1=0) or byte 1 (N1=1) of the register specified in the R1 field is to be treated as the eight-bit operand. For ACR and SCR instructions, the N1 field specifies whether byte 0 (N1=0), or both byte 0 and byte 1 (N1=1) are to be treated as the operand.

Programming Note
With Extended Addressing, byte X is also part of the first operand in an ACR or SCR instruction.

N2 Field: The N2 field in RR format instructions specifies whether byte 0 (N2=0) or byte 1 (N2=1) of the register specified in the R2 field is to be treated as the eight-bit operand.

M Field: The binary value of the three-bit M field in the Branch on Bit instruction (BB) specifies the bit (bit 0-7) to be tested in the byte operand selected by the R and N fields of the instruction.

Explicitly Addressed Operands in Storage

B Field: The B field in RS and RSA format instructions specifies a general register in the active group that contains a base address. The base address is used to address second operand locations in storage. For RS format instructions, the storage address is formed by the addition of the base address (contained in the register specified by the B field) and a positive displacement specified in the D field of the instruction.

For ICT and STCT (RSA format) instructions, the base address contained in the register specified by the B field is used without modification for the storage address.

For RS format instructions, if the 3-bit B field is zero, a fixed address constant is used for the base address instead of the contents of register 0. This permits direct access to system parameters at preassigned storage locations. The address constants for the various instructions are:

Instruction	*Address Constant*
IC and STC	X'0680'
LH and STH	X'0700'
L and ST	X'0780'

D Field: The D field in RS format instructions contains the displacement that is added to the base address to form the storage address of the second operand. The D field is treated as a positive binary number that represents a byte displacement for IC and STC instructions, a halfword displacement for LH and STH instructions, and a fullword displacement for L and ST instructions. The displacement ranges that can be specified are:

Instruction	*Displacement*
IC and STC	0 to 127 bytes
LH and STH	0 to 126 bytes in multiples of two
L and ST	0 to 124 bytes in multiples of four

T Field: The T field in the RT format instructions is treated as a signed binary number. The number represents a halfword displacement from the address in register 0 of the active group of registers. Before the RT format instructions are executed, register 0 is incremented to point to the next sequential instruction (as is done for all instructions). This means that the displacement is with respect to the address of the next sequential instruction after the branch instruction. The low-order bit of the T field (instruction bit 15) is used as the sign bit. When this bit is zero, the displacement is positive. If the bit is a one, the displacement is negative. Thus, the following displacement

ranges are allowed in the formation of the branch address:

Instruction	*T Field range in halfwords*	*Displacement from Branch instruction in halfwords*
BCL,BZL,B	+1023 to −1023	+1024 to −1022
BB, BCT	+63 to −63	+64 to −62

Condition Latches

A condition latch is a hardware latch that may be set or reset by instruction execution. Each of the five program levels has its own set of two condition latches. These condition latches are designated C and Z. The results of many instructions set the C and Z latches of the active group to 1 or 0. The states of these latches are described in the following instruction description sections. These condition latches can be inspected for decision making by Branch on C Latch (BCL) and Branch on Z Latch (BZL) instructions. A branch instruction never alters a condition latch.However, the program level 5 condition latches can be altered by executing an Output X'79' instruction. The state of these latches may be used as input via an Input X'79' instruction.

Programming Note

Since there is a separate set of C and Z condition latches for each of the five program levels, the state of the condition latches used by an interrupted program is not affected by other interrupting programs.

General Register Usage

Any register in the active group may be specified as containing an operand. However, in a byte operation, only the odd-numbered registers (that is, 1, 3, 5 and 7) in the active group may be specified as containing the byte operand. This is because only a two-bit field is allocated within the machine bit structure of the instruction to specify the register. Therefore, when the hardware decodes an instruction that contains a byte operation, a low-order one bit is added to access an odd-numbered register.

When a general register is specified for a halfword operation, byte 0 and byte 1 of the register are treated as a contiguous 16-bit binary operand. With Extended Addressing, byte X of the register is not used in a halfword operation and does not affect the setting of the condition latches.

When a general register is specified for an Extended Addressing operation, byte X, byte 0, and byte 1 of the register are treated as a contiguous 18 or 20-bit binary operand.

When a general register is specified for a single byte operand, either byte 0 or byte 1 of the register may be specified as the operand. The other bytes in the register do not affect the setting of the condition latches. For ARI, SRI, ACR, SCR, and BCT instructions, byte 0 or both byte 0 and byte 1 can be specified as the first operand in the general register to contain the result of the arithmetic operation. For example, for the Add Character Register (ACR) instruction, the operand in R2 is added to the operand in R1, and the result is placed in R1. Since R1 is to contain the result, byte 0 or both bytes 0 and 1 of R1 could be specified as an operand, whereas only a single byte (0 or 1) of R2 can be specified as an operand.

Programming Note

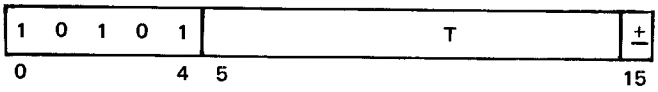
With Extended Addressing, byte X is included with the selected byte of the first operand in an ACR, ARI, SCR, or SRI instruction but does not affect the setting of the condition latches.

Instruction Descriptions

The following is a description of each of the 3704/3705 instructions.

BRANCH

B T [RT]



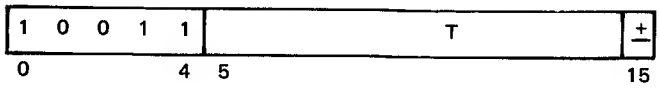
This instruction causes an unconditional branch to the branch address. The branch address is formed by adding the displacement value in the T field to the address of the next sequential instruction. Therefore, the branch address is always calculated relative to the next sequential instruction. The T field allows a displacement of +1023 to −1023 halfwords.

The low-order bit position (bit 15) of this instruction indicates whether the displacement is positive or negative. A 0 in bit 15 indicates that the displacement is in a positive direction, and a 1 indicates a negative direction.

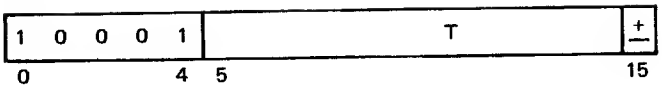
Resulting Condition Latches: Unchanged

BRANCH ON C LATCH
BRANCH ON Z LATCH

BCL T [RT]



BZL T [RT]



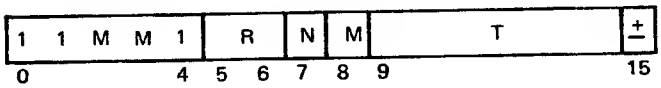
These instructions test the state of the C and Z condition latches associated with the active group of registers. If the tested latch is not set (0), the next sequential instruction is executed. If the tested latch is set (1), the next instruction to be executed is at the branch address. The branch address is formed by adding the displacement value in the T field to the address of next sequential instruction. Therefore, the branch address is always calculated relative to the next sequential instruction. The T field allows a displacement of +1023 to −1023 halfwords.

The low-order bit position (bit 15) of this instruction indicates whether the displacement is positive or negative. A 0 in bit 15 indicates that the displacement is in a positive direction, and a 1 indicates a negative direction.

Resulting Condition Latches: Unchanged

BRANCH ON BIT

BB R(N,M),T [RT]



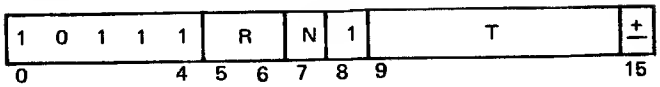
This instruction tests the state of a specified bit in a general register. If the bit tested is a zero, the next sequential instruction is executed. If the bit tested is a one, then the next instruction to be executed is at the branch address. The branch address is formed by adding the displacement value in the T field to the address of the next sequential instruction. Therefore, the branch address is always calculated relative to the next sequential instruction. The T field allows a displacement of −63 to +63 halfwords. The M field specifies which one of the eight bits of byte 0 (if N=0) or byte 1 (if N=1) of R is to be tested. The register specified by R must be an odd-numbered register.

The low-order bit position (bit 15) of this instruction indicates whether the displacement is positive or negative. A 0 in bit 15 indicates that the displacement is in a positive direction, and a 1 indicates a negative direction.

Resulting Condition Latches: Unchanged

BRANCH ON COUNT

BCT R(N),T [RT]



The count value in the register specified by R is decremented by one and then tested for zero. If the result is zero, the next sequential instruction is executed. If the result is nonzero, the next instruction to be executed is at the branch address. The count is contained in byte 0 (if N=0) or in both bytes 0 and 1 (if N=1) of the register. The branch address is formed by adding the displacement value in the T field to the address of the next sequential instruction. Therefore, the branch address is always calculated relative to the next sequential instruction. The T field allows for a displacement of −63 to +63 halfwords. The register specified by R must be an odd-numbered register.

The low-order bit position (bit 15) of this instruction indicates whether the displacement is positive or negative. A 0 in bit 15 indicates that the displacement is in a positive direction, and a 1 indicates a negative direction.

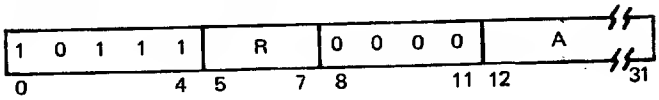
Resulting Condition Latches: Unchanged

Programming Note

If, before execution of this instruction, the count value (byte 0 or bytes 0 and 1) in the register is zero, the effective count value is 256 or 65,536, respectively.

BRANCH AND LINK

BAL R,A [RA]



This instruction is a 32-bit instruction that causes an unconditional branch. The address of the next sequential instruction is stored as link information in the register specified by R. Subsequently, the instruction address in register 0 is replaced by the branch address (address contained in the A field), and the branch is executed.

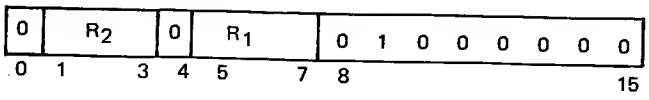
Resulting Condition Latches: Unchanged

Programming Notes

1. Since register 0 is the IAR, no linkage is provided if it is specified in the R field.
2. Bits 12, 13, 14, and 15 in the A field are used only with Extended Addressing.

BRANCH AND LINK REGISTER

BALR R1,R2 [RR]



The address of the next sequential instruction is stored as link information in the register specified by R1. Subsequently, the instruction address in register 0 is replaced by the branch address (address in the register specified by R2), and the branch is executed. The branch address is obtained from R2 before the link information is stored in R1.

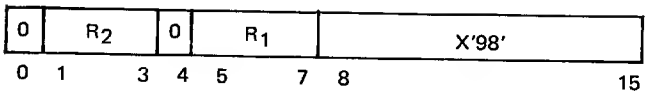
Resulting Condition Latches: Unchanged

Programming Note

Since register 0 is the IAR, no linkage is provided if it is specified in the R1 field, and no branch occurs if it is specified in the R2 field.

ADD REGISTER

AR R1,R2 [RR]



The second operand (R2) is added to the first operand (R1), and the sum is placed in the first operand location. Addition of all bits in the register operands is performed logically without regard to a sign, and the appropriate condition latches are set.

Resulting Condition Latches:

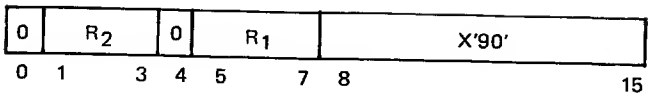
C An overflow occurred from R1
Z The result in R1 = 0

Programming Notes

1. If register 0 is specified by R1, a branch to the address formed in register 0 results, and the condition latches remain unchanged.
2. With Extended Addressing, this instruction operates on all 18 or 20 bit positions (bytes X, 0, and 1) of the registers. Without Extended Addressing, operation is the same as for the Add Halfword Register instruction.

ADD HALFWORD REGISTER

AHR R1,R2 [RR]



The second operand (R2, bytes 0 and 1) is added to the first operand (R1, bytes 0 and 1), and the sum is placed in the first operand location. Addition of the register operands is performed logically without regard to a sign, and the appropriate condition latches are set.

Resulting Condition Latches:

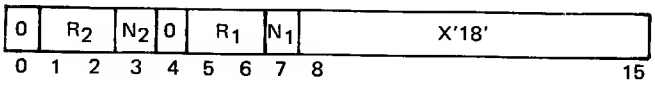
C An overflow occurred from byte 0 of R1
Z The result in bytes 0 and 1 of R1 = 0

Programming Note

If register 0 is specified as R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.

ADD CHARACTER REGISTER

ACR R1(N1),R2(N2) [RR]



The second operand (R2, byte 0 if N2=0 or byte 1 if N2=1) is added to the first operand (R1, byte 0 if N1=0 or bytes 0 and 1 if N1=1). The sum is placed in the first operand location. If N1 = 0, byte 1 of R1 remains unchanged. The registers specified by R1 and R2 must be odd-numbered registers.

Resulting Condition Latches:

N1 = 0
C An overflow occurred from byte 0 of R1
Z The result in byte 0 of R1 = 0

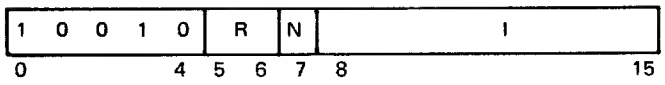
N1 = 1
C An overflow occurred from bytes 0 and 1 of R1
Z The result in bytes 0 and 1 of R1 = 0

Programming Note

With Extended Addressing, the first operand includes byte X of the register specified by R1. However, byte X does not affect the setting of the condition latches.

ADD REGISTER IMMEDIATE

ARI R(N),I [RI]



The second operand (I field) is added to the first operand (byte 0 if N=0 or bytes 0 and 1 if N=1 of the register specified by R). The sum is then placed in the first operand location. The register specified by R must be an odd-numbered register. If N=0, byte 1 of R remains unchanged.

Resulting Condition Latches:

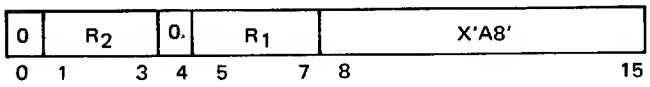
N = 0
C An overflow occurred from byte 0 of R
Z The result in byte 0 of R = 0

N = 1
C An overflow occurred from bytes 0 and 1 of R
Z The result in bytes 0 and 1 of R = 0

Programming Note
With Extended Addressing, the first operand includes byte X of the register specified by R. However, byte X does not affect the setting of the condition latches.

SUBTRACT REGISTER

SR R1,R2 [RR]



The second operand (R2) is subtracted from the first operand (R1), and the result is placed in the first operand location.

Subtraction is performed by adding the two's complement of the second operand to the first operand and setting the appropriate condition latch. If the difference is less than zero, the result is in the two's complement form.

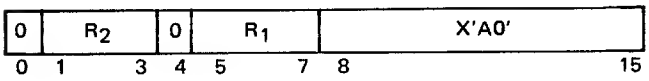
Resulting Condition Latches:

C The result in R1 < 0
Z The result in R1 = 0

Programming Notes
1. If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.
2. With Extended Addressing, this instruction operates on all 18 or 20 bit positions (bytes X, 0, and 1) of the registers. Without Extended Addressing, the operation is the same as for the Subtract Halfword Register instruction.

SUBTRACT HALFWORD REGISTER

SHR R1,R2 [RR]



The second operand (R2, bytes 0 and 1) is subtracted from the first operand (R1, bytes 0 and 1), and the result is placed in the first operand location.

Subtraction is performed by adding the two's complement of the second operand to the first operand and setting the appropriate condition latch. If the difference is less than zero, the result is in the two's complement form.

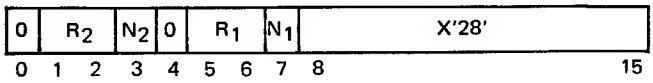
Resulting Condition Latches:

C The result in bytes 0 and 1 of R1 < 0
Z The result in bytes 0 and 1 of R1 = 0

Programming Note
If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.

SUBTRACT CHARACTER REGISTER

SCR R1(N1),R2(N2) [RR]



The second operand (R2, byte 0 if N2=0 or byte 1 if N2=1) is subtracted from the first operand (R1, byte 0 if N1=0 or bytes 0 and 1 if N1=1). The result is placed into the first operand location. The registers specified by R1 and R2 must be odd-numbered registers.

Before the subtraction is performed, the second operand is expanded with high-order zeros to equal the size of the first operand. Subtraction is performed by adding the two's complement of the second operand to the first operand and setting the appropriate condition latch. If the difference is less than zero, the result is in the two's complement form.

Resulting Condition Latches:

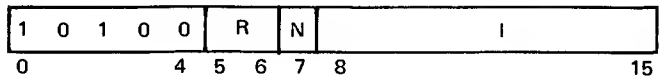
N1 = 0
C The result in byte 0 of R1 < 0
Z The result in byte 0 of R1 = 0

N1 = 1
C The result in bytes 0 and 1 of R1 < 0
Z The result in bytes 0 and 1 of R1 = 0

Programming Note
With Extended Addressing, the first operand includes byte X of the register specified by R1. However, byte X does not affect the setting of the condition latches.

SUBTRACT REGISTER IMMEDIATE

SRI R(N),I [RI]



The second operand (I field) is subtracted from the first operand (byte 0 if N=0 or bytes 0 and 1 if N=1 of the register specified by R). The result is placed in the first operand location. The register specified by R must be an odd-numbered register.

Before the subtraction is performed, the second operand is expanded with high-order zeros to equal the size of the first operand. Subtraction is performed by adding the two's complement of the second operand to the first operand and setting the appropriate condition latch. If the difference is less than zero, the result is in the two's complement form.

Resulting Condition Latches:

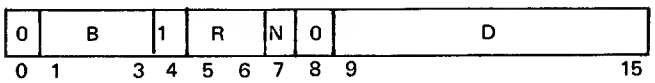
N = 0
C The result in byte 0 of R < 0
Z The result in byte 0 of R = 0

N = 1
C The result in bytes 0 and 1 of R < 0
Z The result in bytes 0 and 1 of R = 0

Programming Note
With Extended Addressing, the first operand includes byte X of the register specified by R. However, byte X does not affect the setting of the condition latches.

INSERT CHARACTER

IC R(N),D(B) [RS]



The eight-bit character at the second operand address is placed into byte 0 (if N=0) or byte 1 (if N=1) of the register specified by R. The remaining bits of the register are unchanged. The storage address of the second operand is formed by adding the displacement value in the D field to the contents of the base register specified by the B field. The D field allows for a displacement of 0 to +127 bytes. The register specified by R must be an odd-numbered register.

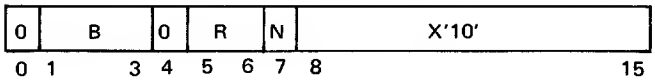
Resulting Condition Latches:

C The selected byte of R contains an even number of 1 bits or R = 0
Z The selected byte of R = 0

Programming Note
If the B field is 0, address X'0680' is used as the base address instead of the contents of register 0. This permits direct addressing of the 128 bytes starting at address X'0680' without having to load a base register.

INSERT CHARACTER and COUNT

ICT R(N),B [RSA]



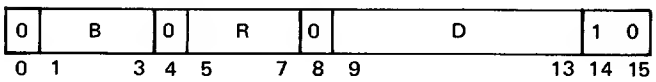
The eight-bit character at the second operand address is placed into byte 0 (if N=0) or byte 1 (if N=1) of the register specified by R. After the storage address has been obtained from the base register (B), the contents of the base register are incremented by 1.Therefore, after the execution of this instruction, the register specified by the B field normally contains an address one byte greater than before execution. (See note 2 below.) The register specified by R must be an odd-numbered register.

Resulting Condition Latches: Unchanged

Programming Notes
1. Register 0 should not normally be specified in the B field, because it contains the instruction address.
2. If R and B specify the same (odd) register, its contents are incremented by one before the character is inserted into the selected byte of the register.

LOAD

L R,D(B) [RS]



This instruction loads the data (second operand) from a four-byte field in storage into the first operand (register specified by R). The four-byte field containing the second operand must be on a halfword boundary. Since the general registers are not a fullword (32 bits) in length, only the low-order bits of that storage location are used. (See note 4 below.) The storage address is formed by adding the displacement value in the D field to the contents of the base register specified by B. The D field allows for a displacement of 0 to 124 bytes in multiples of 4 (31 fullwords).

Resulting Condition Latches:

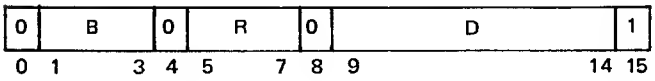
C The result in R ≠ 0
Z The result in R = 0

Programming Notes

1. The low-order bit of the storage address is ignored since storage is addressed on halfword boundaries with this instruction.
2. If register 0 (IAR) is specified in the R field, this instruction results in an unconditional branch to the address loaded in register 0, and the condition latches remain unchanged.
3. If the B field is 0, address X'0780' is used as the base address instead of the contents of register 0. This permits direct addressing of the 32 fullwords starting at address X'0780' without having to load a base register.
4. With Extended Addressing, this instruction loads the 18 or 20 low-order bits from the four-byte field addressed by the second operand into bytes X, 0, and 1 of R. The 12 or 14 high-order bits in storage are ignored. Without Extended Addressing, the low-order 16 bits of the addressed four-byte field are loaded into bytes 0 and 1 of R, and the 16 high-order bits in storage are ignored.

LOAD HALFWORD

LH R,D(B) [RS]



This instruction loads a halfword from storage into bytes 0 and 1 of the register specified by R. The storage address is formed by adding the displacement value in the D field to the contents of the base register (B). The D field allows for a displacement of 0 to 126 bytes in multiples of 2 (63 halfwords).

Resulting Condition Latches:

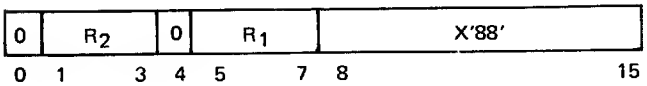
C The result in bytes 0 and 1 of R ≠ 0
Z The result in bytes 0 and 1 of R = 0

Programming Notes

1. For all Load Halfword instructions, the halfword obtained from storage is loaded into both the specified general register and the old-CRC register. See *Cyclic Redundancy Check* in Chapter 5. For normal operations (non-CRC), the loading of data into the old-CRC register serves no function.
2. The low-order bit of the storage address is ignored since storage is addressed on halfword boundaries with this instruction.
3. If register 0 (IAR) is specified in the R field, this instruction results in an unconditional branch to the address formed in register 0, and the condition latches remain unchanged.
4. If the B field is 0, address X'0700' is used as the base address instead of the contents of register 0. This permits direct addressing of the 64 halfwords starting at address X'0700' without having to load a base register.
5. With Extended Addressing, byte X of the register specified by R is set to zero during the load operation.

LOAD REGISTER

LR R1,R2 [RR]



The second operand (R2) is loaded into the first operand (R1). All bits of the register specified by R2 are moved into the register specified by R1 and are not changed. Condition latches are set according to the result in the first operand.

Resulting Condition Latches:

C The result in R1 ≠ 0
Z The result in R1 = 0

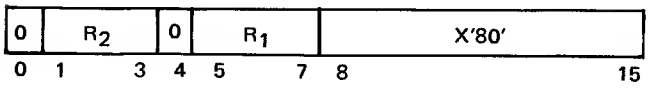
Programming Notes

1. If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.
2. With Extended Addressing, this instruction operates on all 18 or 20 bit positions (bytes X, 0, and 1) of the registers. Without Extended Addressing, operation

is the same as for the Load Halfword Register instruction.

LOAD HALFWORD REGISTER

LHR R1,R2 [RR]



The second operand (R2, bytes 0 and 1) is loaded into the first operand (R1, bytes 0 and 1). The second operand is not changed, and the condition latches are set according to the result of the first operand.

Resulting Condition Latches:

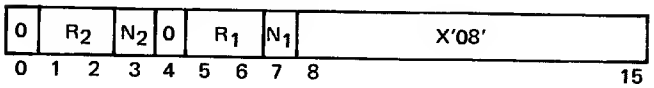
C The result in bytes 0 and 1 of R1 ≠ 0
Z The result in bytes 0 and 1 of R1 = 0

Programming Note

If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.

LOAD CHARACTER REGISTER

LCR R1(N1),R2(N2) [RR]



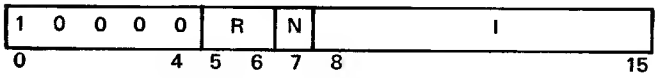
The second operand (R2, byte 0 if N2=0 or byte 1 if N2=1) is loaded into the first operand (R1, byte 0 if N1=0 or byte 1 if N1=1). The registers specified by R1 and R2 must be odd-numbered registers.

Resulting Condition Latches:

C The selected byte of R1 contains an even number of 1 bits or R1 = 0
Z The selected byte of R1 = 0

LOAD REGISTER IMMEDIATE

LRI R(N),I [RI]



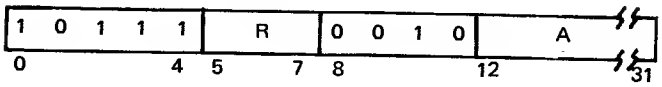
The second operand (I field) is loaded into the first operand (byte 0 if N=0 or byte 1 if N=1 of the register specified by R). The non-selected byte(s) of the register remain unchanged. The register specified by R must be an odd-numbered register.

Resulting Condition Latches:

C The result in the selected byte of R ≠ 0
Z The result in the selected byte of R = 0

LOAD ADDRESS

LA R,A [RA]



This instruction is a 32-bit instruction. The second operand (A field) is treated as an immediate operand and is loaded into the first operand (R).

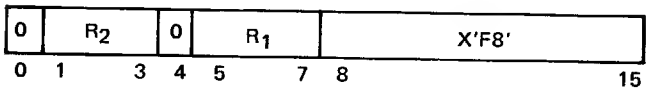
Resulting Condition Latches: Unchanged

Programming Notes

1. With Extended Addressing instruction bits 12, 13, 14, and 15 in the A field are loaded into byte X of R. Without Extended Addressing, these bits are ignored.
2. If register 0 is specified by R, a branch results to the address contained in the A field.

LOAD with OFFSET REGISTER

LOR R1,R2 [RR]



The second operand (R2) is shifted right one bit position, and the result is loaded into the first operand (R1). A zero bit is inserted in the high-order bit position of R1.

Resulting Condition Latches:

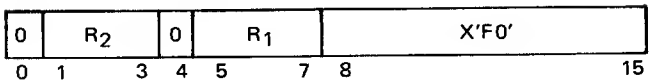
C A 1 bit shifted out of byte 1, bit 7
Z The result in R1 = 0

Programming Notes

1. If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.
2. With Extended Addressing, this instruction operates on all 18 or 20 bit positions (bytes X, 0, and 1) of the registers. Without Extended Addressing, the operation is the same as the Load Halfword with Offset Register instruction.

LOAD HALFWORD with OFFSET REGISTER

LHOR R1,R2 [RR]



The second operand (R2, bytes 0 and 1) is shifted right one bit position, and the result is loaded into the first operand (R1, bytes 0 and 1). A zero bit is inserted into the high-order bit position of R1, byte 0.

Resulting Condition Latches:

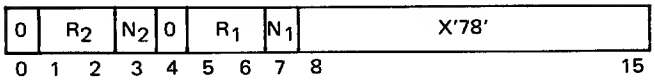
C A 1 bit shifted out of byte 1, bit 7
Z The result in bytes 0 and 1 of R1 = 0

Programming Note

If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.

LOAD CHARACTER with OFFSET REGISTER

LCOR R1(N1),R2(N2) [RR)



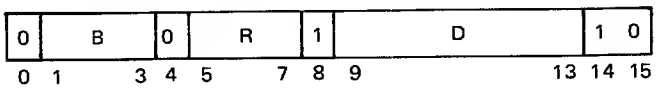
The second operand (R2, byte 0 if N2=0 or byte 1 if N2=1) is shifted right one bit position, and the result is loaded into the first operand (R1, byte 0 if N=0 or byte 1 if N=1). A zero bit is inserted into the high-order bit position of the selected byte of R1. The non-selected byte(s) of R1 remain unchanged. The registers specified by R1 and R2 must be odd-numbered registers.

Resulting Condition Latches:

C A 1 bit shifted out of the selected byte
Z The result in the selected byte of R1 = 0

STORE

ST R,D(B) [RS]



This instruction stores the contents of the first operand (the register specified by R) into the second operand in storage. The address of the second operand must be on a halfword boundary. Since the general registers are not a fullword (32 bits) in length, only the low-order bits of the four-byte field in storage will be affected. (See note 5 below.) The storage address is formed by adding the displacement contained in the D field to the contents of the base register specified by the B field. The D field allows for a displacement of 0 to 124 bytes in multiples of 4 (31 fullwords).

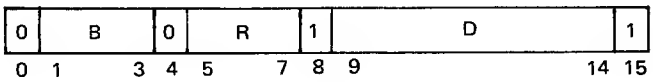
Resulting Condition Latches: Unchanged

Programming Notes

1. The low-order bit of the storage address is ignored because storage is addressed on halfword boundaries with this instruction.
2. If the B field is 0, address X'0780' is used as the base address instead of the contents of register 0. This permits direct addressing of the 32 fullwords starting at address X'0780' without having to load a base register.
3. If the R field is 0, zeros are stored, instead of the contents of register 0 (with the exception of note 4 below).
4. A Store instruction must be located at storage location X'0010' so that when a program level 1 interrupt occurs, this instruction is the first to be executed at that level. The normal function of the store instruction is modified in this special case to permit storing the contents of register 0. See the programming note under *Program Levels* in Chapter 2.
5. With Extended Addressing, the contents of the register (bytes X, 0, and 1) are stored into the low-order 18 or 20 bits of the four-byte field addressed in storage. The 12 or 14 high order bits remain unchanged. Without Extended Addressing, bytes 0 and 1 of the register are stored into the low-order 16 bits of the four-byte field in storage, and the 16 high-order bits remain unchanged.

STORE HALFWORD

STH R,D(B) [RS]



This instruction stores bytes 0 and 1 of the register specified by R into the second operand in storage. The storage address of the second operand is formed by adding the displacement value in the D field to the contents of the base register specified by B. The D field allows for a displacement of 0 to 126 bytes in multiples of 2 (63 halfwords).

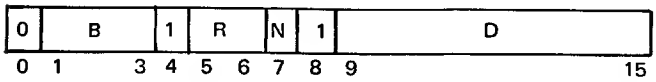
Resulting Condition Latches: Unchanged

Programming Notes

1. The low-order bit of the storage address is ignored because storage is addressed on halfword boundaries with this instruction.
2. If the R field is zero, X'0000' is stored at the storage address instead of the contents of register 0.
3. If the B field is 0, address X'0700' is used as the base address instead of the contents of register 0. This permits direct addressing of the 64 halfwords starting at address X'0700' without having to load a base register.

STORE CHARACTER

STC R(N),D(B) [RS]



The first operand (byte 0 if N=0 or byte 1 if N=1 of the register specified by R) is stored into the second operand in storage. The storage address of the second operand is formed by adding the displacement value specified by the D field to the contents of the base register specified by B. The D field allows for a displacement of 0 to 127 bytes. The register specified by R must be an odd-numbered register.

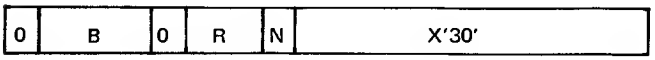
Resulting Condition Latches: Unchanged

Programming Note

If the B field is 0, address X'0680' is used as the base address instead of the contents of register 0. This permits direct addressing of the 128 bytes starting at address X'0680' without having to load a base register.

STORE CHARACTER and COUNT

STCT R(N),B [RSA]



The first operand is placed in the second operand in storage. The storage address of the second operand is contained in the register specified by the B field. The byte stored is byte 0 (if N=0) or byte 1 (if N=1) of the register specified by R. After the storage address has been obtained from the base register (B field), the contents of the register are incremented by 1.Therefore, at the completion of the execution of this instruction, the base register contains an address one byte greater than before execution. The register specified by R must be an odd-numbered register.

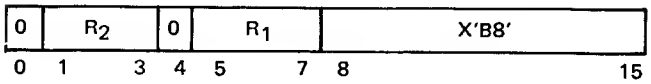
Resulting Condition Latches: Unchanged

Programming Notes

1. Register 0 should not normally be specified in the B field, because it contains the instruction address.
2. If R and B specify the same (odd) register, its contents are incremented by one before the selected byte of that register is stored.

COMPARE REGISTER

CR R1,R2 [RR]



The second operand (R2) is compared to the first operand (R1), and the result sets the appropriate condition latch. This instruction performs a logical compare without regard to a sign bit. All bits of each operand participate in the comparison. The contents of the registers are not changed.

Resulting Condition Latches:

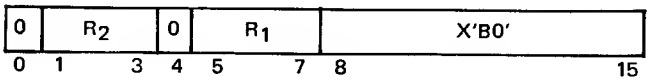
C Value in R1 < value in R2
Z Value in R1 = value in R2

Programming Note

With Extended Addressing, this instruction operates on all 18 or 20 bit positions (bytes X, 0, and 1) of the registers. Without Extended Addressing, operation is the same as the Compare Halfword Register instruction.

COMPARE HALFWORD REGISTER

CHR R1,R2 [RR]



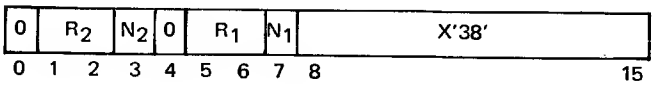
The second operand (R2, bytes 0 and 1) is compared to the first operand (R1, bytes 0 and 1), and the result sets the appropriate condition latch. This instruction performs a logical compare without regard to a sign bit. All bits of each operand participate in the comparison. The contents of the registers are not changed.

Resulting Condition Latches:

C Bytes 0 and 1 of R1 < bytes 0 and 1 of R2
Z Bytes 0 and 1 of R1 = bytes 0 and 1 of R2

COMPARE CHARACTER REGISTER

CCR R1(N1),R2(N2) [RR]



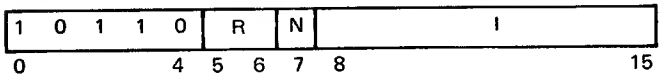
The second operand (R2, byte 0 if N2=0 or byte 1 if N2=1), is compared with the first operand (R1, byte 0 if N1=0 or byte 1 if N1=1), and the appropriate condition latch is set. This instruction performs a logical compare without regard to a sign bit. All bits of each operand participate in the comparison. The registers specified by R1 and R2 must be odd-numbered registers. The contents of the registers are not changed.

Resulting Condition Latches:

C The selected byte of R1 < the selected byte of R2
Z The selected byte of R1 = the selected byte of R2

COMPARE REGISTER IMMEDIATE

CRI R(N),I [RI]



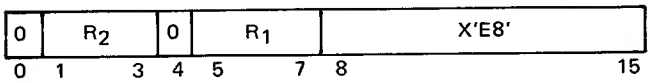
The second operand (I field) is compared with the first operand (byte 0 if N=0 or byte 1 if N=1 of the register specified by R), and the appropriate condition latch is set. This instruction performs a logical compare without regard to a sign bit. All bits of each operand participate in the comparison. The register specified by R must be an odd-numbered register, and its contents are not changed.

Resulting Condition Latches:

C The value in the selected byte of R < I
Z The value in the selected byte of R = I

AND REGISTER

NR R1,R2 [RR]



The second operand (R2) is ANDed with the first operand (R1), and the result is placed in the first operand location.

Operands are treated as unstructured logical quantities, and the connective AND is applied bit by bit. A bit position in the result is set to one if the corresponding bit positions in both operands contain a one; otherwise, the result bit is set to zero. All bits of each operand participate in the operation. Any value in the operands or result is valid.

Resulting Condition Latches:

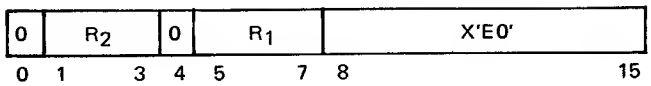
C The result in R1 ≠ 0
Z The result in R1 = 0

Programming Notes

1. If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.
2. With Extended Addressing, this instruction operates on all 18 or 20 bit positions (bytes X, 0, and 1) of the registers. Without Extended Addressing, the operation is the same as for the And Halfword Register instruction.

AND HALFWORD REGISTER

NHR R1,R2 [RR]



The second operand (R2, bytes 0 and 1) is ANDed with first operand (R1, bytes 0 and 1), and the result is placed in the first operand location.

The operation is performed in the same manner as the AND Register instruction except that only the low-order 16 bits (bytes 0 and 1) of the registers are used.

Resulting Condition Latches:

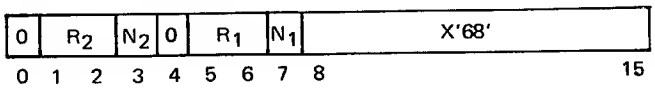
C The result in bytes 0 and 1 of R1 ≠ 0
Z The result in bytes 0 and 1 of R1 = 0

Programming Note

If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.

AND CHARACTER REGISTER

NCR R1(N1),R2(N2) [RR]



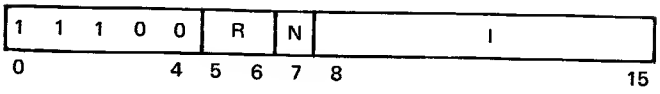
The second operand (R2, byte 0 if N2=0 or byte 1 if N2=1) is ANDed with the first operand (R1, byte 0 if N1=0 or byte 1 if N1=1). The operation is performed in the same manner as the AND Register instruction, and the result is placed in the first operand location. The registers specified by R1 and R2 must be odd-numbered registers. The nonselected byte(s) of R1 remain unchanged.

Resulting Condition Latches:

C The result in the selected byte of R1 ≠ 0
Z The result in the selected byte of R1 = 0

AND REGISTER IMMEDIATE

NRI R(N),I [RI]



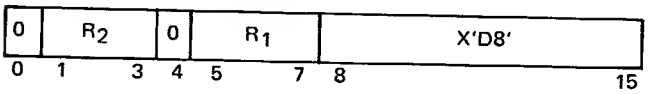
The second operand (I field) is ANDed with the first operand (byte 0 if N=0 or byte 1 if N=1 of the register specified by R). The result is placed into the first operand location with the remaining byte(s) of the register unchanged. The operation is performed in the same manner as the AND Register instruction. The register specified by R must be an odd-numbered register.

Resulting Condition Latches:

C The result in the selected byte of R ≠ 0
Z The result in the selected byte of R = 0

OR REGISTER

OR R1,R2 [RR]



The second operand (R2) is ORed with the first operand (R1), and the result is placed in the first operand location. All bits of each operand participate in the operation.

Operands are treated as unstructured logical quantities, and the connective inclusive OR is applied bit by bit. A bit position in the result is set to one if the corresponding bit position in either one or both of the operands contains a one. Otherwise, the result bit is set to zero. Any value in the operands or result is valid.

Resulting Condition Latches:

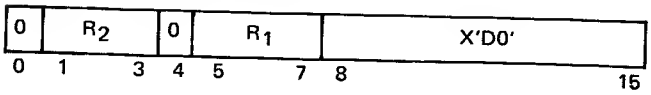
C The result in R1 ≠ 0
Z The result in R1 = 0

Programming Notes

1. If register 0 is specified by R1, a branch to the address formed in register 0 results, and the condition latches remain unchanged.
2. With Extended Addressing, this instruction operates on all 18 or 20 bit positions (bytes X, 0, and 1) of the registers. Without Extended Addressing, the operation is the same as the Or Halfword Register instruction.

OR HALFWORD REGISTER

OHR R1,R2 [RR]



The second operand (R2, bytes 0 and 1) is ORed with the first operand (R1, bytes 0 and 1), and the result is placed in the first operand location.

The operation is performed in the same manner as the OR Register instruction with the exception that only the low-order 16 bits (bytes 0 and 1) of the registers are used.

Resulting Condition Latches:

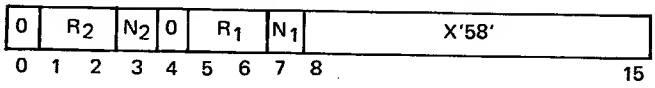
C The result in bytes 0 and 1 of R1 ≠ 0
Z The result in bytes 0 and 1 of R1 = 0

Programming Note

If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.

OR CHARACTER REGISTER

OCR R1(N1),R2(N2) [RR]



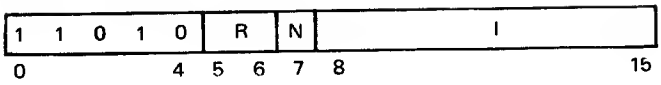
The second operand (R2, byte 0 if N2=0 or byte 1 if N2=1) is ORed with the first operand (R1, byte 0 if N1=0 or byte 1 if N1=1). The operation is performed in the same manner as the OR Register instruction, and the result is placed in the first operand location. The registers specified by R1 and R2 must be odd-numbered registers. The nonselected byte(s) of R1 remain unchanged.

Resulting Condition Latches:

C The result in the selected byte of R1 ≠ 0
Z The result in the selected byte of R1 = 0

OR REGISTER IMMEDIATE

ORI R(N),I [RI]



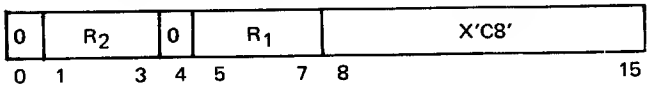
The second operand (I field) is ORed with the first operand (byte 0 if N=0 or byte 1 if N=1 of the register specified by R). The result is placed into the first operand location with the remaining byte(s) of R unchanged. The operation is performed in the same manner as the OR Register instruction. The register specified by R must be an odd-numbered register.

Resulting Condition Latches:

C The result in the selected byte of R ≠ 0
Z The result in the selected byte of R = 0

EXCLUSIVE OR REGISTER

XR R1,R2 [RR]



The second operand (R2) is exclusive ORed with the first operand (R1), and the result is placed in the first operand location. All bits of each operand participate in the operation.

Operands are treated as unstructured logical quantities, and the connective exclusive OR is applied bit by bit. A bit position in the result is set to one if the corresponding bit positions in the two operands are unlike; otherwise, the resulting bit is set to zero.

Resulting Condition Latches:

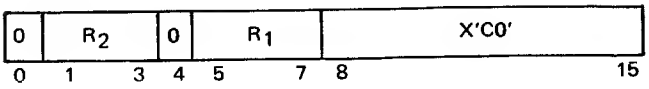
C The result in R1 ≠ 0
Z The result in R1 = 0

Programming Notes

1. If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.
2. With Extended Addressing, this instruction operates on all 18 or 20 bit positions (bytes X, 0, and 1) of the registers. Without Extended Addressing, the operation is the same as the Exclusive OR Halfword Register instruction.

EXCLUSIVE OR HALFWORD REGISTER

XHR R1,R2 [RR]



The second operand (R2, bytes 0 and 1) is exclusive ORed with the first operand (R1, bytes 0 and 1), and the result is placed in the first operand location.

The operation is performed in the same manner as the Exclusive OR Register instruction except that only the low-order 16 bits (bytes 0 and 1) of the registers are used.

Resulting Condition Latches:

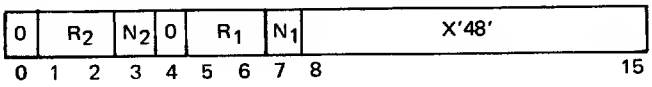
C The result in bytes 0 and 1 of R1 ≠ 0
Z The result in bytes 0 and 1 of R1 = 0

Programming Note

If register 0 is specified by R1, a branch results to the address formed in register 0, and the condition latches remain unchanged.

EXCLUSIVE OR CHARACTER REGISTER

XCR R1(N1),R2(N2) [RR]



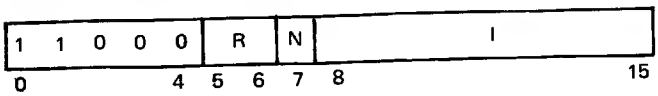
The second operand (R2, byte 0 if N1=0 or byte 1 if N2=1) is exclusive ORed with the first operand (R1, byte 0 if N1=0 or byte 1 if N1=1). The result is placed in the first operand location, and the appropriate condition latch is set. The operation is performed in the same manner as the Exclusive OR Register instruction. The registers specified by R1 and R2 must be odd-numbered registers.

Resulting Condition Latches:

C The result in the selected byte of R1 ≠ 0
Z The result in the selected byte of R1 = 0

EXCLUSIVE OR REGISTER IMMEDIATE

XRI R(N),I [RI]



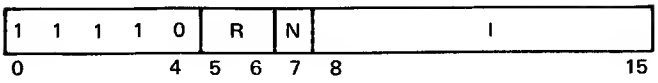
The second operand (I field) is exclusive ORed with the first operand (byte 0 if N=0 or byte 1 if N=1 of the register specified by R). The resulting byte is placed in the first operand location, and the appropriate condition latch is set. The operation is performed in the same manner as the Exclusive OR Register instruction. The register specified by R must be an odd-numbered register.

Resulting Condition Latches:

C The result in the selected byte of R ≠ 0
Z The result in the selected byte of R = 0

TEST REGISTER UNDER MASK

TRM R(N),I [RI]



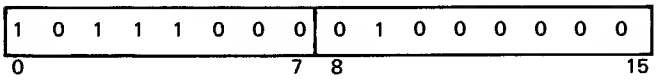
The state of the first operand bits selected by a mask is used to set the appropriate condition latch. The byte of immediate data (I field) is used as an eight-bit mask. The bits of the mask are made to correspond one for one with the bits of the first operand (byte 0 if N=0 or byte 1 if N=1 of the register specified by R). A mask bit of one indicates that the register bit is to be tested. When the mask bit is zero, the register bit is ignored. Testing is done by ANDing the selected byte of the register with the immediate operand. The contents of R are not altered. The register specified by R must be an odd-numbered register.

Resulting Condition Latches:

C The result ≠ 0
Z The result = 0

EXIT

EXIT [EXIT]



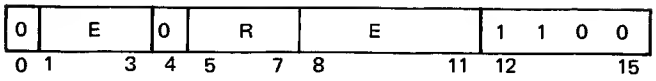
The Exit instruction is used to exit from the active program level. The interrupt-priority logic then determines which group of general registers to select as the active group for the next program operation. If executed at program level 5, the level 4 supervisor call interrupt request (SVC L4) is set. Then the next instruction executed is normally the instruction at the starting address for program level 4. However, if other interrupt requests are present, the next instruction executed is the instruction at the starting address of the highest priority program level requesting an interrupt.

This instruction also resets the 'interrupt entered' latch for the program level that executes it.

Resulting Condition Latches: Unchanged

INPUT

IN R,E [RE]



This instruction loads the register specified by R with the contents of one of 128 input-addressable external registers, specified by the E field. Throughout this text the input instructions are referred to in the form: Input X'*nn*' where *nn* is the hexadecimal address of the external register. Appendix A shows the hexadecimal addresses of the external registers. The 32 general registers can also be addressed as external registers. Appendixes B and C show the bit definitions for the external registers.

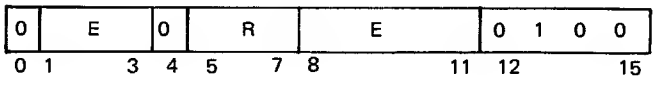
Resulting Condition Latches: Unchanged

Programming Notes

1. If register 0 is specified by R, this instruction results in a branch to the address formed in register 0.
2. This instruction is a *privileged* instruction executable only at program levels 1, 2, 3 or 4. Any attempt to execute this instruction at program level 5 causes the level 1 input/output check interrupt request (In/Out Check L1) to be set.
3. The input/output check request is set when the instruction is executed at program level 1, 2, 3, or 4 if the external register address either is not assigned or is not recognized by any adapter or the CCU.
4. The input/output check request is set if incorrect parity is detected on the CCU inbus when an input instruction is executed. This can occur for some input instructions if they are executed at an improper time. See the individual input instruction descriptions for details.
5. With Extended Addressing, byte X of the register specified by R is set to zeros with the following exceptions: (1) the E field is X'00' through X'1F' (signifying a general register), (2) the E field is X'74' (lagging address register), or (3) the E field is X'71' (panel address/data entry digits).

OUTPUT

OUT R,E [RE]



This instruction loads one of 128 output-addressable external registers specified by the E field with the contents of the register specified by R. Throughout this text the output instructions are referred to in the form: Output X'*nn*', where *nn* is the hexadecimal address of the external register. Appendix A shows the hexadecimal addresses of the external registers. The 32 general registers can also be addressed as external registers. Appendixes B and C show the bit definitions for the external registers.

Resulting Condition Latches: Unchanged

Programming Notes

1. If register 0 of the active group of general registers is addressed as the external register, this instruction results in a branch to the address formed in register 0.
2. This instruction is a *privileged* instruction executable at program levels 1, 2, 3 or 4 only. Any attempt to execute this instruction at program level 5 causes the level 1 input/output check interrupt request (In/Out Check L1) to be set.
3. The input/output check request is set when this instruction is executed at program levels 1, 2, 3 or 4 and if the external register address either is not assigned or is not recognized by the CCU or any adapter.
4. If the R field is 0, and an external register from X'00' through X'1F' is specified in the E field, the parity bits of the external register are regenerated, but the data is not changed.
5. If any output instruction is executed at program levels 1, 2, 3, or 4, the output also causes the CRC data register in the CCU to be loaded with the contents of byte 1 of the register specified by R. See *Cyclic Redundancy Check* in Chapter 5.
6. With Extended Addressing, byte X of the register specified by R is ignored with the following exceptions: (1) the E field specifies an external register from X'00' through X'1F' (signifying a general register) or (2) the E field is X'71' or X'72' (display register 1 or 2).

Chapter 5: Central Control Unit

This chapter is intended to give the reader a basic understanding of the operation of the Central Control Unit and the requirements necessary to program its operation.

The Central Control Unit (CCU) contains the circuits and data flow paths needed (1) to execute the instruction set, (2) to address storage, (3) to perform arithmetic and logical processing of data, and (4) to control the attached adapters. Operation of the CCU is under control of the programs in storage.

The data flow in the CCU is of a general hardware nature. Data flow for a particular operation is determined by the instruction, cycle steal, or control operation being executed.

CCU Registers

The CCU contains the 32 general registers used by the control program for instruction execution and data handling. It also contains various hardware registers that are used to store and pass information essential to the controller operation. Some of these hardware registers are available to the control program as external register addresses through the use of input and output instructions. These registers are described in the following paragraphs.

CRC Register

When an Input X'7B' or X'7C' instruction is executed, this register is loaded with the new Cyclic Redundancy Check character and is loaded into the general register specified by the input instruction. The contents of the general register is a current CRC character that is the combination of the old-CRC register and the CRC data register. See the *Cyclic Redundancy Check* section of this chapter for a complete description of its use.

CRC Data Register

The CRC Data register is loaded with the next data character to be included in the calculation of a Cyclic Redundancy Check character. The contents of this register are then combined (by hardware) with the contents of the old-CRC register to form the new CRC character. See the *Cyclic Redundancy Check* section of this chapter for a complete description of its use.

Display Register 1 (DR1)

Display Register 1 is used as temporary storage for data to be displayed in the Display A lights on the control panel. The register is displayed on a 3705 whenever the Display/Function Select switch is in the STORAGE ADDRESS, REGISTER ADDRESS, or any of the FUNCTION 1-6 positions. On a 3704, the Display Register 1 and 2 push button must be active. This register can be loaded by pressing the Store or Set Address/Display push button on the control panel; or it can be loaded with data by executing an Output X'71' instruction. See the 3704 or 3705 *Control Panel Guide* for information on the operations that set this register.

Display Register 2 (DR2)

Display Register 2 is used as temporary storage for data to be displayed in the Display B lights on the control panel. The register is displayed on a 3705 whenever the Display/Function Select switch is in the STORAGE ADDRESS, REGISTER ADDRESS, or any of the FUNCTION 1-6 positions. On a 3704, the Display Register 1 and 2 push button must be active. This register can be loaded by pressing the Store or Set Address/Display push button on the control panel; or it can be loaded with data by executing an Output X'72' instruction. See the 3704 or 3705 *Control Panel Guide* for information on the operations that set this register.

Lagging Address Register (LAR)

The Lagging Address Register is a "came from" register. It normally contains the address of the last instruction executed prior to the instruction that is currently being executed. The LAR is loaded from the storage address register each time an instruction is executed in program levels 2, 3, 4, and 5. A program level 1 interrupt prevents setting the LAR until the Exit instruction is executed and no other requests for level 1 are outstanding. This action preserves the address of the last instruction executed before a level 1 request. Since level 1 interrupts are caused primarily by the detection of an error condition, this register becomes extremely important for error recovery procedures. Figure 5-1 shows the contents of LAR after a check condition or a control panel operation other than normal instruction execution.

The control program can load the contents of LAR into a general register by executing an Input X'74' instruction. The control program can then either examine the contents of the general register or display the address on the control panel by using the general register as input to the display registers.

Cycle Utilization Counter Register (CUCR)

The Cycle Utilization Counter Register is a 15-bit binary counter that operates in conjunction with a licensed IBM program, ACF/NCP/VS, to count utilized machine cycles.

CONDITION	*LAR CONTENTS*
Invalid Op Code Check	Address of last instruction executed before the one that caused the check (see note)
Protection Check or Address Exception Check	Address of last instruction executed before the one that caused the check (see note) -or- Address of the instruction that caused the check
In/Out Check at Level 2, 3, or 4	Address of the input or output instruction that caused the check
In/Out Check at Level 5	Address of last instruction executed before the one that caused the check (see note)
IPL (including CCU check)	Address of last instruction executed before IPL phase 1
Adapter Check	Unpredictable
-- Control Panel Operations --	
LOAD ADDRESS COMPARE, PROGRAM STOP or INTERRUPT	Address of last instruction executed before the one whose address is set in switches A to E (3705) or B to E (3704) (see note)
LOAD or STORE, ADDRESS COMPARE, PROGRAM STOP or INTERRUPT	Address of instruction that was loaded from or stored into the location set in switches A to E (3705) or B to E (3704)
INSTRUCTION STEP	Address of last instruction executed
STOP Push Button	Address of last instruction executed

Note: *The last instruction may have been an Exit instruction executing at a higher priority program level than the level executing at the time the condition occurred. Therefore, LAR contains the address of that Exit instruction.*

Figure 5-1. Lagging Address Register (LAR)

Utilized machine cycles consist of the 3705 cycles used for instruction execution, cycle steal operations, or maintenance.

The counter advances once for each 8 utilized cycles. Cycle Utilization Counter data may be accessed using an Input X'7A' instruction and reset with an Output X'7A' instruction. The Cycle Utilization Counter Feature is available for 3705-II, Models J–L only. For information about starting, stopping, and resetting the counter from the operator panel, refer to *Guide to Using the IBM 3705 Communications Controller Control Panel*, GA27-3087.

Old-CRC Register
The Old-CRC accumulation register is used as a temporary storage register in the calculation of a Cyclic Redundancy Check (CRC) character. When an Input X'7B' instruction is executed, the contents of this register are combined with the character in the CRC data register to form a new CRC character. This register is loaded by any Load Halfword instruction. See the *Cyclic Redundancy Check* section of this chapter for a complete description of its use.

Operation Register (OP Reg)
The Operation Register is used to hold the first 16 bits of the instruction being executed. This register can be displayed in the Display B lights on the control panel.

Storage Address Register (SAR)
The Storage Address Register contains the storage address currently used by the program to read or write data to and from storage. This register is loaded from the temporary address register for instruction execution or from the cycle-steal address bus for cycle-steal operations. The contents of SAR are displayed on the 3704 control panel when the SAR and Op Register push button is active.

Temporary Address Register (TAR)
The Temporary Address Register holds the storage addresses pertaining to instruction execution until the storage address register can be changed. This register normally contains the address of the next instruction to be executed. The contents of TAR are displayed in the DISPLAY A lights on the 3705 control panel when the Display/Function Select switch is in the TAR/OP REGISTER position.

Setting/Resetting Interrupt Requests

A particular interrupt request latch can be set as a result of a hardware-detected condition or, in some cases, by the program through the execution of an output instruction. The latch can be reset by either an input or an output instruction, depending upon the specific interrupt request. The procedures for setting and resetting individual adapter interrupt requests are described in the adapter sections.

For special service requests, program levels 1, 2, 3, and 4 may issue a program-controlled interrupt (PCI) request to program levels 3 and 4. Output instructions X'7C' (set PCI level 3) and X'7D' (set PCI level 4) set the PCI interrupt requests. (See Appendix B, Output X'7C' and X'7D'.) Certain bits in Output X'77' (miscellaneous control) reset the PCI requests and

other Central Control Unit interrupt requests such as the interval timer level 3 request and the SVC level 4 request.

Determining the Cause of an Interrupt

The priority of simultaneous interrupt requests assigned to the same interrupt program level is resolved by the order in which the program tests the set/reset condition of the CCU and adapter interrupt request latches.

Interrupt requests from the CCU and the adapters are grouped together according to their source for ease of identification. The set/reset condition of a specific interrupt request latch can be determined by checking the interrupt request group to which it is assigned. Inputs X'76' and X'77' indicate the interrupt requests that are set by the adapters. A request for level 1 sets a bit in Input X'76', and a request for levels 2 or 3 sets a bit in Input X'77'. The CCU interrupt requests for level 1 or levels 2, 3, and 4 are set in Inputs X'7E' and X'7F' respectively. These inputs load the contents of the appropriate interrupt request group into an active general register. (See Appendix B for input instruction bit definitions of interrupt request groups.) The program may then test the general register to identify the request.

Masking Program Level Priorities

Programs at program levels 1, 2, 3, or 4 can selectively mask program levels 2, 3, 4, or 5, and level 1 adapter checks. Level 1 adapter checks, however, can be masked only while the CCU is in the *test mode.* (See *CCU Diagnostic Facilities* in this chapter.) The normal operational priority structure can be changed by Output instructions X'7E' and X'7F' (set/reset mask register). Refer to Appendix B for the mask register bit assignments.

When a program level is masked, use of machine cycles for instruction execution at that program level is suppressed until it is unmasked. Masking is normally used to prevent a higher-priority program level from interrupting a lower-priority level during execution of a time or data dependent routine. For example, if program level 3 contains a routine that should not be interrupted, the level 3 program can mask level 2 interrupts before entering this routine to ensure contiguous instruction execution. When the routine is completed, level 2 should be unmasked to allow interrupts.

If program level 2, 3, or 4 has already been entered, instruction execution at that level is allowed to finish before the masking of that level is effective. For example, if program level 2 interrupts program level 3 and subsequently masks level 3 interrupts, control can return to the level 3 program at the end of level 2 processing. However, once the level 3 program executes an Exit instruction, interrupts to level 3 cannot occur until it is unmasked. If program level 5 is interrupted by another level that sets the level 5 mask, control cannot be returned to level 5 until it is unmasked.

To selectively mask one or more program levels, one of the active general registers is loaded with the bits corresponding to those program levels to be masked. Output instruction X'7E' (set mask register) is then executed using the general register as input to the mask register. To selectively unmask one or more program levels, the same procedure is followed except that the Output X'7F' (reset mask register) instruction is executed.

Important: Masking and subsequent unmasking should be handled with extreme caution to avoid disrupting the normal priority structure. If not used carefully, masking could cause overrun conditions or delay of hardware error indications.

Storage Protect

Storage Protect is a means of notifying the control program whenever the contents of storage are accessed for unauthorized modification. This facility monitors all attempts to modify storage and execute instructions. However, due to hardware restrictions, storage protection is effective only in program level 5 and for cycle-steal operations for Type 2, 3, and 4 Channel Adapters and Type 3 Communication Scanners.

Protection is achieved by a hardware comparison of separate keys assigned to the program and to storage. A user's ability to modify storage is identified by a 3-bit *protect key.* Each program level and cycle-steal mechanism is considered a user, and each has its own protect key. Storage is divided into blocks of 2048 bytes, and each block is assigned a 3-bit *storage key.*

When a protected area of storage is addressed, the storage key for that location is compared with the protect key associated with the user. Access to the location, for operands and instructions, is granted only when the two keys match. For attempts to execute an instruction, the two 3-bit keys *must* be equal. If the keys do not match, a protection exception L1 interrupt request is set. For attempts to modify a storage location, the keys match when (1) the keys are equal, (2) the protect key is X'0', or (3) the storage key is X'7' (unprotected storage).

The protect keys for program levels 1, 2, 3, and 4 are fixed at 0 and cannot be changed. The protect keys for the remaining users are set by the control program with an Output X'73' (set key) instruction. Byte 1, bit 3 of an Output X'73' instruction must be 0 to indicate protect key selection. The protect key address of the desired user is placed in byte 0, bits 4-6,

and the protect key is placed in byte 1, bits 5-7.Figure 5-2 shows the protect key addresses and the users they apply to.

To set any key, byte 1, bit 4 (set key) must also be 1. The set-key bit allows execution of the Output X'73' instruction to access either a storage or protect key without changing the key.

The Output X'73' instruction also sets the storage keys. The storage key of an area is determined by dividing storage into 2K blocks. Each block is then given a storage block address, from 0 to 128 (0 to 256 for 3705, Models J–L), relative to its position in storage. Figure 5-3 shows the storage block address that is assigned to the storage blocks. To set a storage key, the storage block address and the storage key must be placed in a general register. Byte 1, bit 3 (key address select) and bit 4 (set key) of the general register must be 1 to select the storage key and allow it to be set when an Output X'73' is executed. See Appendix B for a definition of the bits used in the Output X'73' instruction.

*Protect Key Address (PKA)**	*Applies to*
Bits 0 1 2	
0 0 0	Protect Key - Program Level 5
0 0 1	Protect Key - CA-1 Cycle Steals†
0 1 0	Protect Key - CA-2 Cycle Steals†
0 1 1	Reserved
1 0 0	Protect Key-Type 3 Scanner Cycle Steals†
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

* Output X'73', byte 0, bits 4-6
† Does not apply to the 3704

Note: *The protect key address is not an actual storage address. This key address is only a reference pointer for assigning a key to a user.*

Figure 5-2. Protect Key Address Bits

The Input X'73' instruction (insert key) can be used to determine the key (storage or protect) that must be used for storage access. When executed, this input instruction places the key that was addressed by the last Output X'73' instruction into byte 1, bits 5-7 of the register specified by the R operand. Therefore, the program must know what type of key and what address was used in the preceding Output X'73'. When an Output X'73' is executed with byte 1, bit 4 (set key bit) off, no keys are changed. However, this allows the address portion of the register to be used by an Input X'73'. Byte 1, bit 3 (key select bit) of the output instruction must also be known in order to determine the type of key (storage or protect) being accessed. See Appendix B for a definition of the bits used in the Input X'73' instruction.

Resetting the Central Control Unit disables storage protection. Therefore, any instruction fetch is valid, and any attempt to modify storage is permitted. The first Output X'73' instruction to be executed after a reset enables storage protect. This output instruction *must* set a storage key of 0 at the key address that corresponds to the storage block where the instruction execution is taking place. Otherwise a *protection check* occurs unless the storage key is already 0.

When the controller is powered on, the bits in all the protect keys except program levels 1-4 and all the storage keys assume a random bit pattern. Therefore, each key must be initialized by an Output X'73' containing its key address and key type (storage or protect). Until each key is fully initialized, caution must be exercised in the control of program levels and I/O activity that may depend on storage protection.

Interval Timer

The interval timer provides a program level 3 interrupt request (Interval Timer L3) approximately once every 100 milliseconds. The time interval is derived from

3705 Models A—H and the 3704

SKA 8its 0 to 2	SKA Bits 3 to 6																
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
000	0000	0800	1000	1800	2000	2800	3000	3800	4000	4800	5000	5800	6000	6800	7000	7800	3704 and 3705
001	8000	8800	9000	9800	A000	A800	B000	B800	C000	C800	D000	D800	E000	E800	F000	F800	
010	10000	10800	11000	11800	12000	12800	13000	13800	14000	14800	15000	15800	16000	16800	17000	17800	3705 only
011	18000	18800	19000	19800	1A000	1A800	1B000	1B800	1C000	1C800	1D000	1D800	1E000	1E800	1F000	1F800	
100	20000	20800	21000	21800	22000	22800	23000	23800	24000	24800	25000	25800	26000	26800	27000	27800	
101	28000	28800	29000	29800	2A000	2A800	2B000	2B800	2C000	2C800	2D000	2D800	2E000	2E800	2F000	2F800	
110	30000	30800	31000	31800	32000	32800	33000	33800	34000	34800	35000	35800	36000	36800	37000	37800	
111	38000	38800	39000	39800	3A000	3A800	38000	3B800	3C000	3C800	3D000	3D800	3E000	3E800	3F000	3F800	

Applicable to 3705-II Models E—H only

3705 Models J—L only

SKA 8its 3 to 6	SKA 8its 7 to 10															
	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0000	0800	1000	1800	2000	2B00	3000	3800	4000	4800	5000	5800	6000	6800	7000	7800
0001	8000	8800	9000	9800	A000	AB00	B000	B800	C000	CB00	D000	D800	E000	E800	F000	F800
0010	10000	10800	11000	11800	12000	12800	13000	13800	14000	14800	15000	15800	16000	16800	17000	17800
0011	18000	18B00	19000	19800	1A000	1AB00	18000	1B800	1C000	1C800	1D000	1D800	1E000	1EB00	1F000	1F800
0100	20000	20800	21000	21800	22000	22800	23000	23800	24000	24800	25000	25800	26000	26B00	27000	27800
0101	28000	28800	29000	29800	2A000	2A800	2B000	28800	2C000	2C800	2D000	2D800	2E000	2E800	2F000	2F800
0110	30000	30800	31000	31800	32000	32800	33000	33800	34000	34B00	35000	35800	36000	36800	37000	37800
0111	38000	38800	39000	39800	3A000	3A800	38000	3B800	3C000	3C800	3D000	3D800	3E000	3EB00	3F000	3F800
1000	40000	40800	41000	41800	42000	42800	43000	43800	44000	44B00	45000	45800	46000	46B00	47000	47B00
1001	48000	48800	49000	49800	4A000	4A800	4B000	4B800	4C000	4C800	4D000	4D800	4E000	4EB00	4F000	4F800
1010	50000	50800	51000	51800	52000	52B00	53000	53800	54000	54800	55000	55800	56000	56800	57000	57800
1011	58000	58800	59000	59800	5A000	5A800	58000	5B800	5C000	5C800	5D000	5D800	5E000	5E800	5F000	5F800
1100	60000	60800	61000	61800	62000	62800	63000	63800	64000	64800	65000	65800	66000	66800	67000	67800
1101	68000	68800	69000	69800	6A000	6A800	68000	6B800	6C000	6C800	6D000	6D800	6E000	6E800	6F000	6F800
1110	70000	70800	71000	71800	72000	72800	73000	73800	74000	74800	75000	75800	76000	76800	77000	77800
1111	78000	78800	79000	79800	7A000	7A800	7B000	78800	7C000	7C800	7D000	7D800	7E000	7E800	7F000	7F800

Notes:

1. Storage addresses are shown in hexadecimal.
2. Storage addresses shown are beginning addresses of block.
3. Storage Key Address (SKA) bits correspond to Output X'73' instruction byte 0, bits 0 to 6.

Figure 5-3. Storage Key Addresses

the 50/60 Hertz power line frequency, and its accuracy depends on the stability of the power source.

The interval timer may be used to maintain a real-time clock in storage, perform long and short I/O time-outs, and perform supervisory functions on a periodic basis. The interval timer interrupt request can be reset by executing an Output X'77' (miscellaneous control) instruction with byte 1, bit 1 set to 1.

Cyclic Redundancy Check (CRC)

Although any cyclic redundancy check (CRC) can be performed by a program algorithm, the communications controller has special hardware to speed the CRC accumulation function required for binary-synchronous (BSC) EBCDIC and Synchronous Data Link Control (SDLC) communications.

For all Load Halfword instructions executed at program levels 1, 2, 3, or 4, the halfword obtained from storage is loaded into both the specified general register and a register called the old-CRC register. For normal operations (non-CRC), the loading of data into the old-CRC register serves no function.However, when a CRC update is to be performed, an additional instruction is not required, because the old CRC accumulation is automatically loaded into the old-CRC register.

To generate a new CRC accumulation, a Load Halfword instruction should be used to load the old-CRC register. The next character to be included in the CRC accumulation should then be placed in the low-order byte of one of the active general registers. Any output instruction can then be executed using the general register as the source of output. This places the character from the general register into a register called the CRC data register.

Note: *When updating the CRC accumulation, the output instruction executed also performs its normal functions. Therefore, caution must be taken not to execute an Output instruction that can alter the status or state of either an adapter or an interface.*

After a character to be added is in the CRC data register and the old-CRC accumulation is in the old-CRC register, one of the following input instructions should be used to load the new CRC character accumulation to a general register.

- Input X'7B' (BSC CRC) - This instruction is used for interface lines defined as BSC. It stores the new CRC in bytes 0 and 1 of the specified general register.
- Input X'7C' (SDLC CRC) - This instruction is used for interface lines defined as SDLC. It stores the new CRC in the low-order byte (byte 1), bits 0-7 of the specified general register. During execution of the input instruction, the character to be included in the CRC accumulation and the old-CRC are combined by hardware circuits, and the new-CRC is stored in bytes 0 and 1 of the general register specified in the input instruction. With Extended Addressing, bits 4-7 of byte X are reset to 0. The new CRC accumulation may then be placed in storage by the program.

Programming Note

The Load Halfword instruction that loads the old-CRC accumulation, the output instruction that loads the character into the CRC data register, and the input instruction (X'7B' or X'7C') that loads the new CRC into a general register do not have to be consecutive instructions. However, there must not be another Load Halfword instruction (executed at program levels 1, 2, 3, or 4) between loading the old CRC in the old-CRC register and loading the new CRC to a general register. Also, another output instruction must not be executed between loading the CRC data register and storing the new CRC.

Initial Program Load (IPL)

The initial program load (IPL) mechanism controls the loading of an initial program into the controller via a channel adapter (1) when the system is first powered up, (2) when further processing is not possible due to an error condition, or (3) when the channel adapter decodes a Write IPL command. Three phases of the IPL program (IPL Phase 1-3) control the loading operation. IPL is accomplished by successful completion of all three phases. See Chapter 11 for a description of remote communications controller IPL.

Phase 1 of the IPL operation is a general reset to the controller. During phase 2, a small bootstrap program is automatically loaded into storage from the controller's read-only-storage (ROS) array, and control passes to this program. Execution of the bootstrap program (phase 3) then controls channel operations until the first *load module* from the host is successfully transferred into storage under a Write IPL channel command (X'05').

After successful transfer of the first program segment into storage, the initial program loading operation performed by the bootstrap program is complete. The controller is initialized, and the bootstrap program passes control to the loaded program segment. This program segment then controls the loading of whatever additional load modules are required to complete the program load operation.

The two lights on the control panel labeled IPL Phase, indicate the three phases of IPL. These lights

are a binary representation of the phase number. That is, 01 = phase 1, 10 = phase 2, and 11 = phase 3.

The Load light on the control panel comes on when IPL is initiated. It does not go off when IPL Phase 3 is completed. It must be turned off by executing an Output X'79' instruction when the program determines that the controller has been completely loaded.

IPL starts when either of the following occurs:

- The Diagnostic Control switch is in the PROCESS, CCU CHECK HARD STOP or BYPASS CCU CHECK STOP position and either (1) the Load push button is pressed; (2) a power-on occurs; (3) a channel adapter decodes a Write IPL command, and the controller is either not already in IPL phase 1, 2, or 3 or not in a hard stop condition; or (4) the control program executes an Output X'79' instruction with byte 0, bit 2 (set IPL) set to 1 in the register specified by the R operand.
- The Diagnostic Control switch is in the PROCESS position, a Central Control Unit check occurs, and the controller is not in IPL phase 1, 2, or 3.

IPL Phase 1 - Reset: During this phase the Load light is turned on, the CCU is placed in the test mode and a general reset occurs in the controller. Unless the IPL is initiated by a power-on sequence, the phase 1 reset does not affect the state of the channel adapter(s).

The reset in the CCU:

- Sets the mask bits for program levels 2-5 and level 1 adapter requests.
- Resets all 'interrupt entered' latches.
- Resets all CCU interrupt requests.
- Resets program stop and hard stop.
- Prohibits storage references and instruction execution.
- Disables the storage protect facility until an Output X'73' instruction is executed.
- Turns *on* the Test light on the control panel.

IPL Phase 2 - Bootstrap Load: In this phase the bootstrap program is automatically loaded into storage from read-only-storage (ROS). Different ROS arrays are installed for different types or combinations of types of channel adapters installed. The bootstrap program for either channel adapter begins loading at address X'0000' and is 512 bytes long. When two channel adapters are installed, the bootstrap program is 1024 bytes to handle IPL from either channel adapter.

When the bootstrap load operation is complete, the IPL L1 interrupt request is set, and the controller enters IPL phase 3 (bootstrap execution).

IPL Phase 3 - Bootstrap Execution: The bootstrap program begins execution at address X'0010' as a result of the IPL level 1 interrupt request set by phase 2 and operates entirely at program level 1.

The bootstrap program is divided into two sections. The first section:

1. Saves the general registers of group 0 starting at storage location X'0780'. Each register location starts on a fullword boundary.
2. Verifies the operation of the controller instructions to be used in the second section of the bootstrap program.
3. If the program is allowed to continue, it saves external registers X'76', X'7D', and X'7E' at storage locations X'0702', X'0704', and X'0706' respectively.
4. Resets the test mode and turns the Test light on the control panel *off*.

The second section of the bootstrap program controls the channel adapter operations until the first program load module is successfully transferred from the host processor.

If no outstanding command or final status is pending in the channel adapter, it generates an asynchronous status of Device End and Unit Check. If any command other than Write IPL is pending, the channel adapter generates a final status of Channel End, Device End, and Unit Check. In either case, sense bit 6 (Not Initialized) is set for the subsequent Sense command. A Write IPL command normally follows the Sense command. The Not Initialized bit is reset after the first program segment is successfully transferred into storage from the host processor.

The Write IPL command causes the transfer of the first load module from the host processor into controller storage. Under the Write IPL command, the load module is stored in sequential locations starting at storage location X'0400'. The maximum size of this load module cannot exceed 768 bytes. After successful completion of this transfer, the bootstrap program executes an Output X'77' instruction with byte 0, bit 0 (reset IPL L1) *on* in the register specified by the R operand. This resets the IPL L1 interrupt request and turns *off* the IPL Phase lights on the control panel. The bootstrap program then turns control over to the load module at program level 1 by branching to storage location X'0404'.

The IPL operation is complete when the IPL L1 interrupt request is reset and the IPL Phase lights are turned *off*. However, the Load light on the control panel remains on until reset by byte 1, bit 1 of Output X'79'. The program just loaded from the host should execute the Output X'79' when it is determined that the controller is completely loaded.

Programming Note
The first two halfwords of the load module must contain an IPL source identification (host processor ID) and the number of bytes in the load module (including the source ID and count bytes).

Check Conditions During IPL
Central Control Unit (CCU) checks are prohibited during IPL phase 1 since that phase performs a reset. If a CCU check occurs during IPL phase 2 or IPL phase 3, a *hard stop* occurs.

If the bootstrap program does not reach completion for any of the following reasons, the controller either comes to a hard stop or enters a loop and attempts to display the cause of the check condition in the control panel display lights.

- CCU check hard stop condition.
- Improper operation of an instruction during instruction verification in the first section of phase 3.
- Program continuity check (Type 2 and Type 3 CA only). This check ensures that all instructions in the bootstrap program have been executed in the correct sequence.
- Channel adapter disabled.
- Channel adapter hardware malfunction.
- Byte count in the second halfword of the load module does not compare with the number of bytes transferred from the host.

Input/Output Instructions
The control program uses input and output instructions to control and monitor the status of the CCU and the installed adapters. Appendix B defines the bits for each of the input and output instructions.

Input Instructions
The Central Control Unit has 16 external registers that can be accessed by executing input instructions. With these input instructions, the control program monitors the status of the CCU, the communication scanners, the channel adapters, and the control panel, and is informed of any error conditions. Two of the input instructions (X'75' and X'78') are not used, and if executed, the bits in the general register are set to zero. The other thirteen instructions set the bits of the general register according to the particular external register value. (Appendix B defines the bits within each input instruction.)

Input X'70' (Storage Size): This instruction loads a general register with a combination of bits that indicates the amount of storage installed.

Input X'71' (Panel Address/Data Entry): This instruction loads a general register with a combination of bits to indicate the storage or register address or data to be used in a control panel function. These bits correspond to the Address/Data switches on the 3705 or the Hexadecimal Display switches B-E on the 3704. Through the use of this instruction. the program can accept information from the operator.

Input X'72' (Panel Display/Function Select Control): This instruction loads a general register with a combination of bits to indicate the position of the control panel Display/Function Select switch. Through the use of this instruction, the program can accept information from the operator.

Note: *The STATUS and the TAR & OP REGISTER positions of the 3705 Display/Function Select switch are not included in the register.*

Input X'73' (Insert Key): This instruction loads a general register with the storage key or protect key addressed by the last Output X'73' instruction executed. The program must know the bit setting of the the key address bits set in the last Output X'73' instruction before this input is meaningful.

Input X'74' (Lagging Address Register): This instruction loads a general register with the contents of the lagging address register. When this input is executed at program levels 2, 3, or 4, the address transferred into the general register is that of the last instruction executed before the input instruction.

When Input X'74' is executed in program level 1, the address transferred into the general register is that of the last instruction executed at the program level that was active before the level 1 interrupt.

Input X'76' (Adapter Level 1 Interrupt Requests): This instruction loads a general register with information that can be used to determine which channel adapter or communication scanner caused a level 1 interrupt. In a remote communications controller, this instruction is also used to determine if the interrupt was from the remote program loader.

Input X'77' (Adapter Level 2 or 3 Interrupt Requests): This instruction loads a general register with information that can be used to determine which channel adapter or communication scanner caused a level 2 or level 3 interrupt.

Input X'79' (Utility): This instruction loads a general register with utility information. When it is executed in program level 1, byte 1, bits 0-3 designate the program level that was operating before the level 1 inter-

rupt. When it is executed in program levels 2, 3, or 4 (or level 1 if level 1 is re-entered immediately after a level 1 Exit), byte 1, bits 0-3 have no significance and are set to zero. When Input X'79' is executed at any level, byte 0, bits 6 and 7 indicate the state of the program level 5 C and Z condition latches.

Input X'7A' (Cycle Utilization Counter Register): This instruction provides access to an accumulated count of the 3705 machine cycles used for cycle steal operations, instruction execution, and maintenance. The counter, operating under a release of ACF/NCP/VS (a licensed IBM program), allows a user to measure 3705 utilization. The Cycle Utilization Counter is a standard feature for 3705 Models J–L only.

Input X'7B' (BSC CRC Register): This instruction loads a general register with the new binary synchronous CRC character from the BSC CRC register.

Input X'7C' (SDLC CRC Register): This instruction loads a general register with the new synchronous data link control CRC character from the SDLC CRC register. See the *Cyclic Redundancy Check (CRC)* section of this chapter.

Input X'7D' (CCU Check Register): This instruction loads a general register with the contents of the CCU check register. The program can test this register to determine the cause of a program level 1 interrupt due to a CCU check condition.

Input X'7E' (CCU Level 1 Interrupt Requests): This instruction loads a general register with a configuration of bits to indicate the cause of a program check or a program level 1 interrupt due to an address compare or IPL. When a program check occurs, Input X'7D', byte 0, bit 3 should also be tested to determine if the check occurred while in program level 1 or in one of the other program levels.

Input X'7F' (CCU Level 2, 3, or 4 Interrupt Requests): This instruction loads a general register with a combination of bits to indicate the cause of various interrupts. Certain interrupt requests from program levels 2-4 set a bit associated with the type of request presented.

Output Instructions

The Central Control Unit has 16 external registers that can be loaded by executing output instructions to control its operation and data flow. However, the Output X'74', X'75', X'76', X'7A', and X'7B' instructions are not used, and if executed, the bit settings of the register specified by the R operand are ignored. The instructions that have an effect on an external register are as follows. (Appendix B defines the bits within each output instruction.)

Output X'70' (Hardstop): This instruction turns the 'hardstop' latch in the CCU *on*. This stops all machine activity and requires a reset and IPL to continue operation. Since this instruction performs a function and not an operation, the bit settings of the general register are ignored.

Output X'71' (Display Register 1): This instruction loads the contents of the general register into display register 1. Whenever the Display Register 1 and 2 push button on the 3704 control panel or the Display/Function Select switch on the 3705 control panel is in the STORAGE ADDRESS, REGISTER ADDRESS, or any of the FUNCTION 1-6 positions, the bits of the register are displayed in the Display A lights on the control panel.

The Program Display light on the control panel also comes *on* to inform the operator that information has been placed in the display register.

Output X'72' (Display Register 2): This instruction causes the contents of the general register to be loaded into display register 2. Whenever the Display Register 1 and 2 push button on the 3704 control panel or the Display/Function Select switch on the 3705 control panel is in the STORAGE ADDRESS, REGISTER ADDRESS, or any of the FUNCTION 1-6 positions, the bits of the register are displayed in the Display B lights on the control panel.

The Program Display light on the control panel also comes *on* to inform the operator that information has been placed in the display register.

Output X'73' (Set Key): This instruction causes the contents of the general register to be used to address and/or set the storage and protect keys.

Output X'77' (Miscellaneous Control): This instruction causes the contents of the specified general register to be used to set or reset various interrupt requests.

Output X'78' (Force CCU Checks): This instruction provides the means for testing the CCU check circuits under diagnostic control. It causes the contents of the general register to be used to force certain error conditions in the CCU data flow. This instruction is valid only while the CCU is in the test mode. Refer to the *CCU Diagnostic Facilities* section of this chapter for details on forcing check conditions.

Output X'79' (Utility): This instruction causes the contents of the specified general register to set and/or reset various hardware latches and lights.

Output X'7A' (Cycle Utilization Counter Reset): When this instruction is issued, the bits in the Cycle Utilization Counter Register are reset to zero. The general register bits of the Output X'7A' instruction are ignored.

Output X'7C' (Set PCI L3): This instruction causes a Program Controlled Interrupt request to be set for program level 3 (PCI L3). This allows a program level to transfer a processing requirement to a different priority program level. Since this instruction performs a function, the bit settings of the general register are ignored.

Output X'7D' (Set PCI L4): This instruction causes a Program Controlled Interrupt request to be set for program level 4 (PCI L4). This allows a program level to transfer a processing requirement to a lower priority level. Since this instruction performs a function, the bit settings of the general register are ignored.

Output X'7E' (Set Mask Bits): This instruction causes the mask bits of the program levels to be set according to the contents of the general register. When a mask bit is set on, interrupts for the program level that corresponds to that bit are not permitted.

Output X'7F' (Reset Mask Bits): This instruction causes the mask bits of the program levels to be reset according to the contents of the general register.

CCU Checks

The Central Control Unit performs various hardware checks on the program operation and hardware circuits in the controller to ensure proper operation. When a check condition is detected, bits set in the CCU check register indicate the type of check. The control program can then execute an Input X'7D' instruction to load a general register with the information available in the check register.

The first occurrence of a check condition sets the CCU check register. Subsequent checks are not allowed to enter the check register until it is reset. The check register is reset by executing an Output X'77' instruction with byte 0, bit 1 set to 1, or by pressing the CCU Check Reset or Reset push button on the control panel.

When a CCU check condition is detected and the Diagnostic Control switch on the control panel is in the PROCESS position, an automatic IPL is initiated. If the check condition persists after the IPL sequence is initiated, the 'hard stop' latch is set, and the machine stops. Reset and re-IPL are the only means of resetting a hard stop condition.

If the Diagnostic Control switch is not in the PROCESS position, the action taken for a particular switch position is described in the 3704 or 3705 *Control Panel Guide.*

Program Checks

The Central Control Unit hardware monitors the control program operation for proper instruction execution and indicates to both the control program and the operator when a program check is detected.

Detection of a program check causes a level 1 interrupt request to be set. If the Display/Function Select switch is in the STATUS position, the type of check is indicated in the Display B lights on the control panel. The control program can determine the cause of the check by executing an Input X'7E' instruction and testing the register bits. Program action may vary according to the type of check detected; see the descriptions of each check (below) for appropriate action.

If error recovery for the program check is successful, the control program can reset the interrupt request by executing an Output X'77' instruction (miscellaneous control) with byte 1, bit 5 set to 1.

A program check while level 1 is active is indicated in the CCU check register (Input X'7D') by byte 0, bit 3 being set to 1, and the type of check is indicated in Input X'7E'. This condition causes an automatic IPL unless the Diagnostic Control switch on the control panel is in one of the check-control positions or the controller is in IPL Phase 3.

Below is a description of each of the four program checks.

In/Out Check

Input and output instructions are privileged instructions that can be executed only in program level 1, 2, 3, or 4. Any attempt to execute an input or output instruction at program level 5 causes a level 1 interrupt and sets the In/Out Check bit in the CCU interrupt request group 1 register (Input X'7E').

The In/Out Check bit is set when an input or output instruction is executed at program level 1, 2, 3, or 4 with an external register address that is either not assigned or not recognized by any adapter. For example, issuing an Input X'38' instruction (nonexistent) or an Output X'52' (for Type 2 Channel Adapter only) when a Type 1 Channel Adapter is installed sets the In/Out Check bit. An In/Out check is also set if an Inbus parity check is detected by the CCU during execution of an input instruction.

If an In/Out Check is detected while in program level 1, a no-op is performed, and the Program Check in Level 1 bit in the CCU check register is set along with the In/Out Check L1 interrupt request. The In/Out check is then handled as a CCU check.

Protection Exception

Whenever the control program attempts to modify a storage location that is protected and does not have a matching protect key, the result is a protection exception. A protection exception sets the Protection Check L1 interrupt request and suppresses storage access.

When a protection exception is detected during a cycle-steal operation, it is signaled to the Type 2, 3, or 4 Channel Adapter or Type 3 Communication Scanner involved as an addressing error. The adapter immediately terminates its cycle-steal operation and sets its check-interrupt request bit assigned to program level 1.

If a protection exception occurs when storage is accessed to execute an instruction, an effective no-op is performed, and the instruction address register (IAR) is not updated. If the exception occurs in program level 2, 3, 4, or 5, a level 1 interrupt request is set. The control program can normally determine the address of the last instruction executed by examining the contents of the lagging address register (LAR).

A protection exception caused by an instruction attempting to modify a storage location can occur only when program level 5 is active. (The protect keys for the other program levels are fixed at 0 by the hardware design.) Such a protection violation causes the instruction to be suppressed and sets the level 1 interrupt request. The address of the instruction that caused the exception can be determined by examining the contents of the lagging address register (LAR).

If a protection exception is detected while in program level 1, the result is a no-op, and the Program Check in Level 1 bit in the CCU check register is set along with the Protection Check L1 interrupt request. The protection exception is then handled as a CCU check.

Invalid Op-Code Check

The communications controller is limited to the 51 instructions described in Chapter 4. Each instruction has its own operation code bit structure. Whenever an attempt is made to execute an instruction with an op code that does not compare to any of the 51 valid op codes, the Invalid Op Check level 1 interrupt request is set and instruction execution is suppressed.

If an attempt is made at program level 2, 3, 4, or 5 to execute an invalid op code, an interrupt occurs to program level 1.

If an attempt is made at program level 1 to execute an invalid op code, the instruction execution is suppressed, and the Program Check in Level 1 bit in the CCU check register is set along with the Invalid Op Check L1 request. The invalid op code check is then handled as a CCU check.

Address Exception

An address exception occurs whenever an attempt is made to gain access to an uninstalled storage location for the given machine. For example, addressing storage location 52,304 when the controller contains only 49,152 bytes of storage causes an address exception.

When an address exception is recognized, an effective no-op is performed for the machine cycle in which it is detected. An Address Exception Check level 1 interrupt is then requested to inform the control program of the error.

An address exception during a cycle-steal operation is signaled to the adapter involved as an *address check.* Upon the detection of an address check, the adapter immediately terminates its cycle-steal operation and sets its check interrupt request assigned to program level 1. This informs the control program of the error.

The following checks for address exceptions are made during instruction execution.

a. A check is made in the first cycle of each instruction as the storage address register (SAR) is loaded with the address of the instruction. If an address exception is detected, an effective no-op is performed and the instruction address register (IAR) is not updated. If an address exception occurs during the first cycle of an instruction executing at program level 2, 3, 4, or 5, a level 1 interrupt is taken and the address of the instruction last executed in that program level can normally be determined by examining the contents of the lagging address register (LAR).
b. A check is made in each subsequent cycle of multicycle instructions as the SAR is loaded with the address of the storage location to be accessed. If an address exception is detected, the operation in that cycle is suppressed. If an addressing exception occurs during the second or third cycle of an instruction executing at program level 2, 3, 4, or 5, a level 1 interrupt is taken, and the address of the instruction that caused the error can be determined by examining the contents of the lagging address register.

If an address exception is detected while program level 1 is active, the Program Check in Level 1 bit in the CCU check register and the Address Exception Check L1 bits are set to 1. The address exception is then handled as a CCU check.

CCU Diagnostic Facilities

The communications controller has diagnostic facilities designed to allow the control program to perform test procedures on the controller hardware. The diagnostic test routines can be either part of the online control program or a standalone control program used for testing purposes only. If these test routines are part of the online control program, the communication lines and adapters not being tested are allowed to continue operating.

To use the CCU diagnostic facilities of the control program, the CCU must be in the test mode. This mode of operation allows the use of certain bits and external registers that are not otherwise available to the control program. The test mode is entered by executing an Output X'79' instruction with byte 1, bit 2 (set test mode) set to 1 in the register specified by the R operand. Upon completion of testing, the control program should reset the test mode by executing an Output X'79' with byte 1, bit 3 (reset test mode) *on.*

While in the test mode, the following operations are available for program use:

1. Set and reset diagnostic L2 - Output X'77', byte 0, bit 6 sets a level 2 interrupt request that allows the program to execute a user diagnostic routine during normal program execution. When a level 2 interrupt occurs, the control program should test byte 1, bit 0 of the CCU interrupt request group 2 (Input X'7F') to determine if the interrupt is for diagnostic purposes. On completion of the diagnostic routine, the diagnostic L2 interrupt request must be reset by executing an Output X'77' with byte 0,bit 7 (reset diagnostic L2) set to 1.
2. Set and reset the bypass CCU check stop mode - Output X'79', byte 1, bit 4 set to 1 allows CCU check stops to be bypassed. If the Diagnostic Control switch on the control panel is in the PROCESS or the CLOCK STEP position, the bypass CCU check stop mode forces the check control hardware to operate as if the panel switch were in the BYPASS CCU CHECK STOP position. If the Diagnostic Control switch is in any other position, this operation is ignored. To reset the bypass mode, the control program must execute an Output X'79' instruction with byte 1, bit 5 set to 1.
3. Set and reset L1 adapter mask - Program level 1 interrupt requests caused by a check condition in an adapter (scanner or CA) can be masked by using an Output X'7E', byte 1, bit 1. This operation performs the same functions for the level 1 adapter checks as those described in the section on *Masking Program Level Priorities* in this chapter. To unmask the level 1 requests, the control program must execute an Output X'7F' (reset mask bits) with byte 1, bit 1 set to 1.
4. Force CCU checks - While in test mode, the control program can use the Output X'78' instruction. When used in a 3705, the setting of bits in byte 0 of this output instruction complements bits in the bytes being directed to the Arithmetic Logic Unit (ALU) to cause parity checks. The bits in byte 1 are used to complement storage and Z bus parity, and cause A-register or INDATA bus checks.

   When used in a 3704, setting bits 5, 6, and 7 of byte 0 selects the instruction cycle in which the selected error occurs. Bits 0-4 of this byte are not used by the 3704. The bits in byte 1 are used to complement storage and Z bus parity, cause A-register checks, and cause B-register, SAR, and Op Reg parity errors.

This chapter is intended to give the reader a basic understanding of the operation of the Type 1 Communication Scanner and the requirements necessary to program the scanner.

The Type 1 Communication Scanner (Type 1 Scanner) permits the control program to communicate with a line or autocall interface. This communication is done through the use of input and output instructions executed by the control program to the interface addressed by the communication scanner. The Type 1 Scanner makes data, status, and control information pertaining to each of the installed communication lines available to the program.

Most of the scanner functions are under direct control of the level 2 interrupt program and of processing routines that may be in other program levels. This permits increased flexibility by decreasing the number of restrictions caused by requirements of fixed hardware. The control program must assume the responsibility of the assembly and disassembly of characters, control character recognition, translation, and line control. Character assembly and disassembly are required of the program because the Type 1 Scanner transfers only one information bit at a time to or from the interface.

The Type 1 Scanner differs slightly, depending on whether it is installed in a 3704 or a 3705. In a 3705, the scanner supports four LIBs with a maximum of 64 lines. When installed in a 3704, the Type 1 Scanner supports two LIBs with a maximum of 32 lines.

Operation and Data Flow

The Type 1 Communication Scanner hardware operates asynchronously with the other functional components of the controller. See Figure 6-1 for the Type 1 Scanner general hardware operation.

A *scan counter* sequentially addresses each interface in search of a service request. If a bit service request is detected, the scanner stops on that interface and requests a level 2 interrupt. All data and information for that interface is then made available to the control program through input instructions. When the program executes the proper output instructions, the scanner hardware passes information to the interface hardware.

When a character service request is detected, the control program is notified by a level 2 interrupt request. The scanner does not stop for a character service interrupt, but continues generating addresses in search of a bit service request.

Programming for the Type 1 Scanner should normally be done in the level 2 interrupt program because

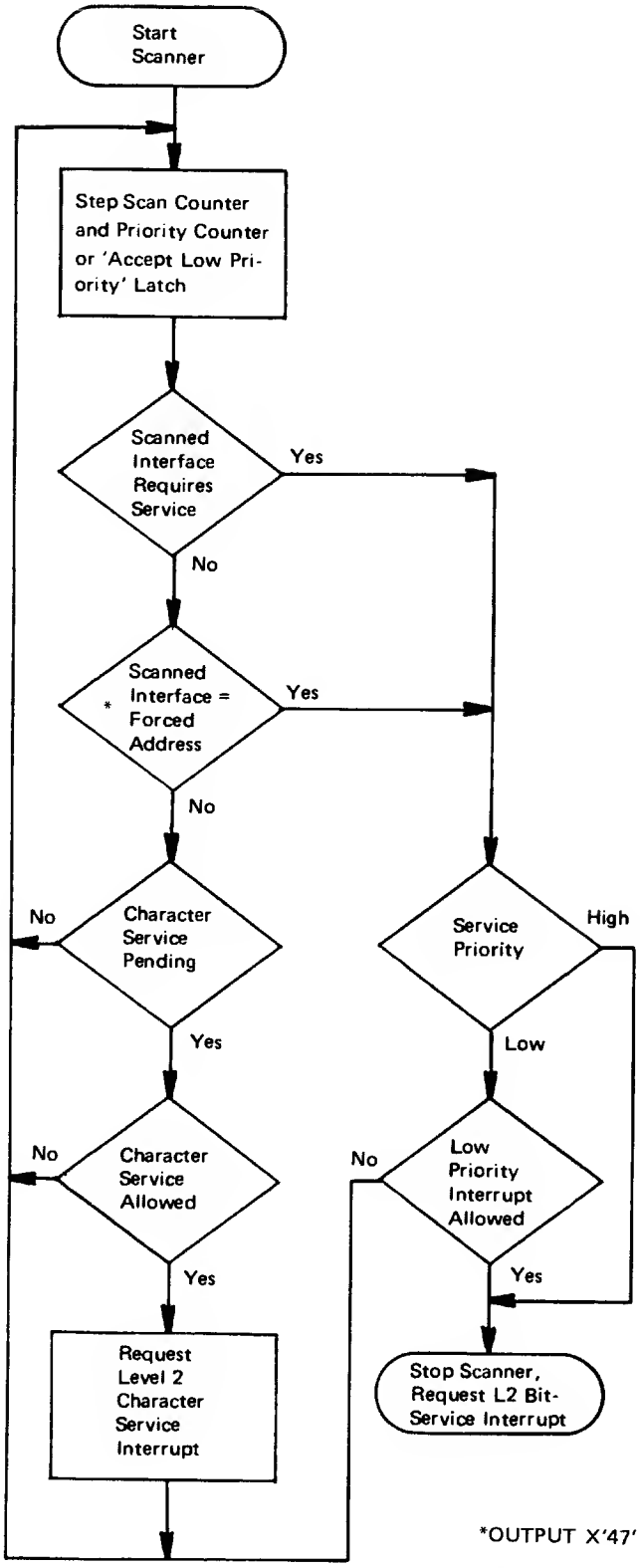


Figure 6-1. Type 1 Communication Scanner Operation

of the high priority placed on communication lines. However, the transferred bits and characters may be processed in a lower priority program level. See Figure 6-2 for a general flow of the Type 1 Scanner level 2 program.

When a level 2 interrupt occurs, an Input X'41' (interface address) instruction should be the first instruction executed to determine the cause of the interrupt. A branch can then be taken to the bit service or character service routine to handle the request.

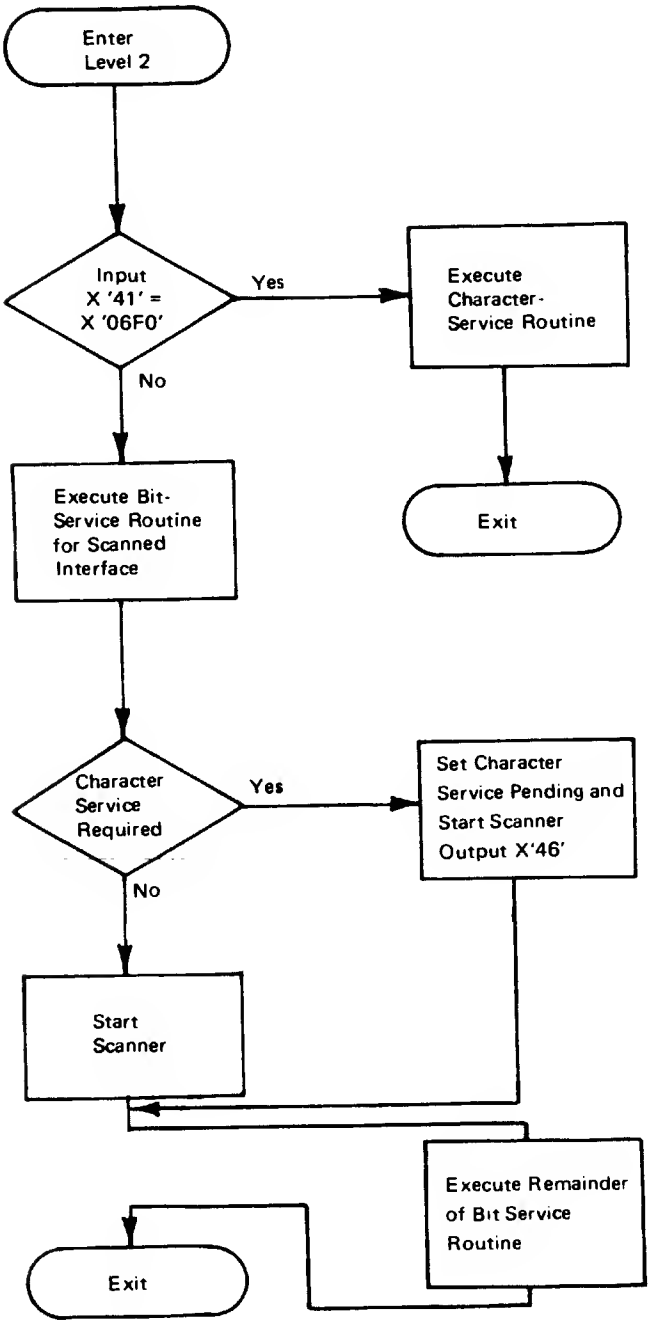


Figure 6-2. Level 2 Program Flow (Type 1 Communication Scanner)

The bit service routine determines if a bit has actually been received or must be transmitted. If a bit has been received, the routine places the received bit in the proper storage location allocated for the character to be received. If a bit is to be transmitted, the routine must remove a bit from the character and pass it to the interface. When the last bit of a character has been received or transmitted, the bit service routine must request a character service interrupt from the scanner hardware.

Before exiting the level 2 bit service routine, the program must restart the scanner by executing the proper output instruction (Output X'41' or Output X'46').

Interface Scanning

All interface addresses (both used and unused) assigned to the LIB positions are scanned sequentially. These lines are physically addressed by stepping a *scan counter* that generates an interface address. As the scan counter steps through each interface address, a check is made to see if that interface has a request for service. If a service request is present, the scanner checks the service priority and mode of the interface. If interrupts are allowed, the scanner determines whether the request is for bit service or character service. If bit service is required, the scanner *stops* on the interface and causes a level 2 interrupt request. If the request is for character service, the scanner signals the control program by requesting a level 2 interrupt.

When the bit service routine has obtained all necessary information pertaining to that line, it must execute an Output X'41' (or Output X'46' to request character service). These output instructions reset the level 2 bit service interrupt request and restart the scan counter.

Note: *The scan counter, when not stopped to allow a particular interface to be serviced, is stepped at a rate of 400 nanoseconds per interface in a 3705 and at a rate of 600 nanoseconds per interface in a 3704.*

Bit-Service Priority

Higher-speed communication lines should be serviced more frequently than lower-speed lines. To do this, the Type 1 Scanner allows the program to assign one of two (high or low) bit service priorities to each interface. An Output X'42' (control A) instruction is used to set the service priority for a particular interface.

When an interface is scanned, its assigned service priority is checked to determine whether it has high or low priority. If the service priority is high, and the interface requires service on this scan, the scanner stops and causes a level 2 bit service interrupt request.

This permits the program to service that interface. A high-priority interface is serviced each time the line is scanned and bit service is required.

If the service priority is low, and the interface requires service, the scanner stops only if the interface being addressed is the first low-priority line encountered on that cycle of the scan counter. (Refer to Figure 6-3.) To simplify this concept, Figure 6-3 shows only the first ten lines, and all are assumed to have a bit service request each time the scanner addresses them. Also assume for this example that a cycle is one complete scan of all interface addresses.

In a 3705, when the scanner addresses the first low priority interface requiring service and the control program executes an Input X'41' instruction, the priority counter is reset to zero. The priority counter then adds a one to its count for each interface scanned (high or low priority) following the reset. As the scanner encounters the next and any other low priority interface, the priority counter is checked to see if a low priority interrupt is allowed. Low priority interrupts are not allowed until the counter reaches 65. When the scanner stops on the next low-priority interface and the control program executes an Input X'41' instruction, the *priority counter* is reset to zero and again, low-priority interrupts are not allowed until the counter reaches 65.

In a 3704, when a service request from a low priority line is honored by the scanner, that line address is stored in the address remember register and the 'accept low priority' latch is reset. When the scanner is restarted by an Output X'41' instruction, it will continue to honor service requests from lines assigned high priority but will service no further low priority lines until the address in the scan counter is one greater than that in the address remember register, at which time the 'accept low priority' latch is set again. The scanner has then passed the address that caused the last low priority bit service interrupt and is able to stop on the next low priority line requesting service.

Programming Note

All interfaces are set to high priority by a power-on-reset, IPL, machine reset, or a scanner disable (Output X'45' byte 0, bit 2).

Interrupt Requests

The Type 1 Scanner can initiate interrupt requests for either level 1 or level 2 service. Level 1 requests occur when the scanner detects an error condition affecting interface or scanner operation. Two different types of level 2 interrupt requests can occur for the purpose of handling normal service requests: the level 2 bit service request and the level 2 character service request.

The following paragraphs describe the bit service and character service interrupt requests.

Bit Service Interrupt Request

The Type 1 Scanner level 2 bit service interrupt request occurs when the scanner stops on the address of an interface requesting service. Once the scanner has stopped on an interface, the program can identify the interface by executing an Input X'41' (interface address) instruction. Input X'41' loads a general register with the storage address associated with the interface requesting service. (See Figure 3-5 to determine the interface address and storage address association.) With the scanner stopped and the interrupting interface identified, a bit service routine can gain access to various control latches and status signals in the interface hardware to allow servicing of the bit request.

When enough information has been exchanged between the program and the interface hardware, the program must execute an output instruction to restart the scanner. An Output X'41' instruction is used to reset the interrupt request and start the scanner when the bit received is not the last bit of a character. An Output X'46' instruction sets the character service pending indication in addition to resetting the interrupt request and starting the scanner when character service is required.

Programming Note

The instruction to start the scanner should be executed as early as possible in the bit servicing program so the scanner delay (the time required to address another interface) can be overlapped with bit service processing.

Character Service Interrupt Request

When a bit service routine detects that character service is required, it should execute an Output X'46' instruction to set the 'character service pending' latch, reset the level 2 bit service interrupt request, and start the scanner.

Once the 'character service pending' latch is set, the scanner allows a character service interrupt request to be set when either of the following conditions is satisfied.

1. The scanner passes four enabled high-priority interfaces that do not request bit service.
2. The scanner makes four complete cycles, addressing all interfaces without detecting a bit service request.

When a character service interrupt is set, the address provided by the Input X'41' instruction (interface address) is forced to X'06F0'. This address identifies the interrupt as being caused by a character service request and can be used to direct

Line Number	1	2	3	4	5	6	7	8	9	10
Priority	H	H	L	H	L	H	H	L	L	H
1st Cycle	X	X	X*	X		X	X			X
2nd Cycle	X	X	**	X	X*	X	X			X
3rd Cycle	X	X		X	**	X	X	X*		X
4th Cycle	X	X		X		X	X	**	X*	X
5th Cycle	X	X		X		X	X		**	X
6th Cycle	X	X	X*	X		X	X			X

X = Request honored.

* = Priority circuits prevent further low priority interrupts.

** = Priority circuits allow low priority interrupts.

Figure 6-3. Interfaces Serviced According to Priority

the control program to a character service routine.

The Type 1 Scanner has only one 'character service pending' latch; therefore, the control program should ensure that this latch remains set until the character service routine processes all pending character service requests. The control program should then execute an Output X'44' instruction with byte 1, bit 4 set to 1 to reset the 'character service pending' latch and the level 2 interrupt request.

Programming Note

A character service interrupt request does not stop the scanner; therefore, during the processing of a character, a bit service interrupt request can also be set. However, the request is not honored until an Exit instruction is executed in level 2 character service.

Scanner and Interface Initialization

Initialization is required to place the Type 1 Scanner and the attached interfaces into the proper mode for operation. This must be done any time the Type 1 Scanner has become disabled so that all interfaces have been reset and no interrupts occur.

Conditions such as 'power on reset' and 'initial program load' cause the Type 1 Scanner and the attached interfaces to be disabled. The control program can also cause the same condition by executing an Output X'45' instruction with byte 0, bit 2 set to 1.

In the reset or disabled state, the scanner and all interfaces are reset to a nonoperational state. The scan counter continues to run, but no interrupts are permitted, and all interfaces are set to high bit service priority. A minimum delay of 30 microseconds is required before the program can enable the scanner. The control program can enable the scanner and all the LIB positions by executing an Output X'45' instruction with byte 0, bit 1 set to 1 and byte 0, bits 4-7 set to 0.

Each interface address to be used for communications must be initialized. Once the scanner has been enabled, an individual interface may be enabled or disabled at any time.

When an interface is disabled, normal service interrupts for that interface are prohibited. To enable an interface, the control program must execute an Output X'47' (force bit service) with the associated storage address set in byte 0, bits 6-7 and byte 1, bits 0-3. This causes the scanner to stop when it reaches that interface address and to set a level 2 interrupt request. With the scanner stopped, the interface can be initialized for operation with an Output X'42' (control A) instruction.

The Output X'42' is a control instruction and includes (1) setting the interface mode, (2) selecting high or low priority, (3) selecting start-stop or synchronous/business machine or modem clocking, (4) selecting data rate, and (5) selecting an oscillator. (See Appendix B for Output X'42' bit definitions.) When the mode bits (byte 0, bits 6-7) are set to a nonzero value, the interface is enabled to accept interrupts. (See *Interface Modes of Operation* in this chapter.) The interface is then ready to send or receive data. If the mode is set to 11, an interrupt request is set for the interface at each bit interval when that interface is addressed by the scan counter.

Programming Considerations

When the control program has a record or message to send to a teleprocessing device, it may request a bit service interrupt by executing an Output X'47' instruction containing the storage address associated with that line interface. This causes that interface to set a level 2 bit service request. The next time the scanner services this interface, it stops, and the level 2 interrupt is requested. The bit service routine must then disassemble the character to be sent and execute a series of output instructions to transmit the bits. For each bit to be transmitted, the program must execute an Output X'43' (control B) instruction with byte 1, bit 4 set to 1 to indicate a transmit operation, and byte 1, bit 7 set to the proper bit value (mark or space). The Output X'43' is executed once each time a level 2 interrupt occurs for the particular interface until the complete character is transmitted.

Interface Modes of Operation

The Type 1 Scanner provides four modes of operation for the interface. The modes are set by the combination of bits 6 and 7 of byte 0 in the Output X'42' instruction. The setting of these bits are:

Bit 6	*Bit 7*	*Mode*
0	0	Level 2 interrupts disabled.
0	1	Monitor ring-indicator or data-set-ready.
1	0	Monitor Receive-Data-Space.
1	1	Allow level 2 interrupts.

In the *disabled mode* (00), no interrupts are allowed from the interface until an Output X'47' (force bit service request) is executed or mode bit override (Output X'40') is set. This generates the first bit service interrupt request. When the interrupt occurs, the mode can then be changed to allow interrupts (11) for normal operation. This applies to all transmit and receive operations.

The *monitor ring-indicator* or *data-set-ready mode* (01) allows the scanner to monitor for ring-indicator or data-set-ready on a low-priority interface without

causing an interrupt each bit time. This mode is valid only when the line is set to low priority. When either the ring-indicator lead or the data-set-ready lead becomes active, a bit service interrupt is requested. When the scanner stops on this interface to honor the request, the program should set the mode to allow interrupts (11) for normal operation. When the program has determined that the interface has completed the required action, the mode should be returned to a monitor mode to wait for the next request.

If the interface service priority is high, that interface is disabled from causing a level 2 interrupt in the monitor ring-indicator or data-set-ready mode. A force bit service (Output X'47') or a diagnostic bit service (Output X'44' byte 1, bit 0) is required to override the mode setting and cause a level 2 interrupt.

The *monitor receive-data-space mode* (10) allows the interface to remain idle in a 'mark' state without causing an interrupt each bit time. However, when the line changes to a 'space' level, signaling the start of activity, a bit service is requested. When the scanner stops on this interface to honor the request, the program should set the allow interrupt mode (11) for normal operation. When the program has determined that the interface has completed the required action, the mode should be returned to a monitor mode to wait for the next request.

The *allow interrupt mode* (11) permits interrupt requests to be serviced at each bit interval when the scanner addresses that interface.

The *mode bit override* function is initiated by executing an Output X'40' instruction. Setting the 'mode bit override' latch overrides all mode settings except mode 01 at high-priority. When this latch is set, all interfaces set to any mode other than 01 and to high-priority request a level 2 interrupt each bit-interval regardless of that interface's mode setting. This function allows the control program to force bit service on multiple interfaces without requiring an Output X'47' instruction for each interface address.

Programming Note for a 3705

When in the monitor ring-indicator or data-set-ready mode, the scanner hardware does not service bit service requests. Therefore, a bit overrun/underrun may be indicated when a level 2 interrupt is forced. The bit overrun/underrun indication should be ignored and reset by the control program. When in the monitor for receive data space mode, the hardware services bits while monitoring for a space. Therefore, the control program should always test for a bit overrun/underrun indication.

The Type 1 Scanner hardware services interface bit service requests in accordance with the state of the 'enable scanner' latch and the mode bit setting for each line. When a bit service request is to be ignored, as in the case of mode 01 or 10 conditions not being satisfied, or the line interface or the entire scanner being disabled, the interface service request is reset by the scanner hardware before the next line is scanned. Lines attached through a disabled LIB cannot be serviced by the program or hardware.

Unless its LIB is disabled, a line interface bit overrun indication (Input X'43', byte 1, bit 7) is always valid regardless of the setting of the interface mode bits or the 'enable scanner' latch. When a LIB is disabled, all lines attached through it will overrun until the LIB is reenabled, and indications of overrun should be ignored.

Business Machine Clocks

The Type 1 Scanner must have at least one business machine clock installed and may have as many as four. If modem clocking is used with any of the lines, a business machine clock must be installed in the scanner with a speed less than one-half that of the lowest speed modem clock. Figure 6-4 lists the business machine clocks available.

Clock Speed	*Power On Warm Up Period (Seconds)*
45.5 bps	5
50.0 bps	4
56.89 bps	20
74.2 bps	5
75.0 bps	5
100.0 bps	4
110.0 bps	3
134.5 bps	2
150.0 bps	less than 1
200.0 bps	less than 1
300.0 bps	less than 1
600.0 bps	less than 1
950.0 bps	less than 1
1200.0 bps	less than 1
2000.0 bps	less than 1
2400.0 bps	less than 1

Figure 6-4. Business Machine Clocks and Warm Up Period

Modems attached to a 3705 must provide clock pulses for line speeds above 2400 bps. Some line sets can operate with a business machine clock or a modem clock and some can operate only with a business machine clock. Refer to the *Introduction to the IBM 3704 and 3705* manual for a description

of the individual LIB and line set types and their clocking requirements.

The installed business machine clock used for a given line is selected under program control by executing an Output X'42' (control A) instruction with byte 1, bits 6 and 7 set to indicate the desired clock. Figure 6-5 shows the proper setting of the oscillator select bits to assign an installed oscillator to a given interface.

Bit 6	7	*Selected Business Machine Clock*	
0	0	Lowest speed clock	(OSC0)
0	1	Next higher speed clock	(OSC1)
1	0	Next higher speed clock	(OSC2)
1	1	Highest speed clock	(OSC3)

Figure 6-5. Type 1 Scanner Business Machine Clock Selection

No business machine clock is selected if the Output X'42' bits are set to select an uninstalled oscillator (for example, bits 6 and 7 set to 11 when only two or three oscillators are installed).

Every interface must have a business machine clock assigned whether it is specified to be business machine or modem clocked. For autocall interfaces and for line interfaces that are to use modem clocking, the assigned business machine clock is used to ensure that the interface is periodically accessed. The lowest speed oscillator is always used for an autocall interface.

The oscillator select bits are set to 0 by a reset to the scanner. Therefore, the lowest speed clock is initially selected, and unless an Output X'42' is executed to select another clock for a given interface, the lowest speed clock is used.

After a power-on reset occurs, there is a warm-up period associated with the different clocks. (Refer to Figure 6-4.) During this warm-up period, a business machine clock cannot provide bit service requests.

Programming Notes

1. The oscillator select bits for a line interface can be changed without causing a switched network connection to be broken, if *data terminal ready* is up when the Output X'42' is executed.
2. The business machine clock selected for a modem-clocked line interface must be less than one-half the rate of the modem clock.

Autocall Interface Operation

Programming the Type 1 Scanner for an autocall interface is essentially the same as for a line interface. The major difference is in the bit settings of Input instructions X'42' and X'43' and Output instructions X'42' and X'43'. Appendix B defines the affected instructions and the differences in the bit definitions.

Input/Output Instructions

The Type 1 Communication Scanner and the line interface bases it supports are controlled through the use of input and output instructions. These instructions allow the program to (1) control the attached interfaces, (2) send and receive data, and (3) monitor the status of the scanner and line interfaces to ensure proper operation. Appendix B defines the bits within each input and output instruction.

Certain input and output instructions should be executed only when the scanner is stopped. If an Input X'41', X'42', or X'43' instruction is executed when the scanner is running, the result in the general register specified in the instruction pertains to the interface addressed at the time of execution. However, there is no way to determine which interface was addressed. If an Output X'41', X'42', X'43' is executed when the scanner is running, the mode or status of an unknown interface may be changed, and an error condition may result. Input X'41' and X'43' may be executed when a character service interrupt is pending with the scanner running.

Input Instructions

Four functional input instructions (Input X'41', X'42', X'43', and X'44') are used with the Type 1 Communication Scanner. With these instructions, the control program receives data from the lines, monitors the status of the lines, and is informed of any error conditions. Execution of Input instructions X'40', X'45', X'46', and X'47' sets the bits in the general register to zero. (Appendix B defines the bits within each input instruction.)

Input X'41' (Interface Address): This instruction loads a general register with the storage address associated with the interface the scanner is addressing. Each time the scanner stops because of a bit service interrupt, this input may be issued to determine which interface caused the request.

If the level 2 interrupt is the result of a character service request, the address loaded into the register will be X'06F0'. This address identifies the interrupt as being caused by a character service request and can be used to direct the control program to a character service routine.

Programming Note

An Input X'41' instruction should normally be the first scanner instruction executed in program level 2.

Input X'42' (Control A): This instruction loads a general register with the 'control A' information as set by an Output X'42' instruction. An Input X'42' instruction is used to check the state of the control A bits. It is a direct bit-for-bit reflection of the last Output X'42' instruction to that interface.

The Input X'42' instruction should be executed only when the scanner is stopped.

Input X'43' (Control B/C): This instruction can be executed in either a bit service or a character service routine. However, an Input X'41' instruction must be executed between the level 2 interrupt and execution of the Input X'43' instruction.

Executing an Input X'43' instruction as a result of a bit service interrupt loads a general register with the control B/C information. Data received from the interface, along with error information and line status, is set for the interface that caused the service request. If an Input X'43' is executed as the result of a character service interrupt, the specified general register (R) will contain X'0000'.

An Input X'43' instruction *must not* be executed if there is not a bit service or character service level 2 interrupt pending. Execution without an interrupt pending may cause a CCU In/Out level 1 check due to incorrect input parity.

Programming Note

This instruction cannot be executed immediately following an Output X'43' for feedback checking. However, it can be executed after Output X'43' to obtain other status indications.

Input X'44' (Status Register): This instruction loads a general register with the contents of the Type 1 Scanner status register. This register contains (1) indications of level 1 check interrupt requests from the scanner, (2) the scanner enable/disable condition, (3) character service pending information, and (4) mode bit override and override remember indications.

Output Instructions

Eight output instructions are used with the Type 1 Communication Scanner to control its operation and data transfer. (Appendix B defines the bits within each output instruction.)

Output X'40' (Set Mode Bit Override and Override Remember): This instruction sets the 'mode bit override' latch and the 'override remember' latch. The function of the 'mode bit override' latch is described in the *Interface Modes of Operation* section of this chapter. The 'override remember' latch performs no hardware function but is available for use by the control program. Since this instruction performs a function, the bit settings of the register are ignored.

Output X'41' (Reset Bit Service Level 2 Request and Start Scanner): This instruction resets the level 2 bit service interrupt request and starts the scanner. The bit service routine should issue this output after determining that all the information required to service the interface has been obtained or sent. An Output X'41' instruction should be the last instruction executed in the level 2 routine before exiting to a lower priority level for continued bit service processing. Since this instruction performs a function, the bit settings of the register are ignored.

The Output X'41' instruction should be executed only when the scanner is stopped.

Output X'42' (Control A): This instruction sets the mode of an interface according to the bit setting of the specified general register. In addition to setting the mode, it can also set service priority, clocking, data rate, oscillator selection, and diagnostic mode for the interface.

The Output X'42' instruction should be executed only when the scanner is stopped.

Output X'43' (Control B): This instruction sets the interface into a transmit or receive mode and can activate or deactivate various line and autocall-interface leads as required. When the line is transmitting, byte 1, bit 7 of the general register must be loaded with the mark or space to be sent to the interface terminal.

The Output X'43' instruction should be executed only when the scanner is stopped.

Output X'44' (General Control): This instruction sets or resets the diagnostic bit service request and resets (1) the mode bit override and override remember, (2) character service pending, and (3) outstanding error indications.

Output X'45' (Scanner Control): This instruction enables or disables the scanner and/or the line interface bases (LIBs). Normally, this instruction is used only during initialization or when an error has occurred that requires a LIB to be disabled.

Programming Note

Output X'45' can disable interrupts from any LIB attached to the Type 1 Scanner. This can be particularly useful when a bit-clock error occurs in a LIB and causes a level 1 interrupt. The failing LIB, including all lines attached to that LIB, can be disabled to prevent further error conditions while the remaining LIBs continue normal operation.

Output X'46' (Set Character Service Pending, Start Scanner, and Reset Level 2 Bit Service Request): This instruction is normally used at the end of bit service processing when character service is required for that interface. It sets the 'character service pending' latch to signal the scanner that a character service interrupt is required. The instruction then resets the level 2 bit service interrupt request and starts the scanner. Since this instruction performs a function, the bit settings of the register are ignored.

The Output X'46' instruction should be executed only when the scanner is stopped.

Output X'47' (Force Bit Service Request): This instruction forces a bit service interrupt request for the interface address that is specified in the general register. This instruction stops the scanner on an interface and requests a bit service interrupt so that the program can enable the interface or access it to transmit a bit.

Programming Notes

1. Forced bit service cannot be stacked. If an Output X'47' is executed before the previous Output X'47' has been serviced, the second address overlays the first.
2. When bit service is forced to a line interface attached to a LIB that has been disabled, the line adapter is not accessed even though the scanner is stopped at that interface address. Also, except for the mode bits and the feedback check bit, all bit settings in Inputs X'42' and X'43' may be invalid. The execution of Output X'42' or X'43' will either be ineffective or cause scanner checks.

Error Indications

Error conditions detected by the Type 1 Scanner are in one of two groups, depending on the type of error and the impact on the overall system operation. The first and most critical group (level 1 errors) causes a level 1 interrupt request and must be handled with high priority because the error may involve many lines. The second group (interface errors) can be handled at a lower-priority interrupt level because the errors have less system impact. The following paragraphs describe these errors and their detection.

Level 1 Errors

Failures in the Type 1 Communications Scanner or in a line interface base can affect all communication lines attached to the controller or at least a group of lines within a particular LIB. The detection of one or more of these failures by the hardware check circuits causes a Type 1 Scanner L1 interrupt request (Input X'76', byte 0, bit 1). The level 1 interrupt routine, after determining that the interrupt request came from the Type 1 Scanner, should execute an Input X'44' (status register) instruction to further identify the error.

The error condition that caused a level 1 interrupt is indicated in byte 1, bits 2-7 of the Type 1 Scanner status register (Input X'44'). Bits 2-5 correspond to LIB positions 1-4 and are turned *on* respectively as a result of a LIB bit clock parity error. Bit 6 is turned *on* by the detection of a LIB select error. Bit 7 is turned *on* by a parity error on the CCU outbus, which is an internal interface between the Central Control Unit and the Type 1 Scanner. See Appendix B, Input X'44' for a description of these bits and the error conditions.

If the level 1 interrupt routine can handle the error condition and processing can continue, the routine should then issue an Output X'44' instruction with byte 1, bit 5 on to reset the level 1 request. When the error is permanent, the LIB can be disabled via an Output X'45' so that processing can continue on the remaining LIBs.

Interface Errors

Line interface errors indicate intermittent or permanent internal logic faults and most problems with communication facilities. The failure is detected at the interface level, but if failures are detected in a group of interfaces, the fault may be in either the (1) LIB logic, (2) Type 1 Scanner logic, (3) CCU input/output mechanism, or (4) program logic.

Interface errors normally are not critical enough to interrupt the entire system. Therefore, the Type 1 Scanner does not generate a level 1 interrupt when this type of error is detected. Instead, certain bits are set in the control B/C register to indicate the failure. By issuing an Input X'43' instruction when an interface requests service, the program can test for error conditions on that line without disrupting normal processing.

Byte 0, bit 2 of the Input X'43' instruction is a partial summary of interface errors. This interface-error summary bit is set *on* whenever the Type 1 Scanner detects (1) a feedback check, (2) bit overrun or underrun, or (3) that the 'data set ready' line is not up. If the control program checks this bit first, considerable time can be saved in detecting errors.

A feedback check (byte 0, bit 1) is set on when the hardware circuits detect that the bit actually sent to the line set does not compare to the bit as it appears in byte 1, bit 7 of Output X'43'. This error is also set if the interface bit service failed to be reset. A feedback check must be reset before the scanner can be restarted.

Bit overrun/underrun (byte 1, bit 7) is set when the Type 1 Scanner determines that a bit has been lost

because of improper timings between the control program and the bit rate used by an interface.

Telegraph Echo Check (byte 1, bit 4) is set when the telegraph interface detects that an echo check has occurred.

In addition to monitoring byte 0, bit 2 of Input X'43', which is a summary of several error conditions, the bit servicing routine should also monitor byte 1, bit 3 of the same input. Monitoring these bits provides a higher level of security on switched lines. This only applies for start-stop, half-duplex units that require duplex facilities (for transmission interruption ability).

Diagnostic Functions

The Type 1 Communication Scanner provides for three internal diagnostic functions: (1) diagnostic bit service, (2) diagnostic wrap mode, and (3) IBM modem wrap test. These tests run under the control of the scanner program and can provide online testing as described in the following sections. Diagnostic bit service can be issued to an autocall interface, but the diagnostic wrap and the modem wrap test cannot.

Diagnostic Bit Service

The Type 1 Scanner diagnostic bit service provides a means for forcing level 2 bit service interrupt requests. This facility allows the control program, through the use of a diagnostic routine, to exercise program and/or hardware functions in a test environment. The diagnostic routine performed must be part of the control program. Diagnostic bit service causes continuous level 2 bit service requests for all 64 interface addresses whether the interface is used or not. An Output X'44' instruction with byte 1, bit 0 set to 1 indicates the diagnostic bit service function. When an Output X'44' is executed with this bit off (0), the diagnostic requests are terminated.

Diagnostic Wrap Mode

The Type 1 Scanner diagnostic wrap provides a means of testing and locating defects in the line control logic and in the line-interface transmit and receive logic. Diagnostic wrap can be performed online without affecting normal program operation or the lines not in diagnostic mode. The test requires one line interface to act as a transmit line and one or more line interfaces to act as receive lines. Any line can be a transmit or a receive line; however, only one diagnostic wrap transmit line may be present at any one time.

Diagnostic wrap is initiated by executing an Output X'42' instruction to each line to be tested with the following bits set in the register specified by the R operand.

Byte 0, bits 6-7: (Mode Bits 1 and 2)—These bits select the appropriate bit setting for the desired mode. See *Interface Modes of Operation* in this chapter for the mode options.

Byte 1, bit 0: (Bit Service Priority)—This bit selects the appropriate service priority. See Output X'42' for service priority options.

Byte 1, bit 1: (Diagnostic Mode)—This bit must be 1.

Byte 1, bit 2: (Data Terminal Ready)—This bit must be 0.

Byte 1, bit 3: (Synchronous Clock)—This bit must be set according to the type of communication line to be tested. A 1 is set in this position for binary synchronous lines, and a 0 for start-stop lines.

Byte 1, bit 4: (External Clock)—This bit must be 0.

Byte 1, bit 5: (Data Rate Select)—This bit may be either 0 or 1. However, the same type line sets must use the same data rate.

Byte 1, bits 6-7: (Oscillator Select 1 & 2)—These bits select an available line oscillator (business machine clock). For bit clock options, see *Business Machine Clocks* in this chapter. All wrap-test lines must select the same oscillator.

After the Output X'42' instructions are executed, the affected lines can be used through any sequence of point-to-point or multipoint operations.

Diagnostic wrap mode simulates 'data set ready' as active. 'Clear to send' is simulated active if 'request to send' is active.

Programming Notes

1. Only one line may be in a diagnostic wrap transmit state at any given time during the operation.
2. The line used for transmit should be the last line to be issued the Output X'42' instruction.

Modem Wrap Test

Modem wrap test tests the scrambler circuits of IBM 3872, 3874, and 3875 modems under program control. The modem test can be performed online without affecting the normal operation of other lines. This test may also be performed simultaneously on any or all lines for which the test function is initiated.

Modem wrap test is initiated by executing an Output X'42' (control A) instruction with the following bits set in the register specified by the R operand to each line to be tested.

Byte 0, bits 6-7: (Mode Bits 1 and 2)—These bits select the appropriate bit setting for the desired mode. See *Interface Modes of Operation* in this chapter for mode options.

Byte 1, bit 0: (Bit Service Priority)—This bit selects the appropriate service priority. See Output X'42' for service priority options.

Byte 1, bit 1: (Diagnostic Mode)—This bit must be 1.

Byte 1, bit 2: (Data Terminal Ready)—This bit must be 1 to cause the 'data terminal ready' latch to be set in the line interface. When this bit, together with diagnostic mode, is set on, the modem wrap test is performed instead of the diagnostic wrap test.

Byte 1, bit 3: (Synchronous Clock)—This bit must be 0.

Byte 1, bit 4: (External Clock)—This bit must be 1 if the modem provides the clock, and it must be 0 if the modem does not provide the clock.

Byte 1, bit 5: (Data Rate Select)—This bit may be either 0 or 1.

Byte 1, bits 6-7: (Oscillator Select 1 and 2)—These bits must select an internal oscillator whose speed is less then one-half the clock speed if modem clocking is used. If modem clocking is not used, the internal oscillator must match the modem speed. For the proper setting, see *Business Machine Clocks* in this chapter.

Chapter 7: Type 2 Communication Scanner

This chapter is intended to give the reader a basic understanding of the operation of the Type 2 Communication Scanner and the requirements necessary to program the scanner.

The Type 2 Communication Scanner (1) scans the interface addresses assigned to the LIB positions it supports, (2) performs character assembly/ disassembly, (3) provides character buffering, and (4) causes program interrupts when character service is required.

Up to four Type 2 Communication Scanners can be installed in the 3705 (Type 2 Scanner-1 through Type 2 Scanner-4). Type 2 Scanner-1 supports attachment of up to four LIBs with 64 half-duplex (HDX) lines. Type 2 Scanner-2, Type 2 Scanner-3, and Type 2 Scanner-4 can each support attachment of up to six LIBs with 96 HDX lines; thus, up to 352 HDX lines can be attached to the 3705 using four Type 2 Scanners. The Type 2 Scanners can be installed with either the Type 1, Type 2, or Type 3 Channel Adapter features.

The 3704 is limited to one Type 2 Scanner, which is operationally equivalent to and program compatible with the 3705 Type 2 Scanner. The 3704 Type 2 Scanner supports one Type A1 LIB, which provides a maximum of ten lines. Additional capability is available that enables the scanner to support two LIBs and a maximum of 26 half-duplex lines. These LIBs can be in any combination (except two Type 1 LIBs).

The number of lines supported depends on:

- How lines are used.
- Line disciplines.
- Mix of line speeds.

For information about LIBs and their capacities, refer to the *3704 and 3705 Introduction* manual.

Operation and Data Flow

The interface addresses for all installed Type 2 Communication Scanners in the 3705 are generated from a common Type 2 Attachment Base. The 3704 does not have a Type 2 Attachment Base. All necessary hardware functions that would be provided by the Type 2 Attachment Base are integrated within the 3704 Type 2 Scanner. Figure 7-1 shows the basic operation of the Type 2 Scanner. A continuously running *scan counter* in the attachment base places the generated interface address on an address bus that goes to all scanners simultaneously. This address can be modified, under program control, by the attachment base or the scanner.

The interface address is then used to address an interface control word (ICW), which is loaded into the ICW work register where the scanner hardware determines if any action is to be performed for that interface. If no action is required, the ICW is replaced in local store and the next addressed ICW is loaded into the work register. If the scanner determines that program intervention is required, it requests a level 2 interrupt and loads the interface address into an interrupt priority register.

When the level 2 interrupt actually occurs, the address in the highest-priority interrupt priority register that is active is loaded into the attachment buffer address register (ABAR) and is then available to the control program along with the ICW in the ICW input register.

Type 2 Scanner Registers

The Type 2 Scanner contains various hardware registers that are used to store and pass information and data within the scanner and between the scanner and the control program. Some of these hardware registers are available to the control program as external register addresses through input and output instructions. The external registers required for control program access are described in the following paragraphs.

Local Storage

Each Type 2 Scanner contains a local storage array to store the interface control words when not being used by the scanner hardware or the control program. This storage array holds 96 control words of 48 bits each (46 information bits and 2 parity bits). The 3704 local storage is limited to 16 interface control words (only 10 are used). If the scanner supports two LIBs, the 3704 local storage is increased to 32 interface control words (a maximum of 26 can be used).

ICW Work Register

The Type 2 Scanner control logic uses the ICW work register to access, monitor, and modify an interface control word (ICW). This register is loaded each time an ICW is read out of local storage.

ICW Input Register

The control program uses the ICW input register for access to the interface control words. This register is loaded from the ICW work register and reflects the status of the ICW at the time when it was read out of local storage.

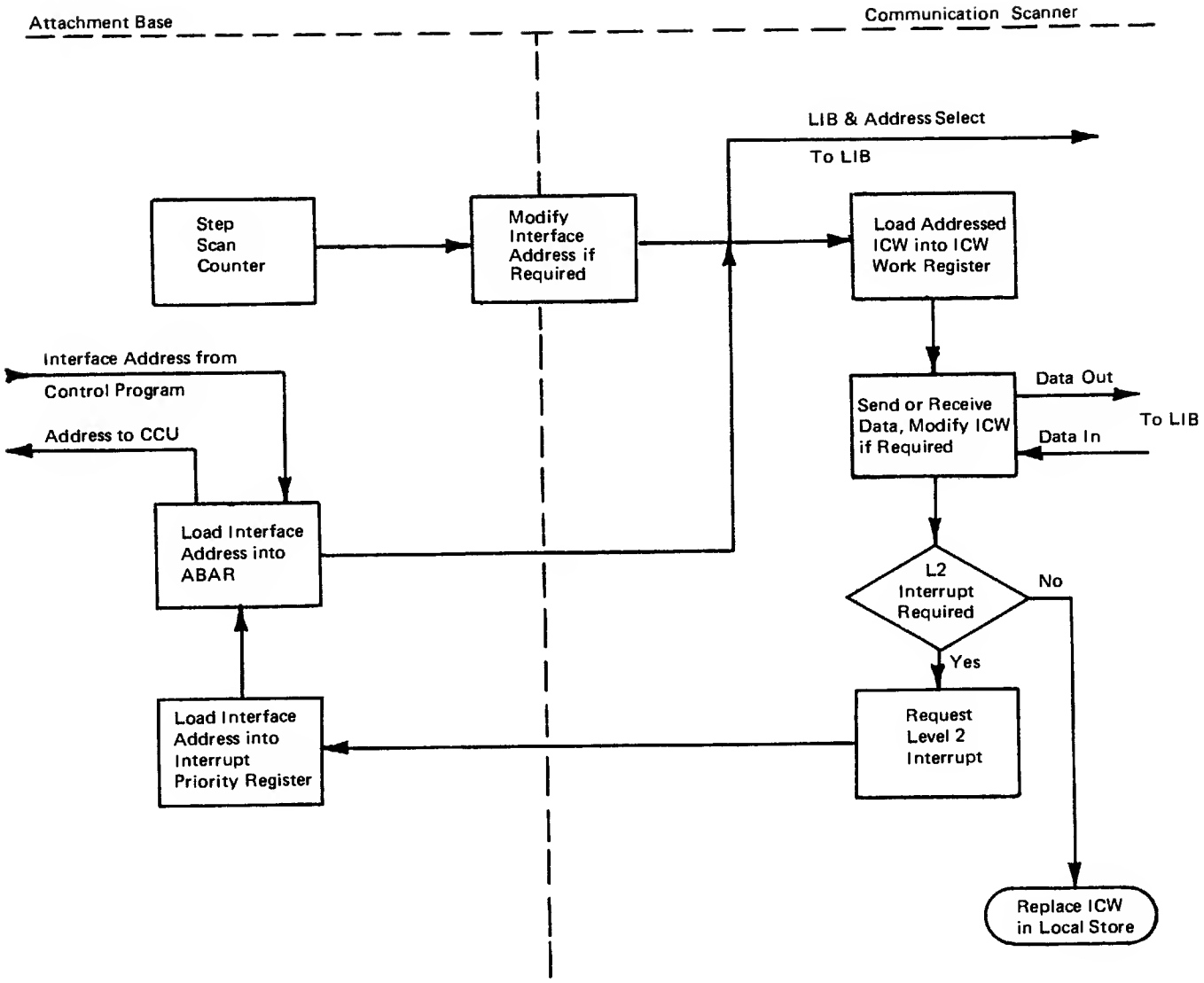


Figure 7-1. Type 2 Communication Scanner Operation

Attachment Buffer Address Register

The attachment buffer address register (ABAR) is physically located in the Type 2 Attachment Base and supplies the interface addresses to the control program. See *I/O Programming Considerations* in this chapter for a description of loading the ABAR.

Programming Note

The ABAR must be initialized by an Output X'40' instruction with an interface address associated with an installed Type 2 Scanner. The Output X'40' must be executed after the controller is powered on and before any other input or output instructions to the scanner are executed.

Display Register

The display register is a temporary storage register that can contain interface control information that the program can use. If bit 38 (display request) of an interface control word is *on*, control information for that interface is loaded into the display register each time that interface is scanned. The control program can then obtain this information by executing an Input X'46' instruction.

There is only one display register for each Type 2 Scanner; therefore, only one ICW at a time should have its display request bit set to 1. Otherwise, the control program cannot determine which interface was the last one to cause the display register to be loaded.

Type 2 Scanner Addressing

The Type 2 Communication Scanner scan-addressing and program-addressing mechanism is controlled by the Type 2 Attachment Base. The attachment base generates the basic scan address and places it on a 'line address bus' for availability to all installed Type 2 Communication Scanners. Refer to the *Interface Addressing* section of Chapter 3 for a detailed discussion of each interface address bit.

Scan Addressing

For scan addressing, an interface in each installed Type 2 Scanner is addressed simultaneously. Each scanner derives the address of the interface it is scanning from the 8-bit address that the Type 2 Attachment Base places on a 'line address bus'. The line address bus is an internal bus that carries the scan address from the attachment base to each of the communication scanners. This address, as modified by each scanner (see upper scan limit), is used not only to select a particular interface but also to address the associated interface control word (ICW) that the scanner maintains in local storage. (See *Interface Control Word* in this chapter.) The Type 2 Scanner examines this ICW and, when an interface service function is required, performs that function; or, when a character service requires programming action, the Type 2 Scanner signals the attachment base that it needs a program level 2 interrupt.

Scan Counter

The 3705 Type 2 Attachment Base scan counter output provides the basic scan addresses for each Type 2 Scanner. If the scan counter output is not modified, each Type 2 Scanner sequentially scans 96 interface addresses. Under these circumstances, the Type 2 Scanner cannot handle line speeds higher than 4800 bps without having the possibility of undetected bit overrun/underrun conditions. However, the ability to substitute some interface addresses (address substitution) and set a limit on the number of interfaces scanned (scan limit), greatly extends the capability of handling higher-speed lines. These mechanisms cause the scan counter output to be modified to allow certain interface addresses to be scanned at a different rate.

The scan counter in the 3704 continuously steps through 16 different interface addresses at a rate of 1.2 microseconds per address and completes one scan of all addresses in 19.2 μsec. However, because the LIB Type A1 can support only ten lines, interface addresses 1, 3, C, D, E, and F are not available for use. Addresses 1 and 3 are modified to addresses 0 and 2 respectively. This allows line speeds up to 56,000 bps to be scanned on addresses 0 and 2.Interface addresses C, D, E, and F are ignored.

If the Type 2 Scanner supports two LIBs, the scan counter steps through 32 different interface addresses during a 38.4 microsecond scan period. With this expanded capability, all interface addresses (0-F) of both LIBs are scanned. Although 32 different addresses are available, the maximum number of lines supported is 26.

Upper Scan Limit

The Type 2 Scanners have an upper scan limit that can be set and reset under program control by an Output X'42' instruction. Each scanner maintains its own upper scan limit and is independent of the limits set by any of the other installed scanners. Based on the state of its 'upper scan limit' latches, a Type 2 Scanner may modify the 'scan counter' output from the Type 2 Attachment Base in such a way as to limit the number of interface addresses scanned.

The actual modification of the scan address is done by the Type 2 Scanner hardware as the line address bus enters the scanner from the attachment base.Figure 7-2 shows the number of interfaces scanned and the LIB position affected for each setting of the upper scan limit. When the upper scan limit is set to any value other than binary 00, the scanner modifies the addresses above the limit to start at the first address again. For example, if the upper scan limit is set to allow only 16 interface addresses to be scanned, the address is modified to scan the first address again when the scan counter output to that scanner reaches the 17th address. This decreases the period of time between successive scans of the remaining interface addresses to accommodate higher-speed lines. In this case, the scanner with an upper scan limit of binary 11 scans the first 16 interfaces four times in the same period of time as another scanner with no limit scans 96 interfaces. Unless the 3704 scanner can support two LIBs, modification of the upper scan limit is restricted to binary 01 in byte 1, bits 6 and 7 of Output X'42'. A binary 01 sets the limit to eight; any other value sets the scan limit to 16.

If the 3704 scanner supports two LIBs, a binary 11 in bits 6 and 7 causes 16 lines to be scanned twice during the scan period (38.4 microseconds). A binary 01 causes 8 lines to be scanned four times during the same scan period. Values of binary 00 and 10 allow all 32 addresses to be scanned (see Figure 7-2).

Upper Scan Limit (Note 1)	*Number of Interfaces Scanned*	*Interface Addresses Scanned*	*Interface Addresses Not Scanned*	*Scan Period (μsec)*		
3704						
00	32 (Note 2)	Addr 0-F,LIB 1-2	-	38.4		
10	32 (Note 2)	Addr 0-F,LIB 1-2	–	38.4		
11	16	Addr 0-F,LIB 1	Addr 0-F,LIB2	19.2		
01	B	Addr 0-7,LIB 1	Addr 0-F,LIB2 and Addr 8-F, LIB 1	9.6		
				(Note 4)	(Notc 5)	(Note 6)
3705						
00	96 (Note 3)	Addr 0-F,LIB 1-6	–	153.6	192	172.8
10	48	Addr 0-F,LIB 1-3	Addr 0-F,LIB 4-6	76.B	96	86.4
11	16	Addr 0-F,LIB 1	Addr 0-F,LIB 2-6	25.6	34	28.B
01	8	Addr 0-7,LIB 1	Addr 8-F,LIB 1 and Addr 0-F,LIB 2-6	12.8	16	14.4

Notes:
1. Set by Output X'42' byte 1, bits 6-7
2. Applies only for a 3704 Type 2 Scanner with the capability of supporting two LIBs.
3. Scanner-1 contains 96 address but only used the first 64.
4. Scan periods for a 3705-I only (1.2 microsecond CCU clock).
5. Scan periods for a 3705-II having a 1.0 microsecond CCU clock.
6. Scan period for a 3705-II having 900 nanosecond CCU clock.

Figure 7-2. Upper Scan Limit

Address Substitution

The output of the scan counter can be modified to cause certain addresses assigned to LIB position 1 to be substituted on the 'line address bus' in place of normal scan addresses. As a result, those addresses that are substituted are scanned by the Type 2 Scanner more frequently than the other addresses. Address substitution affects all installed scanners in the same manner. (Address substitution is ignored in the 3704 unless the Type 2 Scanner can support two LIBs.) When operating with address substitution, each scanner in the 3705 scans the substituted address or addresses, every 12.8, 14.4, or 16.0 microseconds (9.6 microseconds for a 3704 Type 2 Scanner with a two-LIB capability), because address substitution occurs every eighth time the scan counter changes state. This allows the substitution address or addresses in each scanner to handle higher line speeds independent of the state of the scan limit.

Address substitution is controlled by a four-bit register called the substitution control register. The bits of this register may be set under program control by Output X'41' byte 1, bits 2, 3, 4, and 5. Each bit of this substitution control register corresponds to one of four substitution addresses assigned to LIB position 1.

Programming Note

Any combination of the four substitution control register bits may be turned *on* to produce the desired substitutions. If address substitution is not used, Output X'41' must be executed with byte 1, bits 2 through 5 *off* in the register specified by the R operand.

When a given substitution control register bit is on, a corresponding address is substituted on the 'line address bus' every eighth time the scan counter changes state. Combinations of bits on in the substitution control register result in fixed-address substitution for each corresponding bit. Figure 7-3 shows which address is substituted and which addresses are not scanned as a result of that substitution when the different substitution control register bits are on.

Output X'41' Byte 1, Bit:	*Fixed Address Substituted in Each Type 2 Scanner If Substitution Bit ON*	*Addresses Not Scanned In Each Type 2 Scanner If Substitution Bit ON*
2	Adr 0 LIB position 1	Adr E in LIB positions 1-6 Adr F in LIB positions 1-6
3	Adr 2 LIB position 1	Adr C in LIB positions 1-6 Adr D in LIB positions 1-6
4	Adr 4 LIB position 1	Adr A in LIB positions 1-6 Adr B in LIB positions 1-6
5	Adr 6 LIB position 1	Adr 8 in LIB positions 1-6 Adr 9 in LIB positions 1-6

Figure 7-3. Address Substitution Control

Program Addressing

Various input and output instructions exist that allow the program to control the operation of the Type 2 Scanners, Type 2 Attachment Base, and the individual interfaces.

However, before the program can examine or modify fields in a interface control word (ICW) associated with a particular interface, the address of that interface, must be placed in the attachment buffer address register (ABAR) of the attachment base. Similarly, before the program can access certain registers in a particular Type 2 Scanner or perform control functions in that Scanner, the interface address in the ABAR must be one of those assigned to that scanner. Two events can cause the contents of the ABAR to be changed: (1) a program level 2 interrupt, and (2) execution of an Output X'40' instruction.

When a program level 2 interrupt occurs, the contents of the ABAR are automatically set by the Type 2 Attachment Base with the interface address from the highest interrupt priority register that is occupied. The control program can determine which interface address is in the ABAR by executing an Input X'40' instruction. The program can then examine and/or modify fields in the ICW associated with this interface. In the other interrupt program levels (1, 3, and 4), the program may find it necessary to gain access to the ICW associated with a specific interface. By executing Output X'40' under such circumstances, the program can set the ABAR according to the interface address in the register specified by the R operand.

To avoid conflicts with the automatic mechanism that sets the ABAR when a program level 2 interrupt occurs, programs executing at program level 3 or 4 should mask program level 2 interrupts before executing Output X'40'. (Program level 1 should save the value of the ABAR, change it to select the desired interface, and then restore the original value to the ABAR.) If more than one program level is likely to execute an Output X'40', additional interlocking conventions must be established within the control program.

Interface Control Word (ICW)

The Interface Control Word (ICW) provides the normal means by which the control program communicates with the Type 2 Scanner and the interface hardware.

The ICW is made up of 46 information bits and 2 parity bits and is physically located in the scanner local storage. Each scanner contains one ICW for each possible interface. However, even though the scanner contains the maximum number of ICWs (32 for a 3704, 96 for a 3705), only those ICWs associated with an attached and active interface are used.

ICW Access

The Type 2 Scanner hardware gains access to an ICW by using the interface address provided by the interrupt priority register in the Type 2 Attachment Base. When the level 2 interrupt occurs, the address from the interrupt priority register is loaded into the attachment buffer address register (ABAR). The program can then execute an Input X'40' instruction to get the storage address associated with the interface. Once the control program obtains the interface address, it has access to the various fields of the ICW through input and output instructions.

Programming Note

ICW access at program level 3 or 4 should be performed only when program level 2 interrupts are masked off; otherwise, the result is unpredictable.

ICW Modification

Program access to the various fields in the ICW is through the use of input and output instructions. When the Input X'44', X'45', and X'47' instructions are executed, the ICW bits assigned to those inputs are placed in the register specified in the R operand. See Appendix B for the input/output instruction bit definitions.

The information obtained by the input instructions comes from the ICW input register. There is one ICW input register in each communication scanner. This register is automatically loaded from the ICW work register when a level 2 interrupt occurs or when an Output X'40' instruction is executed in any program level other than level 1 or 2.

The ICW input register does not necessarily reflect the current state of the ICW associated with the interface address in ABAR. The actual ICW may have been modified by the Type 2 Scanner during scan addressing after the ICW input register was set.

Also, the actual ICW may have been altered by the execution of an Output X'43', X'44', X'45', X'46', or X'47' instruction. Subsequent input instructions do not include these alterations because the ICW input register had been set by a previous Output X'40' instruction or Type 2 Scanner level 2 interrupt. In the event that an output instruction and scan addressing both occur during the same scan cycle, the output instruction is executed first; then the scanner performs its modification, if needed. This ensures that the latest modifications to the actual ICW will be included during the next scan addressing operation.

Refer to *Interface Control Word Format* in this chapter for a complete description of the individual ICW fields and the I/O instructions associated with each field.

Programming Note
Since the interface control words are asynchronously interrogated and modified by both the scanners and the control program, caution should be observed to ensure the ICW integrity when the program issues an output instruction. The Type 2 Scanner cannot check whether the control program has modified the ICW correctly. Therefore, errors in the modification itself may be difficult to isolate. To prevent control program modifications to the ICW (via output instructions) from being destroyed by the scanner, program modifications are not permitted during that portion of a scan when the Type 2 Scanner fetches, modifies, and restores the ICW for the line being scanned.

Interface Control Word Format
The following paragraphs describe the ICW fields and their bit meanings. (See Figure 7-4.) For descriptions of ICW fields and their bit meanings when used for Synchronous Data Link Control (SDLC) lines, refer to the SDLC section of this chapter.

ICW Bits 0-7 (Secondary Control Field): The secondary control field (SCF) is used as a sense, status, and operation modifier field between the control program and the communication scanner. Bits 0-4 are set by the Type 2 Scanner hardware according to the conditions described below. Bits 6 and 7 are program controlled. This field may be tested by using the Input X'44' instruction. An Output X'44' instruction is used to reset bits 0-3 and 5 and to set and reset bits 6 and 7. Refer to Appendix B, *Input/Output Instruction Bit Definitions.*

Bit 0 — Stop Bit Check/Receive Break: For start-stop lines in PCF state X'7', the receive data bit buffer is checked after each character is received. If the bit buffer contains a (space) instead of a (mark), the Type 2 Scanner signals this condition to the control routine by setting this bit.

For start-stop lines during transmit operations (PCF state X'9'), the 'receive data' line is checked for a space (0) condition every time the first bit of a character is placed in the transmit buffer. If a space condition is detected, this bit is set on. When the control program detects that this bit is set for two consecutive characters, it should be interpreted as a *receive break* signal.

If this bit is 1, the service request interlock (ICW bit 1) will be 0.

For autocall interfaces and binary synchronous line interfaces, this bit is 0.

Bit 1 — Service Request Interlock: This bit is set when the Type 2 Scanner detects that data transfer or control servicing is required between the control program and the 'parallel data field'. The control program must reset this bit after the interrupt is honored and all bits or bytes of the ICW have been modified. If this bit is already set when the scanner is prepared to set it on, and the PCF state is X'7' through X'A', a character overrun/underrun flag is set (ICW bit 2).

If this bit is 1, the stop bit check/receive break, character overrun/underrun, and modem check bits are 0.

Programming Note
The control program should reset the service request interlock before setting the PCF state to monitor modem or autocall unit control lines.

Bit 2 — Character Overrun/Underrun: This bit is set when the Type 2 Scanner attempts to set the service request interlock (ICW bit 1) and finds it already set. This error is normally caused by an instantaneous peak overload situation. Errors of this type should not occur in the average installation and should occur only infrequently in high throughput installations.

If a character overrun occurs, the next character received is placed into the PDF field overlaying the character that was to have been serviced. Thus, if an overrun occurs, a character is lost.

In the event of an underrun, the same character is transmitted until the program changes the PDF field to another character or the primary control field is changed from the transmit state.

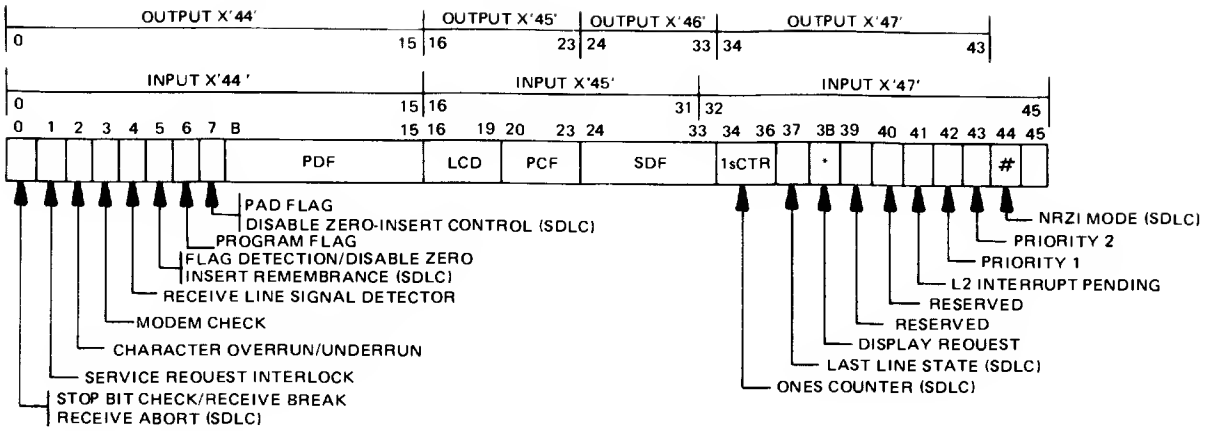
If this bit is 1, the service request interlock (ICW bit 1) is 0.

Bit 3 — Modem Check: During each bit interval (bit service time), the Type 2 Scanner checks the line interface for the proper modem conditions. This bit is set to 1 to indicate the following conditions:

1. The 'data set ready' line is inactive when the PCF field of the ICW is in states X'5', X'7', X'8', X'9', X'A', X'B' or X'D'.
2. The 'clear to send' line is inactive when the PCF field of the ICW is in states X'9', X'A', X'B', or X'D'.
3. A TTY echo check has been detected.
4. The 'receive line signal detect' line is inactive, the interface is start-stop, ICW bit 7 (pad flag) is on, and the PCF of the ICW is in state X'7' (receive).

If this bit is 1, the service request interlock (ICW bit 1) is 0.

Bit 4 — Received Line Signal Detector: This bit is set when the line interface indicates that the data communication equipment is receiving a carrier signal that



PRIMARY CONTROL FIELD (PCF)

HEX	START-STOP	BSC	SDLC	AUTOCALL
0	NO-OP	NO-OP	NO-OP	IDLE
1	SET MODE	SET MODE	SET MODE	NOT USED
2	MON DATA SET READY ON	MON DATA SET READY ON	MON DATA SET READY ON	NOT USED
3	MON RI/DATA SET READY ON	MON RI/DATA SET READY ON	MON RI/DATA SET READY ON	NOT USED
4	NOT USED	MON PHASE DATA SET READY CHECK OFF	MON FLAG, BLOCK DSR ERR.	MON CALL UNIT ACR COS PND
5	NOT USED	MON PHASE DATA SET READY CHECK ON	MON FLAG, ALLOW DSR ERR.	MON CALL UNIT ACR COS
6	NOT USED	NOT USED	RECEIVE INFORMATION, INHIBIT DATA INTERRUPTS	NOT USED
7	RECEIVE	RECEIVE IN PHASE	RECEIVE INFORMATION, ALLOW DATA INTERRUPTS	NOT USED
B	TRANSMIT INITIAL	TRANSMIT INITIAL	TRANSMIT INITIAL	DIGIT VALID
9	TRANSMIT DATA	TRANSMIT DATA	TRANSMIT NORMAL	NOT USED
A	TRANSMIT BREAK	TRANSMIT DATA WITH NEW SYNC	TRANSMIT NORMAL WITH NEW SYNC	NOT USED
B	PREPARE TO TURN	NOT USED	NOT USED	NOT USED
C	TRANSMIT TURNAROUND REQUEST TO SEND OFF	TRANSMIT TURNAROUND REQUEST TO SEND	TRANSMIT TURNAROUND REQUEST TO SEND OFF	NOT USED
D	TRANSMIT TURNAROUND REQUEST TO SEND ON	TRANSMIT TURNAROUND REQUEST TO SEND ON	TRANSMIT TURNAROUND REQUEST TO SEND ON	NOT USED
E	NOT USED	NOT USED	NOT USED	NOT USED
F	DISABLE	DISABLE	DISABLE	DISABLE

SERIAL DATA FIELD (SDF)

BIT	MODE SET	AUTOCALL
24(0)	NOT USED	INTERRUPT REMEMBER
25(1)	NOT USED	POWER INDICATOR (PWI)
26(2)	NOT USED	CALL REQUEST (CRO)
27(3)	DIAGNOSTIC WRAP MODE	DATA LINE OCCUPIED (DLO)
28(4)	SET/RESET DATA TERMINAL READY	PRESENT NEXT DIGIT (PND)
29(5)	SYNC BIT CLOCK	DIGIT PRESENT (DPR)
30(6)	EXTERNAL CLOCK	DATA SET STATUS (DSS)/CALL ORIGINATE STATUS (COS)
31(7)	DATA RATE SELECT	ABANDON CALL & RETRY (ACR)
32(8)	OSC SELECT BIT 1	NOT USED
33(9)	OSC SELECT BIT 2	NOT USED

PARALLEL DATA FIELD (PDF)

	AUTOCALL
4	DIGIT NBR B
5	DIGIT NBR 4
6	DIGIT NBR 2
7	DIGIT NBR 1

LCD

0	SS 9/6
1	Not Used
2	SS B/5
3	AUTOCALL
4	SS 9/7
5	SS 10/7
6	SS 10/B
7	SS 11/B
8	MONITOR FLAG
9	SDLC 8-BIT BYTE
A	NOT USED
B	NOT USED
C	BSC EBCDIC
D	BSC ASCII
E	NOT USED
F	FEEDBACK CHECK

* ICW BIT 38 SET BY OUTPUT X'43'
\# ICW BIT 44 SET BY OUTPUT X'46'

Figure 7-4. Interface Control Word–Type 2 Scanner

meets its requirement for receiving data. The program has no control over this bit.

Bit 5 — This bit is reserved.

Bit 6 — Program Flag: This bit provides a flag in the ICW that can be used by the program.

Bit 7 — Pad Flag: For start-stop transmission, this bit is turned on by the control program when it wants

the Type 2 Scanner to hold the output data line at a mark condition for one complete line-transmission character-time. This operation employs the normal transmit character serializing actions except that the start bit is sent as a mark in place of the normal space. The remainder of the character is serialized as normal, and the control program must ensure that the PDF is loaded with X'7F' if the LCD is X'2' or X'FF' if the LCD is not X'2'. Any number of *pad* characters may be sent by leaving the pad flag on and leaving the PDF set to X'7F' (if LCD is X'2') or X'FF'. When pad transmission is to end, the control program must turn off the pad flag and resume placing normal characters in the PDF. For start-stop receive, this bit is turned on by the control program to cause the Type 2 Scanner to set ICW bit 3 (modem check) when 'receive line signal detect' is inactive. This use of the pad flag provides a higher level of security on switched lines than is attained by monitoring only 'data set ready'. This should only be used on lines with full-duplex facilities.

For autocall and binary synchronous interfaces, this bit is 0.

ICW Bits 8-15 (Parallel Data Field): The parallel data field (PDF) is used as a character buffer. For a transmit operation, the characters to be sent to a terminal are placed in this field by the program with an Output X'44' instruction. Hardware circuits then transfer the character to the serial data field and transmit it to the interface. The format of the character loaded into the PDF depends on the state of the line control definer (LCD).

For receive operations, the character is assembled in the SDF from the line interface and then transferred to the PDF under hardware control. An Input X'44' instruction must then be executed to retrieve the character from this field for program use. The format of the character loaded into the PDF field and how it is used for various line control definer values can be found in the *LCD States* section in this chapter.

For an autocall interface, the digit number must be placed in the PDF as shown in Figure 7-4.

ICW Bits 16-19 (Line Control Definer): The line control definer (LCD) field defines the type of interface associated with the ICW. The LCD, set under program control by an Output X'45' instruction, must be in agreement with the installed interface type and the common carrier or IBM equipment physically attached to the interface. The LCD field definition must also be in agreement with the basic line control procedures to be executed. An LCD is generally set at IPL time and remains static throughout normal operation.

The values of the LCD field are defined in detail along with its effect on the PDF and SDF fields in the section describing LCD states in this chapter.

The LCD field is also used to indicate that a feedback check has occurred. When the scanner sets the LCD field to X'F', it indicates an improper mode set or a hardware failure in either the Type 2 Scanner or the interface hardware.

Programming Note

During a diagnostic wrap operation, the LCD of the line or lines in diagnostic receive must agree with the LCD of the line in diagnostic transmit regardless of the common carrier or IBM equipment physically attached to the line.

ICW Bits 20-23 (Primary Control Field): The primary control field (PCF) defines the state of the interface at any particular time. The interpretation of this field depends on the state of the LCD field. Figure 7-4 shows the PCF states for start-stop, BSC, and SDLC line control. See the section on *Autocall Interface Operation* for a description of the autocall PCF states.

The Output X'45' instruction can be used to set the state of the PCF. Also, an Input X'45' can be executed to test the state of this field. Refer to Appendix B for bit definitions of input/output instructions.

ICW Bits 24-33 (Serial Data Field): The serial data field (SDF) is primarily used as a character deserializer/serializer field. On receive operations, the data coming in from a line is placed in this field bit-by-bit to assemble a character. When a character has been assembled, it is transferred, under hardware control, to the PDF for program access. For transmit operations, a character from the PDF is transferred into the SDF under hardware control and then transferred to the line interface hardware a bit at a time.

The SDF is also used for line interface mode setting and autocall operations. Its format depends on the values in the LCD and PCF fields. See *Interface Mode Set* and *Autocall Interface Operation* in this chapter for further definitions.

Program access to this field is through the Input X'45' and Input X'47' instructions and Output X'46' instruction. Refer to Appendix B for bit definitions of input/output instructions.

ICW Bits 34-36 (SDLC Ones Counter): This counter is used for SDLC lines only.

ICW Bit 37 (SDLC Last Line State): This bit is used only by SDLC lines.

ICW Bit 38 (Display Request): This bit allows the state

of certain latches or signals to be loaded into the Type 2 Scanner display register when the interface associated with this ICW is scanned. The bit may be set and reset by an Output X'43' instruction when the interface address for that ICW is in the attachment buffer address register (ABAR) in the Type 2 Attachment Base.

The contents of the display register in a particular Type 2 Scanner can be accessed by an Input X'46' instruction when that scanner is selected.

Because only one display register is in each Type 2 Scanner, the program should ensure that the display request bit is never on in more than one ICW in each scanner. Only in this way can the information in the display register be meaningful.

Before executing an Input X'46', the program must also ensure that enough time has elapsed to guarantee that the interface has been scanned after setting the display request bit in the ICW associated with the interface.

ICW Bits 39-40: These bits are reserved.

ICW Bit 41 (Level 2 Interrupt Pending): This bit is set when the interrupt priority register (IPR) assigned to this interface is already occupied by another interface. This stacks the new interrupt until the next time the line is scanned and the IPR is not occupied.

ICW Bits 42-43 (Priority Select Bits 1 and 2): These bits assign one of the four interrupt priority registers in the attachment base to the ICW for the interface. All combinations are valid with X'0' designating the lowest priority register and X'3' the highest priority register.

ICW Bit 44 (SDLC NRZI Control): This bit is used only by SDLC lines.

ICW Bit 45: This bit is reserved.

Line Control Definer (LCD) States

This section describes the various LCD (line control definer) states. The LCD field is used during normal transmit and receive operations to define the hardware line control required by the line set type. The variations in the PDF field due to different line set requirements are shown with each LCD state. The first information bit of a transmitted or received character is designated as X1, the second bit as X2, and the nth and last bit as Xn. For start-stop transmissions, the start and stop bits are not regarded as information bits and are inserted or deleted by the Type 2 Scanner hardware.

LCD State X'0' (Start-Stop 9/6 Bit Control): This state should be set for start-stop transmission with a 9/6 format (that is, one start bit, six data bits, and two stop bits). When a character is sent to an interface, the six data bits must be placed into bits 2-7 of the PDF field as shown below. Characters received from the interface are in the same format when the scanner requests a character service interrupt.

PDF bit positions	0	1	2	3	4	5	6	7
Character bits	0	0	X6	X5	X4	X3	X2	X1

LCD State X'1': (Reserved)

LCD State X'2' (Start-Stop 8/5 Bit Control): This state is for start-stop interfaces with an 8/5 format (that is, one start bit, five data bits, and two stop bits). When a character is sent to an interface, the five data bits must be placed into bits 3-7 of the PDF field as shown below. Characters received from the interface are in the same format when the scanner requests a character service interrupt.

PDF bit positions	0	1	2	3	4	5	6	7
Character bits	0	0	0	X5	X4	X3	X2	X1

LCD State X'3' (Autocall): This state is for autocall interfaces. See the *Autocall Interface Operation* section in this chapter.

LCD State X'4' (Start-Stop 9/7 Bit Control): This state is for start-stop interfaces with a 9/7 format (that is, one start bit, seven data bits, and one stop bit). When a character is sent to an interface, the seven data bits are placed into bits 1-7 of the PDF field as shown below. Characters received from the interface are in the same format when the scanner requests a character service interrupt.

PDF bit positions	0	1	2	3	4	5	6	7
Character bits	0	X7	X6	X5	X4	X3	X2	X1

LCD State X'5' (Start-Stop 10/7 Bit Control): This state is for start-stop interfaces with a 10/7 format (that is, one start bit, seven data bits, and two stop

bits). When a character is sent to an interface, the seven data bits must be placed into bits 1-7 of the PDF field as shown below. Characters received from the interface are in the same format when the scanner requests a character service interrupt.

PDF bit positions	0	1	2	3	4	5	6	7
Character bits	0	X7	X6	X5	X4	X3	X2	X1

LCD State X'6' (Start-Stop 10/8 Bit Control): This state is for start-stop interfaces with a 10/8 format (that is, one start bit, eight data bits, and one stop bit). When a character is sent to an interface, the eight data bits must be placed into bits 0-7 of the PDF field as shown below. Characters received from the interface are in the same format when the scanner requests a character service interrupt.

PDF bit positions	0	1	2	3	4	5	6	7
Character bits	X8	X7	X6	X5	X4	X3	X2	X1

LCD State X'7' (Start-Stop 11/8 Bit Control): This state is for start-stop interfaces with an 11/8 format (that is, one start bit, eight data bits, and two stop bits). When a character is sent to an interface, the eight data bits must be placed into bits 0-7 of the PDF field as shown below. Characters received from the interface are in the same format when the scanner requests a character service interrupt.

PDF bit positions	0	1	2	3	4	5	6	7
Character bits	X8	X7	X6	X5	X4	X3	X2	X1

LCD States X'8' through X'B' (SDLC Byte Length): These states are for SDLC lines only.

LCD State X'C' (BSC EBCDIC Line Control): This state is for binary synchronous interfaces using the EBCDIC SYN character. When a character is sent to an interface, the data bits must be placed into bits 0-7 of the PDF field as shown below. The SYN character (X'32') provides for automatic detection of the first phase character during a receive operation.

PDF bit positions	0	1	2	3	4	5	6	7
Character bits	X1	X2	X3	X4	X5	X6	X7	X8

LCD State X'D' (BSC USASCII Line Control): This state is for binary synchronous interfaces using the USASCII SYN character. When a character is sent to the interface, the data bits must be placed into bits 0-7 of the PDF field as shown below. The SYN character (X'16') provides for automatic detection of the first phase character during a receive operation.

PDF bit positions	0	1	2	3	4	5	6	7
Character bits	X1	X2	X3	X4	X5	X6	X7	X8

LCD State X'E': (Reserved)

LCD State X'F' (Feedback Check): This state is set by the Type 2 Scanner whenever a feedback check is detected (1) during scan addressing on any of the scanner 'data in' lines from the selected line interface base, or (2) when a bit service reset error is detected on the line from the selected LIB. A set mode to an interface that has been configurated incorrectly also sets this state.

Primary Control Field (PCF) States

This section describes the PCF states for start-stop and BSC line control. See the *Autocall Interface Operation* section in this chapter for a description of the autocall PCF states. For a description of SDLC line control, see the SDLC section of this chapter.

PCF State X'0' (No-Op): This PCF state causes the Type 2 Scanner to take no action (active or passive) upon subsequent scans. The scanner hardware can request a Type 2 Scanner L2 interrupt and set this PCF state for an interface if it determines that new control information is required from the control program. This PCF state can be set by the control program; however, no interrupts are generated by the interface.

PCF State X'1' (Set Mode): This PCF state causes the scanner to set and reset certain mode latches in the line interface hardware. These latches are specified by the SDF field. When setting this PCF state, the control program must ensure the integrity of the entire ICW. This may be done by first setting the PCF to state X'0' (no-op) so that the ICW will not be modi-

fied by a possible interrupt. The SDF can then be set to the proper value. Finally, state X'1' (set mode) can be set into the PCF field. Execution of a set mode does not require a bit service request from the addressed interface. However, a bit service request must occur to allow the scanner to request a Type 2 Scanner L2 interrupt to end the set mode operation. The set mode operation ends when the scanner hardware sets the PCF state to X'0' (no-op).

A set mode can be executed to change the state of the data rate selector bit and the oscillator select bits without requiring a disable. However, data terminal ready must remain *on*.

PCF State X'2' (Monitor Data Set Ready): This PCF state places the interface in a wait-for-incoming-call condition. For switched lines, this state should normally be set by the control program following a PCF state X'F' (disable) and PCF state X'1' (set mode with data terminal ready bit = 1). When an interface is in this state, the Type 2 Scanner tests the 'data set ready' lead from the common carrier or IBM line adapter for an active condition when the ICW is fetched. When data set ready is *on*, indicating that a call is established, the Type 2 Scanner sets PCF state X'0' (No-Op) for start-stop or PCF state X'4' (monitor phase—data set ready check off) for binary synchronous transmission and requests an L2 interrupt.

Though not necessary, this state can also be used for leased lines. Data set ready should be on at the first bit service request when the interface is scanned.

PCF State X'3' (Monitor Ring Indicator or Data Set Ready): This PCF state, when set by the control program, places the line interface in a wait-for-incoming-call (ring indicator *on*) or wait-for-manual-call-out-connection condition (data set ready *on*). This state must be preceded by setting PCF state X'F' (disable), or a set mode that resets data terminal ready. When the PCF state is set to X'3', the Type 2 Scanner tests the 'ring indicator' and 'data set ready' leads from the common carrier equipment for an active condition of either lead. When 'ring indicator' is active, a call is coming in and a pending connection is to be established. When either of these conditions occurs, the Type 2 Scanner sets PCF state X'0' (no-op) and places the line in a L2 interrupt pending state. This PCF state must be followed by PCF state X'1' (set mode) from the control program to set the 'data terminal ready' latch. After the Type 2 Scanner executes the set mode, it sets PCF state X'0' (no-op) and places the line in a L2 interrupt pending state. The interrupt handling program must then place the line in PCF state X'2' (monitor data set ready on), after which the operation proceeds as described in *PCF state X'2'—Monitor Data Set Ready.*

PCF State X'4' (Monitor Phase—Data Set Ready Check Off): This PCF state is identical to PCF state X'5' (BSC—monitor phase-data set ready check *on*) except that the inactive condition of 'data set ready' does not signal a check condition. PCF X'4' is intended to initialize the *first* receive operation after a switched network call connection has been established.

PCF State X'5' (Monitor Phase—Data Set Ready Check On): This PCF state places a BSC line into a *hunt for phase* condition. The SDF field is shifted each bit interval time, and the contents are examined by the scanner hardware for a comparison with the bit configuration of the 8-bit SYN character. If a compare is successful, PCF state X'7' is set, and the tag bit is inserted in the SDF. An L2 interrupt request, however, is *not* generated at this time. The first interrupt request is at the next subsequent character time. When this interrupt request is presented, the control program must examine the character in the PDF to determine if the second SYN character has been received. If so, the PCF is left in state X'7'. If the second SYN has not been received, the program returns the PCF to state X'5'. The Type 2 Scanner also sets PCF state X'5' after completing a transmit turnaround (PCF state X'C' or X'D').

PCF State X'6' (Receive—Inhibit Data Interrupts): This state is used only for SDLC lines.

PCF State X'7' (Receive): *Start-Stop:* In this PCF state, the Type 2 Scanner monitors for start bits (as described in the *Line Control Definer* section) according to the setting of LCD X'0', X'2', X'4'-X'7'. This state remains in effect until changed by the control program and is set by the Type 2 Scanner after the completion of a transmit turnaround (PCF state X'C' or X'D').

BSC: In this PCF state, the Type 2 Scanner frames consecutive 8-bit characters (as described in the *Line Control Definer* section) according to the setting of the LCD X'C' and X'D'. This state remains in effect until changed by the control program and is set by the Type 2 Scanner after one SYN character has been detected in PCF states X'4' or X'5' for BSC.

PCF State X'8' (Transmit Initial): This PCF state is set by the control program. The Type 2 Scanner places the interface hardware into a transmit condition and transmitting begins when the 'clear to send' lead is activated from the carrier equipment. In addition to

setting this state, the control program must perform the following sequence.

1. Set PCF state X'0' (no-op). This step may have been performed on any previous interrupt.
2. Set the SDF to the first character to be transmitted.
3. Store the second character to be transmitted into the PDF.
4. Set PCF state X'8' (transmit initial).

For start-stop initialization, the first character to be transmitted (set in the SDF) must be X'FF' and the second character (set in the PDF) must be the first information character.

For BSC initialization, when business machine clocking is used, 16 transitions of the 'received data' lead are required to ensure bit synchronization between the transmitting and receiving stations. Therefore, SDF Bits 1-9 must be set to an initial pad of X'355', and the PDF must be set to X'AA'. The next character to be transmitted must be a pad character of X'AA' followed by two SYN characters to enable character synchronization to be established.

BSC specification requires that the first character transmitted be an initial pad character. Therefore, when modem clocking is used, SDF bits 1-9 must be set to X'355'. Since the next two characters must be SYN characters, the PDF must be set to a SYN character. All characters stored into the SDF are assumed to be right-justified.

When the Type 2 Scanner begins transmitting (clear to send *on*), the hardware changes the PCF control state to X'9' (transmit data).

Note: *It may be desirable in certain applications (contention) to test the PCF state in order to determine if a transmit operation should be started. For example, a line may have just set PCF state X'7' (receiving-in-phase), and its subsequent interrupt has not been handled by the control program.*

PCF State X'9' (Transmit Data): This PCF state is set by the Type 2 Scanner after completion of PCF state X'8' (transmit initial). Data is transmitted in this state until one of the transmit turnaround states (PCF X'B', X'C' or X'D') is set by the control program. PCF state X'A' (transmit data with new sync) should be used in place of state X'9' for synchronous modem equipment containing a 'new sync' lead.

All control and non-information characters must be supplied by the control program because the scanner does not perform character decoding, encoding, or insertion of any kind during a transmit operation. The scanner detects and signals underruns, but the control program has to take corrective action, (for example, BSC abort sequence).

For BSC transmission on a line with business machine clocking, the first two characters transmitted in the transmit data states (PCF states X'9' and X'A') must be X'AA' followed by two SYN characters. For BSC transmission on a line with modem clocking, the first character transmitted in PCF state 9 (transmit data) must be X'AA' followed by two SYN characters. Note, this may have already been done under PCF state X'8' (transmit initial).

After all information characters (EOB, EOT, ENQ, ACK, check characters, etc.) have been transmitted under the transmit data states (PCF states X'9' or X'A'), the control program must complete the transmit operation by setting one of the transmit turnaround states (PCF state X'B', X'C' or X'D').

PCF State X'A' (Transmit Break—Start-Stop): This state is set by the control program instead of PCF state X'9' (Transmit Data) when transmitting a *break* signal to the remote destination. The following sequences of PCF states should be set by the control program for transmitting a *break* signal:

	SDF	*PDF*	*Pad Flag*
Transmit Initial (PCF State X'8')	X'FF'	X'FF'	1
Transmit Break		X'00'	0
Transmit Turnaround (PCF X'B' or X'C')		X'FF'	1

After the completion of this sequence, the *break* signal (continuous spacing) continues for n character times. The stop bits for the spaces (X'00') are inhibited from being transmitted as a mark so that the *break* signal is continuous spacing.

Note: *Two character-time delays exist before the actual break signal is transmitted.*

PCF State X'A' (Transmit Data with New Sync): This state is identical to PCF state X'9' (transmit data) except that the 'new sync' line to the modem equipment is active. It must be used only with 4-wire duplex, multipoint leased-line modem equipment where the associated interface is designated as the master station. The control program must change PCF state X'A' to PCF state X'9' (transmit data) in the character service routine that places the last character to be transmitted into the PDF.

PCF State X'B' (Prepare to Turn for Start-Stop): This state is set by the control program on the interrupt following the interrupt that placed the last character (pad or information) to be transmitted into the PDF. While bits are being transmitted, this state is the same as PCF state X'9' (transmit data).

When the character is completely transmitted, PCF state X'C' (transmit turnaround—request to send *off*) is set by the scanner. The SDF is set to X'00', and the line interface transmit data buffer is left in the 'mark' state. This action delays completion of the transmit operation to ensure that the stop bit remains on the interface transmit data output at least one bit time before 'request to send' can be turned off. At the next bit interval, if 'clear to send' is off, the line is placed in an interrupt pending condition as the final interrupt of the transmit operation. PCF state X'7' (Receive—Start-Stop) is set by the Type 2 Scanner, and the SDF is left at X'00'. If 'clear to send' is on, the scanner loops, and there is no change in the PCF state or no interrupt generated until 'clear to send' drops.

PCF State X'C' (Transmit Turnaround—Request to Send Off): For BSC line control (LCD=X'C', or X'D') this PCF state is set by the control program on the interrupt following the interrupt that placed the last pad character to be transmitted into the PDF. While bits are being transmitted, this state is the same as state X'9' (transmit data).

When the character is completely transmitted, 'request to send' is reset along with the 'transmit mode' latch in the interface hardware. PCF State X'C' is not changed until 'clear to send' is off. After 'clear to send' is off, PCF state X'5' (monitor phase - data set ready check *on*) is set, and the line is placed in an interrupt pending state. The control program should make sure 'clear to send' is off before the background time-out elapses. For a description of this state under start-stop line control, see PCF state X'B'.

When the control program wants to close a line that normally transmits with 'request to send' on, it must notify the scanner that 'request to send' is to be turned *off* by a PCF state X'C'. This must be done by sending a *pad message* using PCF state X'B' for start-stop, or PCF state X'C' for BSC, instead of PCF state X'D'. The pad message should result in a continuous marking condition on the line (for Start-Stop, see SCF Pad Flag). An alternative is to ensure that final outgoing transmissions use PCF state X'C'.

Programming Note

Some modems do not turn 'clear to send' off under the above conditions. Therefore, the control program should test this condition and may be required to set the PCF to X'D' and operate with 'request to send' on.

PCF State X'D' (Transmit Turnaround—Request to Send On): This state is set by the control program on the interrupt following the interrupt that placed the last character (pad or information) to be transmitted into the PDF. While the bits are being serialized in the SDF, this state is the same as PCF state X'9' (transmit data).

When the character is fully serialized, the interface transmit control (not including 'request to send') is reset and the final interrupt request is set for the transmit operation. The PCF is set by the Type 2 Scanner to PCF state X'5' (monitor phase - data set ready check *on*) for BSC or to PCF state X'7' (receive) for start-stop.

The significance of 'request to send' on (PCF state X'D') is:

Start-Stop: 'Request to send' on is to be used with all common carrier equipment that provides duplex facilities and for IBM line adapter/modem equipment on duplex communication facilities.

BSC: 'Request to send' on is to be used on point-to-point 4-wire duplex and multipoint 4-wire duplex communication facilities where the controller serves as the master station. All BSC switched network communication facilities are half-duplex.

BSC and Start-Stop Local Attachments: Equivalent to 4-wire point-to-point communication facility.

PCF State X'F' (Disable): This state is set by the control program and causes the Type 2 Scanner to turn off data terminal ready. A disable resets all control information in the line that was provided by the last set mode (PCF state X'1'). The scanner hardware then causes the interface to be placed in an interrupt pending state when the 'data set ready' lead and the 'receive line signal detector' lead are deactivated. For auto-dial applications, other conditions on the automatic calling unit must be satisfied before another dial operation can be attempted. Before the interrupt is requested, PCF state X'0' (no-op) is set by the scanner. Because all control information in the line set is reset, the control program must set up the proper control information again by a set mode (PCF state X'1') in the interrupt after the disable.

Interface Mode Set–SDF Values

The interface hardware latches are set and reset according to the value in the SDF field during PCF state X'1'. The following paragraphs define the SDF values for a set mode.

SDF bits 0-2: ICW Bits 24-26 - Not Used

SDF bit 3: This bit is set to 1 to place the addressed interface in the diagnostic mode.

SDF bit 4: Data Terminal Ready - This bit controls the 'data terminal ready' lead, which must be set to enable the line interfaces provided by all line sets except those used for autocall operation.

SDF bit 5: Synchronous Bit Clock - This bit determines whether synchronous or start-stop clocking is used for the addressed interface when business machine clocking is specified. If SDF bit 6 is 1 (external clock), this bit is ignored.

A feedback check occurs if this bit is on when the program executes a set mode for interfaces provided by all line sets that support start-stop lines only.

SDF bit 6: External Clock - This bit determines whether business machine or modem clocking is used for the addressed interface. A 1 = modem clock, and 0 = business machine clock.

A feedback check occurs if this bit is on when the program executes a set mode for interfaces provided by line sets that allow business machine clock control only.

SDF bit 7: Data Rate Selector - This bit selects a high speed or low speed data rate for the attached modem. A 1 = high data rate, and 0 = low data rate. If modem clocking is specified, this bit selects which of the two clock speeds in the modem is to provide the clock pulses. The low rate usually equals one-half of the high rate. In this case the business machine clock selected by the oscillator select bits must not exceed one-half the clock speed selected in the modem.

A feedback check occurs if this bit is on when the program executes a set mode to a line interface provided by line sets that allow only one data rate.

SDF bits 8 and 9: OSC Select Bits 1 and 2 - The state of these two bits selects the business machine clock to be used by the addressed line interface. At least one business machine clock must be installed in each Type 2 Scanner. See the following section, *Business Machine Clocks.*

Programming Note

The oscillator select bits can be changed without causing a switched network connection to be broken if SDF Bit 4 (Data Terminal Ready) is set when the set mode is executed.

Business Machine Clocks

Each Type 2 Scanner must have at least one business machine clock installed and may have as many as four. If modem clocking is used with any of the lines, a business machine clock must be installed with a speed less than one-half that of the lowest speed modem clock. Figure 6-4 lists the business machine clocks available.

Modems attached to a 3705 must provide clock pulses for line speeds above 2400 bps. Some line sets can operate with either a business machine clock or a modem clock, and some can operate only with a business machine clock. Refer to the *3704 and 3705 Introduction* manual for a description of the individual LIB and line set types.

The installed business machine clock used for a given line is selected under program control by executing a set mode (PCF state X'1') with SDF bits 8 and 9 set to indicate the desired clock. Figure 7-5 shows the proper setting of the oscillator select bits to assign an installed oscillator to a given interface.

SDF Bits 8	9	*Selected Business Machine Clock*	
0	0	Lowest speed clock	(OSC0)
0	1	Next higher speed clock	(OSC1)
1	0	Next higher speed clock	(OSC2)
1	1	Highest speed clock	(OSC3)

Figure 7-5. Type 2 Communication Scanner Business Machine Clock Selection.

No business machine clock is selected if the oscillator select bits are set to select an uninstalled oscillator (for example, bits 8 and 9 set to 11 when only two or three oscillators are installed).

Every interface must have a business machine clock assigned whether it is specified to be business machine or modem clocked. For autocall interfaces and for line interfaces that are to use modem clocking, the assigned business machine clock is used to ensure that the interface is periodically accessed. The lowest speed oscillator must always be used for an autocall interface.

The oscillator select bits are set to 0 by a reset to the scanner. Therefore, the lowest speed clock is initially selected, and unless a set mode is executed to select another clock for a given interface, the lowest speed clock is used.

After a power-on-reset occurs, there is a warm-up period associated with the different clocks. (Refer to Figure 6-4.) During this warm-up period, a business machine clock cannot provide service requests.

Programming Notes

1. The oscillator select bits for a line interface can be changed without causing a switched network connection to be broken, if 'data terminal ready' is up when the set mode is executed.
2. The business machine clock selected for a modem-clocked line interface must be less than one-half the rate of the modem clock.

I/O Programming Considerations

As a general rule, input/output instructions should be issued only when the status of the attachment buffer address register (ABAR) and the particular Type 2 Scanner ICW input register is known. An understanding of how those registers are set or loaded is needed for correct execution.

The ABAR is set under the following conditions:

1. The interface address in the highest priority program level 2 interrupt register located in the attachment base is loaded into ABAR just before program level 2 becomes the current program level.

   Therefore, if an Input X'40' is executed as the first instruction in program level 2, the register specified by the R operand contains the interface address for that interrupt.
2. When the program executes an Output X'40', the interface address in the register specified by the R operand is placed in ABAR.

The ICW input register of the selected Type 2 Scanner is loaded with the contents of the ICW associated with the interface address in the ABAR when:

1. The ABAR is loaded after a program level 2 interrupt occurs.
2. The Output X'40' instruction is executed in program level 3 or 4. This enables the level 3 or 4 routines to access any portion of the selected ICW associated with the interface address in the ABAR.

Figure 7-6 summarizes which program levels can set the ABAR in the attachment base and set the ICW input register in the selected scanner.

Program Level	*ABAR*	*ICW Input Register*
1	Output X'40'	Cannot be set
2	L2 Interrupts	L2 Interrupt
3 or 4	Output X'40'	Output X'40'

Figure 7-6. Setting ABAR and ICW Input Register

The following considerations are recommended for executing input/output instructions in the different program levels.

Program Level 1 (Error Routines)

Input X'40' can be executed to obtain the interface address from the attachment buffer address register (ABAR) in the Type 2 Attachment Base. This old interface address should be saved if a different address is required to select the Type 2 Scanner that has its L1 interrupt request set.

Output X'40' can be executed to select the appropriate Type 2 Scanner if needed. Only the selected Type 2 Scanner can decode the input/output instructions. However, the scanner input register is not changed if an Output X'40' is executed at program level 1 or 2.

After the Type 2 Scanner is selected, other input and output instructions may be executed as needed. Output instructions may be executed in any order, but all output instructions (Outputs X'42', X'43', X'44', X'45', X'46', and X'47') that set a portion of the ICW *must* be separated by at least one cycle. This is required because the output register in the Type 2 Scanner buffers the data from the general register and requires time to store the data in the ICW.

Before exiting from program level 1, the program may execute an Output X'40' to place the old interface address back in ABAR if it had been saved. However, one instruction cycle must separate it from any Output X'42'-X'47'. The selected Type 2 Scanner ICW input register is not changed as a result of Output X'40'.

At least one instruction cycle must separate the last output instruction and an Exit instruction.

Program Level 2 (Character Service)

Input X'40' may be executed immediately to obtain the interface address. When Input X'40' is issued while in program level 2, the 'priority register occupied' latch associated with the interface address in ABAR is reset. This indicates that the character service request is being serviced and that the program level 2 interrupt priority register from which the ABAR was loaded is now available for another level 2 interrupt of the same priority. If all the 'priority register occupied' latches are reset, the Type 2 Scanner L2 interrupt request is reset.

Inputs X'44', X'45', or X'47' may be executed whenever necessary to obtain a portion of the ICW from the Type 2 Scanner ICW input register. Outputs X'43', X'44', X'45', X'46', or X'47' may be executed whenever necessary to set a portion of the ICW.

Output instructions may be executed in any order, but all subsequent Output X'43', X'44', X'45', X'46',

or X'47' instructions must be separated by at least one cycle.

At least one instruction cycle must separate the last output instruction and an Exit instruction.

Programming Note
Subsequent Input X'40' instructions within the same character service interrupt do not reset the 'priority register occupied' latches.

Program Levels 3 and 4 (Lower Level Routines)
Output X'7E' may be executed with a 1 in byte 1, bit 2 of the register specified by the R operand. This will 'mask off' program level 2 interrupts that could change the contents of the attachment buffer address register (ABAR) in the Type 2 Attachment Base by a character service L2 interrupt.

Output X'40' may be executed to load ABAR with the interface address of a line to be acted upon. The contents of the ICW associated with this interface address are placed in that Type 2 Scanner ICW input register.

After the Type 2 Scanner is selected, (1) Output X'43', X'44', X'45', X'46', or X'47' may be executed (to alter the associated portion of the ICW), followed by some other instruction, or (2) some other instruction must be executed, followed by Input X'44', X'45', X'46', or X'47' (to obtain the associated portion of the ICW that was loaded by the Output X'40' into the ICW input register).

If Output X'43', X'44', X'45', X'46', or X'47' was executed as in (1) above, the ICW content was altered, but the ICW input register still contains the contents of the ICW as it was before the alteration.

Output instructions may be executed in any order, but all subsequent Output X'43', X'44', X'45', X'46', or X'47' instructions must be separated by at least one cycle.

It is recommended that all lines in the addressed Type 2 Scanner be disabled before executing an Output X'42' to change the upper scan limit.

Output X'7F' may be executed with a 1 in byte I, bit 2 of the register specified by the R operand. This unmasks the program level 2 interrupts. This output instruction must be separated by at least one instruction cycle from the last Output X'43', X'44', X'45', X'46', or X'47' instruction.

Autocall Interface Operation

The Type 2 Communication Scanner supports operation of an autocall interface when the interface is attached to Line Set 1E and the line control definer (LCD) field of the associated ICW is set to X'3'. The primary control field (PCF) of the ICW is used to control the interface operation. Whenever an autocall interface that has a service request is scanned, the scanner interprets the PCF to determine what communication should occur between the scanner and the interface hardware. The scanner also determines, from the PCF, whether the interface should be placed in a level 2 interrupt pending state. The lowest speed business machine clock installed in each scanner is used to generate service requests for all autocall interfaces installed in that scanner. Service requests are generated at the same rate as the clock speed.

Interface Control Word for Autocall Operation
The following bits/fields are used for autocall operation.

ICW bit 1	Service Request
ICW bits 12-15	PDF bits 4-7
ICW bits 16-19	LCD
ICW bits 20-23	PCF
ICW bits 24-31	SDF bits 0-7
ICW bit 38	Display Request
ICW bit 41	L2 Interrupt Pending
ICW bits 42-43	Service Priority

Programming Note
A reset to the scanner sets the PCF state of each ICW to X'0' and resets ICW bits 34-38 and 41 when the interface is scanned. However, when power is turned on in the controller, all other ICW bits are unpredictable. Therefore the program must ensure that during initialization ICW bits 0-3 are reset.

Primary Control Field for Autocall Operation
Five primary control field (PCF) states are available for autocall operation. Setting the PCF to an undefined value may result in improper operation. Each time the control program changes the PCF state, it should also set the LCD to X'3'. Figure 7-4 shows the PCF states for this LCD value. The following PCF states are valid for autocall interfaces.

PCF State X'0': Idle - This state resets the call request and digit present indications in the autocall interface each time the interface is scanned and a bit service is present. If the control program sets this state, no interrupt requests result from that interface until the program changes the PCF to one of the other valid states. If the scanner sets this state as a result of ending a PCF state X'F' (disable), the interface is placed in a level 2 interrupt pending state.

PCF State X'4': Monitor Call ACR, COS, PND - When the Type 2 Scanner fetches an ICW for an autocall interface in this PCF state, the autocall interface is monitored for the active state of the following leads:

ACR—Abandon Call and Retry
COS—Call Originate Status
PND—Present Next Digit

When any of these leads are found to be active, the appropriate SDF bit is set, and the interface is placed in a level 2 interrupt request pending state.

PCF State X'5': Monitor Call ACR, COS - This state is the same as PCF state X'4' except the active condition of present next digit (PND) does not generate a level 2 interrupt request.

This PCF state can only be set by the control program.

Programming Note
The control program must ensure that the interrupt remember bit (SDF bit 0) is reset when it places the interface in this state. Otherwise no interrupt request can be generated because of active control leads.

PCF State X'8': Digit Valid - This state is set by the control routine after it has placed the next dial digit into the PDF. This digit is continuously presented to the ACU interface until PND falls; the scanner sets the PCF to X'4', and no interrupt is requested.

PCF State X'F': Disable - This state is used to reset the dial interface at the end of the data transfer operation. After all the control leads from the Autocall unit (ACU) have been reset, the Type 2 Scanner sets the PCF to X'0' and places the interface in a level 2 interrupt request pending state.

Serial Data Field for Autocall Operation
The control program can monitor the autocall interface by interrogating the serial data field in the interface control word. Figure 7-4 shows the SDF for ACU interfaces. The serial data field is updated with the current status of the autocall interface each time the interface is scanned and a bit service request is present. SDF bits 1-9 reflect the state of certain autocall control signals and have no effect on the interface operation. Bit 0 is the only SDF bit that affects operation. The following paragraphs describe each SDF bit and its meaning.

SDF Bit 0: Interrupt Remember (IR) - This bit is set by the scanner to indicate a level 2 interrupt pending state. In PCF state X'4' or X'5', the scanner monitors the respective autocall interface leads for an active condition. When one of the monitored leads becomes active, the scanner sets the interrupt remember bit to prevent further interrupts from that interface until the first interrupt has been serviced. This bit must be reset by the control program each time an interrupt is serviced in order to allow the next interrupt to be recognized.

Programming Note
The program should not reset the interrupt remember bit before changing the PCF state from X'4' or X'5' to some other state because an unexpected interrupt request may result.

SDF Bit 1: Power Indicator (PWI) - When this bit is 0, the automatic calling equipment is inoperative because of the lack of power.

SDF Bit 2: Call Request (CRQ) - A 1 in this position indicates a request to originate a call to the autocall interface. The scanner sets the CRQ in the autocall interface whenever (1) the interface is scanned, (2) a bit service request is present, and (3) the PCF State is X'4', X'5', or X'8'. If the condition of this bit does not agree with the state defined for the active PCF state, the LCD is set to X'F' to indicate a feedback check.

SDF Bit 3: Data Line Occupied (DLO) - A 1 in this position indicates that the autocall interface is in use. The program should not attempt to originate a call until this lead becomes inactive.

SDF Bit 4: Present Next Digit (PND) - A 1 in this position indicates that the autocall unit is ready to accept the next digit. The PND lead is used by the autocall unit to control the presentation of digits to the unit during a dialing operation.

When the 'present next digit' lead is active and the PCF state is X'4', the scanner sets the interrupt remember bit if it is not already on. If the PND lead is inactive and the PCF state is X'8', the scanner changes the PCF state to X'4'.

SDF Bit 5: Digit Present (DPR) - A 1 in this position indicates that a valid digit is present on the digit leads to the autocall unit. The scanner sets DPR via PCF state X'8' after present next digit comes on and the next dial digit has been placed into the parallel data field, bits 4-7. When the autocall unit turns PND off, the scanner changes the PCF state to X'4' and resets DPR. The scanner resets DPR when the PCF state is changed to X'0', X'4', X'5', or X'F'. If the condition of this bit does not agree with the state defined for the active PCF state, the LCD field is set to X'F' to indicate a feedback check.

SDF Bit 6: Data Set Status (DSS)/Call Originate Status (COS) - A 1 in this position indicates that a connection has been established and that the modem is

in data mode and can be used for data communications. In PCF state X'4', the scanner sets the interrupt remember bit when the DSS/COS lead becomes active.

SDF Bit 7: Abandon Call and Retry (ACR) - A 1 in this position indicates that a preset time interval in the autocall unit has elapsed since the last change of the present next digit lead. This bit only alerts the control program to the time-out condition; it does not automatically abandon the call and retry. The control program is responsible for abandoning the call and retrying. In PCF state X'4', the scanner sets the interrupt remember bit when the ACR lead becomes active.

SDF Bits 8 and 9: These bits are not used.

Parallel Data Field for Autocall Operation
For autocall operation the parallel data field is used to present the dial digits to the automatic calling unit. When the autocall interface is in PCF state X'8', the parallel data field bits 4-7 must contain a valid digit. In any PCF state other than X'8', the PDF is treated as if it contained all zeros. The valid digits that can be loaded into the PDF are from X'0' to X'9' and X'C' and X'D'. X'0' to X'9' represent the value of the dial digit and X'C' is an *end of number* bit configuration used to inform the autocall unit that the last digit of the called number has been provided. X'D' is a *separator* bit configuration used to inform the autocalling unit to wait for a second dial tone.

Note: *The external automatic calling unit (ACU) must have the appropriate features to use X'C' and X'D'.*

Input/Output Instructions

The Type 2 Scanner input/output instructions enable the program to communicate between line interface bases (LIBs), program interrupt levels, interface control words (ICWs), and Type 2 Scanner registers. Some of the major functions of the I/O instructions are to:

- Determine the interface address that caused a program level 2 interrupt.
- Determine the cause of a program level 1 interrupt once the scanner causing the interrupt has been identified (Input X'76' has been executed).
- Determine the status of a particular ICW.
- Determine the status of a Type 2 Scanner display register.
- Set the attachment buffer address register (ABAR) with the interface address required for:
  a) addressing a particular ICW in program levels 3 or 4.
  b) restoring an old ABAR address that had been saved while in the error routines of a program level 1 interrupt. This allows the program to resume normal operation with the same interface address in the ABAR as when the program level 1 interrupt occurred.
  c) addressing a particular scanner in program level 1, 3, or 4.
- Set and reset bits in a particular ICW.
- Set scan limits in a particular scanner while setting the substitution control register (SCR) in the Type 2 Attachment Base.
- Set control bits in a particular scanner.

Programming Note
Input/Output instructions are privileged instructions executable only at program level 1, 2, 3 or 4. Any attempt to execute these instructions improperly causes a program level 1 interrupt request by setting the 'input/output check L1' latch. Refer to *Input/Output Check* description in Chapter 5 for the conditions that cause the check to be set.

Input Instructions
Six input instructions allow the program to obtain the status of the ICW input register, display register, and error register in the Type 2 Scanner, and the interface address in the attachment base ABAR. (Appendix B defines the bits within each input instruction.)

Programming Notes
1. With Extended Addressing, byte X of all input instructions and external registers is set to zero.
2. When an autocall interface is used, some of the input instructions have different bit definitions. Refer to the individual instruction descriptions for these differences.

Input X'40' (Interface Address): This instruction is used to obtain the line interface address from the ABAR in the attachment base. Conditions that set the ABAR are described in the *I/O Programming Considerations* section in this chapter.

If Input X'40' is issued during program level 2, the 'priority register occupied' latch associated with the interface address in the ABAR is reset. This indicates that the character service request is being serviced and that the program level 2 interrupt priority register from which the ABAR was loaded is now available for another level 2 interrupt of the same priority. If all the 'priority register occupied' latches are reset, the Type 2 Scanner L2 interrupt request is reset.

Programming Note
Subsequent Input X'40' instructions within the same character service interrupt do not reset the 'priority register occupied' latches.

Input X'43' (Check Register): This instruction may be used to obtain the status of the check register of a scanner. Since it is possible for four Type 2 scanners to be installed in the controller, the check register selected is determined by the interface address in the ABAR at time of instruction execution.

Programming Note
If any of the check register bits in the Type 2 Scanner are set to 1, the Type 2 Scanner L1 interrupt request is set.

Input X'44' (ICW Input Register - Bits 0-15): This instruction may be used to determine the state of the secondary control field (SCF) and the parallel data field (PDF) in the ICW that is set in the ICW input register. The interface address in the ABAR selects the proper scanner. Refer to *I/O Programming Considerations* for conditions that set the ICW input register. The SCF and PDF fields and bit definitions are described in the *Interface Control Word Format* section of this chapter. Synchronous Data Link Control (SDLC) uses certain bits of the SCF differently.

Input X'45' (ICW Input Register - Bits 16-31): This instruction may be used to determine the state of the LCD and PCF fields and SDF bits 0-7 in the ICW that is set in the ICW input register. The interface address in the ABAR selects the proper scanner. Refer to *I/O Programming Considerations* in this chapter for conditions that set the ICW input register. The LCD, PCF, and SDF fields and bit definitions are described in the *Interface Control Word Format* section of this chapter. The LCD and PCF fields are used differently for SDLC lines.

Input X'46' (Display Register): This instruction may be used to determine the state of the display register in the Type 2 Scanner selected by the interface address in ABAR.

The program, under control of the *display request* (ICW bit 38), can cause status information for a particular interface to be placed into the Type 2 Scanner display register when the interface is scanned. Input X'46' can then be used to examine this status information.

Input X'47' (ICW Input Register - Bits 32-45): This instruction may be used to determine the state of SDF bits 8-9, display request bit, L2 interrupt pending bit, and priority bits 1-2. The ones counter, the last line state, and the NRZI control bit, all of which are used by SDLC, can also be examined by using this instruction. The interface address in the ABAR selects the proper scanner and associated ICW. See *I/O Programming Considerations* in this chapter for conditions that set the ICW input register. For an interpretation of these bits, see the *Interface Control Word Format* and the *SDLC* sections of this chapter.

Output Instructions
Seven output instructions allow the program to set the status of the ICW and to set the upper scan limit and certain other controls in the Type 2 Scanner. The interface address in the ABAR and the substitution control register in the Type 2 Attachment Base may also be set. (Appendix B defines the bits within each output instruction.)

Programming Note
With Extended Addressing, byte X of all output instructions and external registers has no significance and can be ignored.

Output X'40' (Interface Address): This instruction may be used to set an interface address in the attachment buffer address register (ABAR) of the Type 2 Attachment Base. When this instruction is executed, byte 0, bit 6 through byte 1, bit 6 in the register specified by the R operand are placed in the ABAR.

The interface address placed in ABAR selects the Type 2 Scanner and the ICW associated with that address. Each CCU clock time, the 46 bits of the ICW are placed in the ICW work register. If Output X'40' is executed in program level 3 or 4 the contents of the ICW work register are placed in the ICW input register where it is available for Inputs X'44', X'45', and X'47'.

Output X'41' (Scan Substitution Control): This instruction must be used to set the substitution control register in the Type 2 Attachment Base. See *Address Substitution* in this chapter for the description and coding of the SCR bits.

Output X'42' (Upper Scan Limit Control): This instruction must be used to set the upper scan limit in the selected Type 2 Scanner. At least one Output X'42' must be executed for each Type 2 Scanner available. The Scanner selected is determined by the interface address in the attachment buffer address register (ABAR) of the attachment base at the time of execution.

Output X'43' (Control): This instruction may be executed to set or reset various control functions in a Type 2 Scanner. The Type 2 Scanner is selected by the interface address in the attachment buffer address register (ABAR) of the attachment base.

Output X'44' (ICW Bits 0-3 and 5-15): This instruction may be used to reset secondary control field (SDF) bits 0-3 and 5 (5 is for SDLC use only), and to set or reset bits 6-7 of the SCF. It is also used to set or reset the parallel data field (PDF). For a detailed description of these bits, see the *Interface Control Word Format* section in this chapter and, for Synchronous Data Link Control (SDLC), refer to the *SDLC* section of this chapter. The PDF field is used as a character buffer. The interface address in the attachment buffer address register (ABAR), located in the Type 2 Attachment Base, selects the Type 2 Scanner and the ICW associated with this address. Refer to the secondary control field of the ICW for an interpretation of the SCF bits (byte 0, bits 0-7). See *Interface Control Word Format* for the PDF format as it relates to various line control definer states, and for SDLC variations of the PDF format, refer to the *SDLC* section of this chapter.

Output X'45' (ICW Bits 16-23): This instruction may be used to set the bits of the line control definer (LCD) and the primary control field (PCF) in the ICW. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a detailed interpretation of these bits, see the *Interface Control Word Format* section in this chapter. See the *SDLC* section of this chapter for a detailed description of these bits when they are used to define SDLC lines.

Output X'46' (ICW Bits 24-33 and 44): This instruction is used to set the bits (24-33) of the serial data field (SDF) and bit 44, NRZI Control (SDLC only). The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a detailed interpretation of the SDF bits, see the *Interface Control Word Format* section in this chapter. For a description of bit 44, NRZI Control, refer to the SDLC section of this chapter.

Output X'47' (ICW Bits 34-43): This instruction is used to set the state of ICW bits 34-43. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a detailed interpretation of these bits, see the *Interface Control Word Format* and the *SDLC* sections of this chapter.

SDLC

The following paragraphs describe the Type 2 Scanner as it applies to Synchronous Data Link Control (SDLC). The differences between SDLC lines and other line types center upon the use of the Interface Control Word (ICW). Some ICW bits are used exclusively for SDLC and some bits, which are common to other line types, are used differently for SDLC. The control program must recognize the line as an SDLC line and interpret the ICW bits accordingly. For a description of the SDLC line discipline, refer to the *Synchronous Data Link Control General Information* manual.

ICW Bits 0-7 (Secondary Control Field): The secondary control field (SCF) is used as a sense, status, and operation modifier field between the control program and the Type 2 Scanner. Bits 0-5 are set by the Type 2 scanner hardware according to conditions received from the line. Bits 6 and 7 are program controlled.

This field may be examined by using the Input X'44' instruction. An Output X'44' instruction is used to reset bits 0-3 and 5 and to set and reset bits 6 and 7.

Bit 0—Abort: The Type 2 Scanner sets this bit to 1 when it detects seven consecutive 1 bits in the received data stream while the PCF state is X'6' or X'7'. If this bit is 1, the service request interlock (ICW bit 1) is forced to 0. Bit 0 must be reset by the control program using an Output X'44' instruction.

This bit has no significance during a transmit operation.

Note: *A transmitted abort sequence consists of eight contiguous 1 bits. However, if the scanner detects seven contiguous 1 bits while receiving data, it will set the abort bit (ICW bit 0) to 1.*

Bit 1—Service Request Interlock: The scanner sets this bit to 1 as described in the *ICW Format* section of this chapter, except that the scanner is prevented from setting this bit if an SDLC flag or SDLC abort is detected. This bit is reset as previously described in this chapter and also by detection of SDLC abort.

Bit 2—Character Overrun/Underrun: This bit operates as previously described and has one additional function. If the PCF state is X'7' and the flag is detected at other than the predicted position, this bit is set to one.

Bit 3—Modem Check: This bit is the same for all ICWs. See *ICW Format* in this chapter.

Bit 4—Receive Line Signal Detector: This bit is the same for all ICWs. See *ICW Format* in this chapter.

Bit 5—Flag Detection/Disable Zero Insert Remembrance: During a receive operation (LCD X'8' or X'9'), this bit is set to 1 when the scanner detects a flag character in the received data. An interrupt request is not set because ICW bit 5 is set to 1, but an interrupt request may be set by a change of the PCF state due to detection of the flag. This bit must be reset to 0 by the control program when the scanner is in a receive operation.

During a transmit operation, this bit is set to 1 as a character is being transferred from the PDF to the SDF, provided ICW bit 7 is set to 1. ICW bit 5 set to 1 prevents insertion of a 0 after five contiguous 1 bits are transmitted. If ICW bit 7 is 0, ICW bit 5 is set to 0 as a character is transferred from the PDF to the SDF. With ICW bit 5 set to 0, a 0 bit is inserted into the data stream after five contiguous 1 bits are transmitted.

Bit 6—Program Flag: This bit provides a flag in the ICW that can be used by the program.

Bit 7—Disable Zero Insert Control: For a transmit operation, this bit should be turned on by the control program at the same time a flag or an abort character is set into the PDF. When this bit is 0, the scanner inserts a 0 bit into a transmitted character after five contiguous 1 bits are sent. When this bit is 1, the insertion of a 0 bit is blocked after the five 1 bits, and the sixth bit transmitted is not changed.

As a character is transferred from the PDF to the SDF for transmission, the state of ICW bit 7 is transferred to ICW bit 5. This bit has no significance during a receive operation.

ICW Bits 8-33 (Parallel Data Field): These bits form the parallel data field (8-15), the line control definer (16-19), the primary control field (20-23), and the serial data field (24-33). The PDF and the SDF provide the same functions as described in the *ICW Format* section of this chapter. The changes in the states of the LCD and the PCF for support of Synchronous Data Link Control are described in the following sections.

ICW Bits 34-36 (Ones Counter): These three bits are used as an SDLC ones counter. This counter is stepped and reset by the Type 2 Scanner hardware. During a receive operation, this counter is used to detect:

- Inserted 0's that are to be deleted from the bit stream while in PCF states X'6' and X'7'.
- Flag sequences (X'7E') while in PCF states X'5', X'6', and X'7'.
- Abort sequences (seven consecutive 1 bits) while in PCF states X'6' and X'7'.

During a transmit operation, this counter is used to insert a 0 bit after each five consecutive 1 bits transmitted when ICW bit 5 is set to 0. This applies to PCF states X'8', X'9', X'A', X'C', and X'D' only.

ICW Bit 37 (Last Line State): This bit retains the state of the last bit transacted between the scanner and the LIB during an SDLC operation.

ICW Bits 38-43: These bits have the same definition for SDLC as for other line disciplines.

ICW Bit 44 (NRZI Control): When ICW bit 44 is *on* and the PCF state is X'9', X'C', or X'D', the data that is transmitted is in NRZI mode (non-return-to-zero-inverted). When this bit is *off* the data is transmitted in a normal mode (0 and 1 bits). In NRZI mode the line level is complemented when a 0 is transmitted and unchanged when a 1 bit is transmitted. NRZI mode and zero insertion (ICW bit 7) after five consecutive 1 bits ensure a line transition every six bits regardless of the data pattern. NRZI is used to ensure bit synchronization of modems that do not provide received data timing.

Line Control Definer (LCD) States for SDLC

This section describes the LCD (line control definer) states X'8' and X'9' that apply to SDLC lines. These states are added to the states described previously in this chapter, and unlike the other LCD states, the LCD for an SDLC line can be changed by the Type 2 Scanner. The control program sets the desired LCD state by executing an Output X'45' instruction.

When a flag character is detected in the receive data stream and the LCD state is X'8', the Type 2 Scanner hardware resets the existing LCD state and sets an LCD X'9' to receive that character. This is the only case in which the scanner sets the LCD. Returning the state to the proper setting for the next character is the responsibility of the control program.

The variations in the PDF field due to the different LCD states are shown with each state.

LCD State X'8' (SDLC Monitor Flag): This LCD state along with PCF state X'5' is set by the control program to monitor the received information for an SDLC flag sequence. For a description of what happens when a flag is detected, see *PCF State X'5'* in this section of Chapter 7.

LCD State X'9' (SDLC 8 Bit Byte): This LCD state is

used for transferring SDLC 8-bit characters. This state must be set by the control program for transmitting on SDLC lines. When a character to be transmitted is sent to the PDF, the eight data bits must be placed into bits 0-7 of the PDF as shown below.

PDF bit positions	0	1	2	3	4	5	6	7
Character bits	X1	X2	X3	X4	X5	X6	X7	X8

Characters received from the interface are in the same format when the scanner requests a character service interrupt. All address, control, and flag characters are 8-bit bytes.

This field is set by scanner hardware when a flag is detected in the received information while LCD state X'8' is set.

This is the only LCD state that can be set by the scanner. It is set by the scanner when a flag is received while LCD state X'8' is set.

Primary Control Field for (PCF) States SDLC

This section describes the PCF states for support of SDLC lines in the Type 2 Communication Scanner.

PCF states X'0', X'1', X'2', X'3', X'A', and X'F' are the same as for BSC and start-stop lines, as given elsewhere in this chapter.

PCF State X'4' (Monitor Flag—Block Data Set Ready Error): This PCF state is identical to PCF state X'5' (monitor flag—allow data set ready error) except that the inactive condition of 'data set ready' does not signal a check condition.

PCF State X'5' (Monitor Flag—Allow Data Set Ready Error): This PCF state is used in conjunction with LCD state X'8' to monitor for an SDLC flag after a half-duplex turnaround or after an inactive period on the communication channel. Each bit interval time, the SDF is shifted one bit and the counter located in ICW bits 34-36 is updated. The counter is used to detect the flag character. When a flag character is detected, the following actions are taken by the scanner:

- The contents of the SDF are zeroed out and a tag bit is inserted in the ICW.
- The flag detection bit (ICW bit 5) is set on in the SCF.
- The PCF state is set to X'6'.
- The LCD state is set to X'9'.
- A level 2 interrupt is requested.

The flag character is not transferred to the PDF and the service request bit (ICW bit 1) is not turned on.

PCF State X'6' (Receive Information—Inhibit Interrupts): This state is entered when a flag is detected while in state X'4', X'5', or X'7'. During this state the scanner monitors the receive data stream. Inserted zeros are deleted and 8-bit characters are assembled. If contiguous flags are received:

- Flag detection (ICW bit 5) is set in the SCF every character time.
- Transfer from SDF to PDF is inhibited.
- Service request (ICW bit 1) is not set.
- No interrupt is requested.

When a non-flag character is assembled:

- The PCF state is set to X'7'.
- The character is transferred from SDF to PDF.
- Service request (ICW bit 1) is set to initiate data transfer between the control program and the PDF.

PCF State X'7' (Receive Information—Allow Data Interrupts): This state can be entered from PCF state X'6' when a non-flag character is detected. This state is used in conjunction with LCD state X'9' to assemble consecutive bits into 8-bit SDLC characters. The scanner remains in this state until a flag sequence is detected, or until the state is changed by the control program. When a flag sequence is detected, the scanner changes to PCF state X'6' and requests a level 2 interrupt.

PCF State X'8' (Transmit Initial): PCF state X'8' is used to initiate a transmit operation on an SDLC interface when the LCD is set to X'9'. This state disables the NRZI mode and forces the 'send data' lead to a *mark* state as long as 'clear to send' is not active. When 'clear to send' becomes active, the NRZI mode and the 'send data' lead are allowed to operate normally.

If business machine clocking is used, the first characters transmitted must be X'00' (if using NRZI mode) or X'AA' (if not using NRZI mode) so that the remote clock can get in synchronization. If modem clocking is used, the two leading characters (X'00' or X'AA') are not required, and the first two characters and the tag bit should be set in the SDF and PDF.

When a flag is placed in the PDF for transmission, the disable zero insert control bit (ICW bit 7) must be turned on by the control program. When the Type 2 Scanner begins transmission ('clear to send' on), the scanner hardware changes the PCF state to X'9' (transmit data).

Note: *When operating on a half-duplex line, the control program should not set the PCF state to X'8' until ICW bit 4 (receive line signal detector) is turned off.*

PCF State X'9' (Transmit Normal): This PCF state is set by the Type 2 Scanner after completion of PCF state X'8'. Data is transmitted in this state until one of the transmit turnaround states (PCF X'C' or X'D') is set by the control program.

During transmission of characters over the SDLC line, the control program must maintain the proper state of the LCD. For example, when a flag character is placed into the PDF, the LCD must be set to X'9' and ICW bit 7 (disable zero insert control) must be set to 1. This allows transmission of more than five consecutive 1 bits for control purposes. For non-flag characters the disable zero insert control bit must be off.

PCF State X'C' (Transmit Turnaround—Request to Send Off): This PCF state is set by the control program on the interrupt following the interrupt that placed the last flag character to be transmitted into the PDF. While bits are being transmitted, this state is the same as PCF state X'9'.

When the character is completely transmitted, 'request to send' is reset along with the 'transmit mode' latch in the interface hardware.

PCF State X'D' (Transmit Turnaround—Request To Send On): This PCF state is set by the control program when the ending flag character for a message is placed in the PDF and the disable zero-insert control bit (7) is set on. In this state, the scanner transfers the flag character from the PDF to the SDF and sets the flag detection/disable zero insert remembrance bit (5) to the current state of the disable zero-insert control bit (7) every flag character transfer. Continuous flag characters will be serialized to the LIB without further interrupts until PCF state X'D' is ended by the control program.

The control program normally ends this state by setting PCF state X'9'. When changing from PCF state X'D' to PCF state X'9', the first character to be transmitted in the X'9' state is loaded into the PDF and the disable zero-insert control bit (7) is reset if that character is not a flag. Subsequent characters are supplied by normal data servicing requests.

Programming Note

When changing from state X'D' to state X'9', the program should check that the zero insert remembrance bit (5) is 1 to ensure that at least one flag character has been sent since state X'D' was set.

Diagnostic Functions

The Type 2 Communication Scanner has two diagnostic functions available to the control program: (1) the diagnostic wrap and (2) the IBM modem wrap test. These two tests are run under the control of the scanner program and provide online testing as described in the following sections. These diagnostics cannot be issued to an autocall interface.

For line interfaces attached through any one scanner, either a diagnostic wrap operation or a modem wrap test can be performed, but not simultaneously. However, these tests can be performed on two different scanners simultaneously.

Diagnostic Wrap Test

The Type 2 Scanner diagnostic wrap provides a means of testing and locating defects in the line control logic and line-interface transmit and receive logic. It also provides a method of online program testing.Diagnostic wrap can be performed online without affecting the normal program operation or the lines not in diagnostic mode. The test requires one line interface to act as a transmit line and one or more line interfaces in the same scanner to act as receive lines. Any line in the Type 2 Scanner can be a transmit or a receive line; however, there may be only one diagnostic transmit line per scanner at any one time.

The diagnostic wrap is initiated under program control by executing Output X'45' and Output X'46' instructions to all lines to be tested. The Output X'45' instruction is executed with byte 1, bits 0-3 set for proper line control and byte 1, bit 7 set to 1 to indicate PCF state X'1' (set mode). The remaining bits of this output are set to 0. See PCF state X'1' in this chapter for further information on set mode.

Output X'46' must be set as follows:

Byte 0, bits 0-7: These bits are 0.

Byte 1, bit 0: This bit is 0.

Byte 1, bit 1: Diagnostic Mode (ICW bit 27) - This bit must be set to 1.

Byte 1, bit 2: Data Terminal Ready (ICW bit 28) - This bit must be set to 0.

Byte 1, bit 3: Synchronous Clock (ICW bit 29) - This bit must be set according to the type of Line Set tested. A 1 is placed in this position for binary synchronous lines, and a 0 for start-stop lines.

Byte 1, bit 4: External Clock (ICW bit 30) - This bit must be set to 0 to select a business machine clock.

Byte 1, bit 5: Data Rate Select (ICW bit 31) - This bit may be either 1 or 0.

Byte 1, bits 6-7: Oscillator Select 1 & 2 (ICW bits 32-33) - These bits are set to select an available line oscillator (business machine clock). For proper setting, see *Business Machine Clocks* in this chapter. All wrap test lines must select the same oscillator.

After the set modes are issued, the affected line interfaces can be exercised through any sequence of point-to-point or multipoint operations.

During diagnostic wrap operations both the 'data set ready' lead and the 'clear to send' lead are simulated active to prevent the Type 2 Scanner from setting a modem check (ICW bit 3). The 'clear to send' lead is not simulated active if the PCF is set to X'C' and the Type 2 Scanner detects that it has completely serialized the character in the SDF. This is to allow either the PCF state X'B' or X'C' to be used during a diagnostic wrap.

Programming Note

1. Only one interface per Type 2 Scanner may be in a transmit state at any given time during the operation.
2. The line used for transmit should be the last line to be issued the mode set.
3. Diagnostic wrap cannot be executed on an autocall interface.
4. During a diagnostic wrap operation, the line control definer (LCD) of the line or lines in diagnostic receive must agree with the LCD of the line in diagnostic transmit regardless of the common-carrier or IBM equipment physically attached to the line.

Modem Wrap Test

Modem wrap test tests the scrambler circuits of IBM 3872, 3874, and 3875 modems under program control. The modem test can be performed online without affecting the normal operation of other lines. This test may also be performed simultaneously on any or all interfaces for which the test function is defined.

To execute the modem wrap test, the LCD field of the ICW for the interface to be tested must be X'8', X'9', X'C', or X'D'. The control program must then execute an Output X'46' instruction to set the interface control word SDF as follows:

SDF bits 0-2: These bits are not used and should be 0.

SDF bit 3: This bit must be set to 1 to cause the 'diagnostic mode' latch to be set in the line interface hardware, which conditions the modem for testing.

SDF bit 4: This bit must be set to 1 to cause 'data terminal ready'. When this is set, together with the diagnostic mode, it enables a modem wrap test operation to be performed instead of a diagnostic wrap.

SDF bit 5: This bit must be set to 1 to provide synchronous clocking.

SDF bit 6: This bit must be set to 1 if the modem provides the clock and to 0 if the modem does not provide the clock.

SDF bit 7: This bit may be either 0 or 1.

SDF bits 8 and 9: These bits must select an internal oscillator whose speed is less than one-half the clock speed if the IBM modem provides the clock. If the modem does not provide the clock, the bits must select an internal oscillator whose speed matches that of the modem. For the proper setting, see *Business Machine Clocks* in this chapter.

After the set mode is executed, the interface should be put in PCF state X'8' (transmit initial) to cause 'request to send' to be raised. Before this is done, the PDF and SDF fields should be set to X'FF' and the pad flag (ICW bit 7) turned on to cause continuous marks to be transmitted. When the first interrupt occurs in PCF state X'9', the PCF should be changed to X'D' to cause the interface to turn around with 'request to send' on. When the turnaround is complete, the interface is in PCF state X'5', and a mark is sent.

The program can now test the operation of the modem scrambler circuits by setting the PCF to X'7' (receiving in-phase) and checking the received data for all marks for a period of at least one second.

Chapter 8: Type 3 and Type 3HS Communication Scanners

This chapter is intended to give the reader a basic understanding of the operation of the Type 3 and Type 3HS Communication Scanners and the requirements necessary to program these scanners.

Because the Type 3 and Type 3HS Communication Scanners are similar in operation, only the differences are identified. Unless otherwise noted, the information in this chapter refers to both the Type 3 and Type 3HS Scanners.

The Type 3 or Type 3HS Communication Scanner (1) scans the interface addresses assigned to the LIB positions it supports. (2) performs character assembly/disassemly. (3) provides buffering of message characters within local storage-up to eight characters for Type 3 Scanners and up to sixteen characters for Type 3HS Scanners, and (4) causes program interrupts when program service is required to obtain another program buffer or to handle an end-of-message condition.

Up to four Type 3 Communication Scanners can be installed in the 3705 (Type 3 Scanner-1 through Type 3 Scanner-4). Type 3 Scanner-1 supports attachment of up to three LIBs with 48 half-duplex (HDX) lines. Type 3 Scanner-2, -3, and -4 can each support attachment of up to four LIBs with 64 HDX lines; thus, up to 240 HDX lines can be attached to the 3705 using four Type 3 Scanners. The Type 3 Scanners can be installed with the Type 2, Type 3, or Type 4 Channel Adapter features.

The number of lines supported by a Type 3 Scanner depends on:

- How lines are used.
- Line disciplines.
- Mix of line speeds.

Up to four Type 3HS Communication Scanners can be installed in a 3705-II (the Type 3HS Scanner is not available for the 3705-I or 3704).

The Type 3HS Communication Scanner allows only two line interface addresses on a Type 1 LIB. For duplex SDLC operation, line set 1TA is available for attachment to the Type 3HS Scanner. This line set provides a single line with a transmit address of zero and a receive address of two. For half-duplex BSC or SDLC operation, line set 1GA is available for attachment to the Type 3HS Scanner. Two 1GA line sets (maximum allowed for each scanner) provides two half-duplex lines – one line interface address is zero and the other is two. The Type 3HS Scanner can be installed only with a Type 2, Type 3, or Type 4 Channel Adapter Feature.

For information about LIBs and their capacities, refer to the *Introduction to the IBM 3704 and 3705* manual.

Operation and Data Flow

The interface addresses for all installed Type 3 or Type 3HS Communication Scanners in the 3705 are generated from a common Type 2 Attachment Base. A continuously running *scan counter* in the attachment base places the generated interface address on an address bus that goes to all scanners simultaneously. This address can be modified, under program control, by the attachment base or the scanner.

The interface address is then used to address an interface control word (ICW), which is loaded into the ICW work register where the scanner hardware determines if any action is to be performed for that interface. If no action is required the ICW is replaced in local store and the next addressed ICW is loaded into the work register. If the scanner determines that program intervention is required, it requests a level 2 interrupt and loads the interface address into an interrupt priority register.

When the level 2 interrupt actually occurs, the address in the highest-priority interrupt priority register that is active is loaded into the attachment buffer address register (ABAR) and is then available to the control program along with the ICW in the ICW input register.

Note: *The notation "bit 0.1", "bit 1.5", etc., is used throughout this chapter to refer to the bytes and bits of the ICW and registers. For example, "bit 1.5" refers to byte 1, bit 5.*

Local Storage

Each Type 3 or Type 3HS Scanner contains a local storage array to store the interface control words when not being used by the scanner hardware or the control program. This storage array holds 64 interface control words of 16 bytes each for the Type 3 Scanner and two interface control words of 16 bytes each for the Type 3HS Scanner. (A parity bit is associated with each byte.)

Type 3 or Type 3HS Scanner Registers

The Type 3 or Type 3HS Scanner contains various hardware registers that are used to store and pass information and data within the scanner and between the scanner and the control program. Some of these hardware registers are available to the control program as external register addresses through input and output instructions. The external registers required for control program access are described in the following paragraphs.

ICW Work Register

The Type 3 or Type 3HS Scanner control logic uses the ICW work register to access, monitor, and modify an interface control word (ICW). This register is loaded each time an ICW is read out of local storage.

ICW Input Register
The control program uses the ICW input register for access to the interface control words. This register is loaded from the ICW work register and reflects the status of the ICW at the time when it was read out of local storage.

The ICW is loaded into the input register by level 2 interrupt from the scanner for the associated line or by an Output X'40' instruction in program level 3 or 4 when the address of the line is in the ABAR.

Attachment Buffer Address Register (ABAR)
The attachment buffer address register is physically located in the Type 2 Attachment Base and supplies the interface addresses to the control program. See *I/O Programming Considerations* in this chapter for a description of loading the ABAR.

Programming Note
The ABAR must be initialized by an Output X'40' instruction with an interface address associated with an installed Type 3 or Type 3HS Scanner. The Output X'40' must be executed after the controller is powered on and before any other input or output instructions to the scanner are executed.

Display Register
The display register is a temporary storage register that can contain interface control information that the program can use. If bit 4.6 (display request) of an interface control word is on, control information for that interface is loaded into the display register each time that interface is scanned. (This bit is turned on via an Output X'43' instruction in which bit 0.2 is on; the instruction must be executed after the address of the line for which the information is to be displayed has been loaded in the ABAR via an Output X'40' instruction.) The control program can then obtain this information by executing an Input X'46' instruction.

There is only one display register for each Type 3 or Type 3HS Scanner; therefore, only one ICW at a time should have its display request bit (4.6) set to 1. Otherwise, the control program cannot determine which interface was the last one to cause the display register to be loaded. The display register normally contains the status of the clear to send, ring indicator, data set ready, receive line signal detect, receive data bit buffer, diagnostic wrap mode, bit service request, and ICW diagnostic mode indicators for the line interface (or contains the Autocall unit indicators, for an Autocall interface). Alternatively, the display register contains the status of the scanner-to-line set *data out* lines (if the scanner is in diagnostic 0 mode [ICW bit 5.5 is on]) or the line set-to-scanner *data in* lines (if a feedback check has occurred for the line interface [LCD state is X'7' or X'F']).

A feedback check error occurs when the state of any data in line does not match the state of the corresponding data out line (which indicates that the line interface hardware is not in the state intended to be set by the control program). The display register bit corresponding to the non-matching data out/data in line pair is set to 0; all other bits are 1.

Scanner Output Register
The scanner output register buffers the bits received from the CCU outbus until the next CCU time occurs, allowing the ICW bits or control latch settings to be altered. This register is loaded from the CCU outbus via Output X'41'–X'4F' instructions.

Scanner Check Register
The scanner check register comprises 21 check latches, each associated with the detection of a specific error condition in the Type 3 or Type 3HS Scanner. The control program may access the check register after an interface address specifying a Type 3 or Type 3HS Scanner is placed in the attachment buffer address register (ABAR) via an Output X'40' instruction. The current state of the check register may be determined by an Input X'42' and and an Input X'43' instruction.

The scanner issues a level 1 interrupt request to the CCU when any of the check register latches is set. These latches may be reset by an Output X'43' instruction. The reset bit (byte 0, bit 1) of the instruction must be on and the scanner request bit (byte 1, bit 5) of the register specified by the R field of the instruction must be on.

Diagnostic Buffer Address Register (DBAR)
Bits 1.0–1.5 of an Input X'42' instruction will contain the failing ICW address (in binary for any ICW, work register parity check, PDF array parity check, or LIB select error). The control program can use this address to determine the line for which the error occurred.

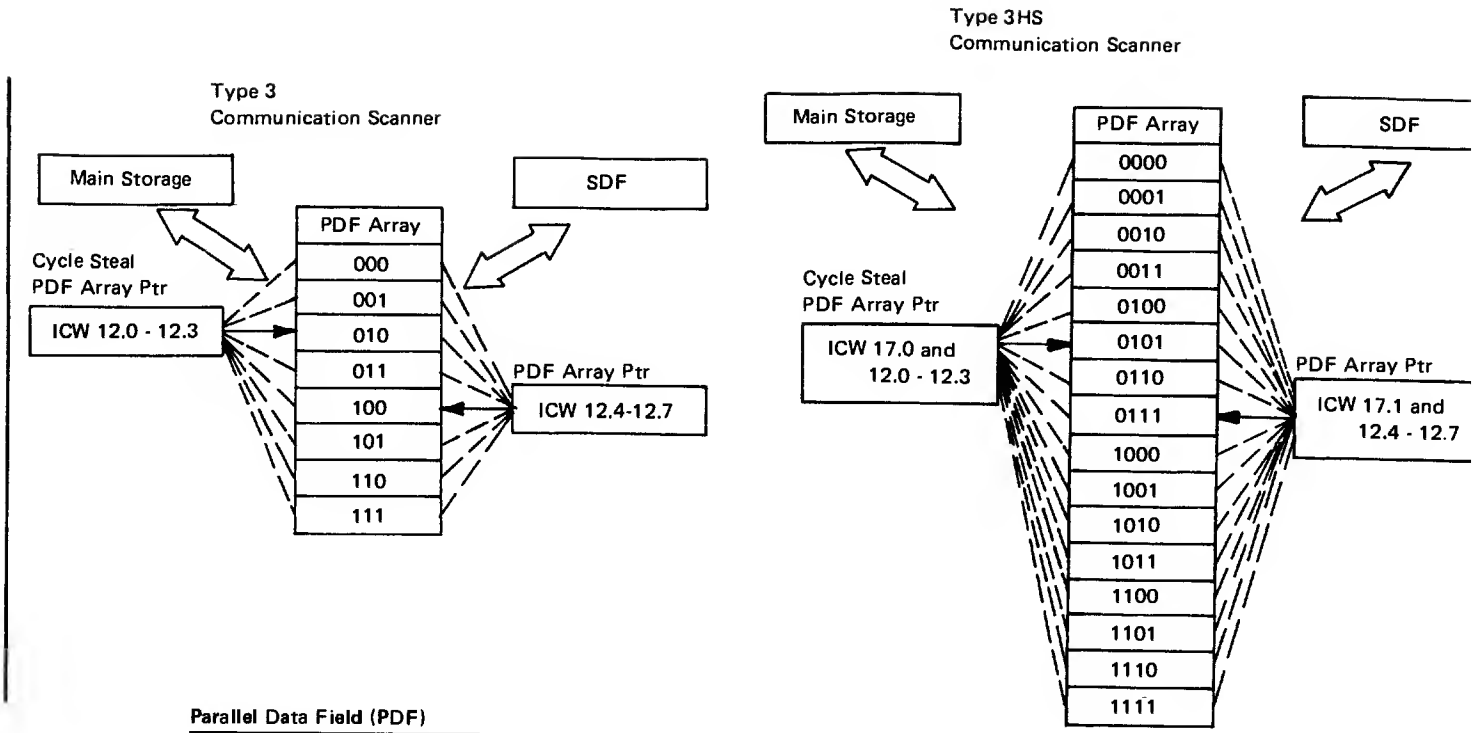
Cycle Steal Buffer Address Register (CBAR)
The scanner loads this register with the current address of main storage into which data is to be stored or from which data is to be fetched with a cycle steal operation. The current address is obtained from ICW bytes 6, 8, and 9.

PDF Array Format

Associated with each ICW is a set of addressable buffers called parallel data fields (PDF). Eight buffers are associated with the Type 3 Scanner and 16 buffers are associated with the Type 3HS Scanner. Each set is called a PDF array. Each PDF in the array contains eleven bits (plus a parity bit) and is used to hold a data character or control and status information pertaining to the receive or transmit operation in which the scanner is currently engaged.

The format of each PDF is shown in Figure 8-1.

Each PDF array buffers message data between main controller storage and the communication line interface with which the array is associated via the interface control word (ICW). The format and content of the interface control word appears later in this chapter.



Parallel Data Field (PDF)

PDF Array Bit	0.5	0.6	0.7	1.0	1.1	1.2	1.3	1.4	1.5	1.6	1.7	P
	0	0	Reserved	DATA 0	1	2	3	4	5	6	7	P
	1	0	CONTROL									P
	1	1	STATUS								Reserved	P

PDF Control Register

Bit	SDLC	BSC
0.7	Set ICW 0.0 ((Abort Detect)	Reserved
1.0	Set ICW 14.1 (Idle Detect)	Set ICW 14.1
1.1	Set ICW 0.3 (reserved)	Set ICW 0.3 (reserved)
1.2	Set ICW 14.3 (Data check) CRC	Set ICW 14.3 (Data check) VRC/CRC
1.3	Set ICW 14.4 (Flag off boundary)	Set ICW 14.4 (Bad Pad)
1.4	Set ICW 0.5 (End of Message)	Set ICW 0.5 (End of Message)
1.5	(Reserved)	Set ICW 14.6 (Invalid DLE sequence)
1.6	Set ICW 14.7 (Length Check)	Set ICW 14.7 (Length Check)
1.7	Set L2 Interrupt	Set L2 Interrupt

PDF Status Register

Bit	SDLC	BSC
0.7	Set ICW 15.0 (Control Exception)	0
1.0	0	0
1.1	0	0
1.2	0	0
1.3	0	BSC Ending Character/T.O. Received
1.4	0	
1.5	0	
1.6	0	
1.7	Reserved	Reserved

FINAL STATUS BSC RECEIVE

Bit 1.3			1.6	
0	0	0	0	Timeout
0	0	0	1	ITB
0	0	1	1	ENQ
1	0	0	1	ETX
1	0	1	0	ETB

Figure 8-1. PDF Array Format

Two pointers within the ICW select the PDF to be used in the current receive or transmit operation. The cycle steal PDF array pointer selects the PDF into which a cycle steal operation is to transfer data from main storage (during a transmit operation) or from which a cycle steal operation is to transfer data to main storage (during a receive operation). The PDF array pointer selects the PDF into which the received data from the SDF is placed, or from which data to be transmitted via the SDF is placed.

During a transmit operation, the scanner places data characters from main storage into the PDFs, in succession via a cycle steal operation. Data transfer continues until all PDFs in the array are full, or until all the data to be transmitted has been placed in the PDF array. The scanner concurrently removes, in succession, data characters from the PDFs that the cycle steal operation has filled and passes them to the line interface hardware via the serial data field (SDF). The SDF serializes the bits to the line interface hardware. (The serial data field is located in byte 3 of the ICW.) The scanner increments the cycle steal PDF array pointer as each byte is transferred from main storage, and increments the PDF array pointer as each data byte is transferred from the PDF to the SDF.

The scanner normally transfers data via cycle steal operation two bytes at a time. The scanner initiates a cycle steal operation each time two PDFs associated with the ICW have been emptied (that is, transmitted). The scanner compares the cycle steal PDF array pointer and the PDF array pointer to determine when two bytes are empty.

During a receive operation, the opposite action occurs. The scanner transfers data characters in succession from the line interface (via the SDF, which deserializes the bits into characters) to the PDF array until all data has been received (as indicated by ending characters) or the PDF array is full. Concurrently, the scanner transfers received characters from the PDF to main storage using a cycle steal operation until all PDFs filled during the receive operation are empty or the scanner detects ending characters.

The scanner increments the cycle steal PDF array pointer as each byte is transferred to main storage, and increments the PDF array pointer as each data byte is transferred from the SDF to the PDF.

For BSC receive operations, the scanner initiates a cycle steal operation whenever two or more PDFs in the array have been filled from the line interface (via the SDF). The scanner compares the cycle steal PDF array pointer and the PDF array pointer to determine when at least two PDFs have been filled. For SDLC receive operations, the scanner initiates a cycle steal operation when the content of the cycle steal message counter (ICW bits 13.6, 13.7) has been incremented to a non-zero value.

For either a transmit or a receive operation, the PDF array acts as a wraparound eight or sixteen-byte buffer. During a transmit operation the PDF array pointer (which "empties" the PDF) logically follows the cycle steal PDF array pointer (which "fills" the PDFs) in succession through the array. During a receive operation, on the other hand, the cycle steal PDF array pointer (which "empties" the PDF) follows the PDF array pointer (which "fills" the PDFs). (See Figure 8-1.)

Ending the Cycle Steal Operation

For a transmit operation, the cycle steal operation that transfers data from main storage to the PDF array continues until the 'cycle steal valid' bit in the ICW (bit 6.5) is reset. This occurs when (1) the cycle steal byte count reaches zero, or (2) the scanner detects an ETB, ETX, or ENQ character in the received data (for BSC line only).

After transmitting all of the data characters to be sent, the scanner transmits the ending character or sequence and then causes a program level 2 interrupt.

For a receive operation, the cycle steal operation that transfers data from the PDF array to main storage continues until the 'cycle steal valid' bit in the ICW (bit 6.5) is reset to 0. This occurs when (1) the cycle steal byte count reaches zero, or (2) the scanner detects a control byte in the PDF array when the 'end of message' bit (ICW bit 0.5) is on.

During a receive operation, the scanner transfers status and control bits to the PDF array following the last message data character received. The specific status and control information placed in the PDF array depends on the current states of the line control definer (LCD), primary control field (PCF), and extended primary control fields of the ICW. These fields are described later in this chapter. Unlike data bytes, which the cycle steal operation transfers to main storage, status bytes are transferred from the PDF to ICW byte 15 (BSC/SDLC control status) and control bits are used to set bits in ICW bytes 0 (secondary control field [SCF]) and 14 (status exception). Storing of status and control bits follows storing of the data bytes.

Upon detecting an ending character or sequence in received data, the scanner causes a program level 2 interrupt.

PDF-Full and PDF-Empty Conditions

The cycle steal PDF array pointer bits and the PDF array pointer bits determine when the PDF is full or empty.

Type 3 Communication Scanner: The PDF array is empty when (1) the low-order bits of both the cycle steal PDF array pointer (ICW bits 12.1 – 12.3) and the PDF array pointer (ICW bits 12.5 – 12.7) are equal, and (2) the high-order bits (bits 12.0 and 12.4) are equal.

The PDF array is full when (1) the low-order bits of both the cycle steal PDF array pointer (ICW bits 12.1 – 12.3) and the PDF array pointer (ICW bits 12.5 – 12.7) are equal, and (2) the high-order bits (bits 12.0 and 12.4) are unequal.

Type 3HS Communication Scanner: The PDF array is empty when (1) the low-order bits of both the cycle steal PDF array pointer (ICW bits 12.0 – 12.3) and the PDF array pointer (ICW bits 12.4 – 12.7) are equal, and (2) the high-order bits (bits 17.0 and 17.1) are equal.

The PDF array is full when (1) the low-order bits of both the cycle steal PDF array pointer (ICW bits 12.0 – 12.3) and the PDF array pointer (ICW bits 12.4 – 12.7) are equal, and (2) the high-order bits (bits 17.0 and 17.1) are unequal.

Scanner Initialization

The scanner and its associated line interfaces (LIB) are placed in a disable state (1) during a power-on sequence, (2) during an initial program load (IPL) of the 3705, (3) when the controller is reset from its control panel, or (4) during the execution of an Output X'43' instruction (discussed later in this chapter) when the general register specified by the R field of the instruction contains appropriate bits. The control program must enable each scanner in the controller by executing an Output X'43' instruction for which register bits 0.1 and 1.6 are 1 before initializing each ICW and the associated line or autocall interface. This initialization must occur before the interface can operate.

PDF Array Reset

It is important to note that when 3705 power is turned off, the PDF array is not automatically reset upon restoration of power. Therefore, the programmer, when loading the controller via IPL, must clear the array by issuing, for each line address to be used, four Output X'4D' instructions, (eight Output X'4D' instructions for the Type 3HS Scanner) followed by one Output X'4E' instruction. Only those addresses to be used by the control program being loaded need have these instructions issued.

Type 3 or Type 3HS Scanner Addressing

The scanner scan-addressing and program-addressing mechanism is controlled by the Type 2 Attachment Base. The attachment base generates the basic scan address and places it on a 'line address bus' for availability to all installed Type 3 or Type 3HS Communication Scanners. Refer to the *Interface Addressing* section of Chapter 3 for a detailed discussion of each interface address bit.

Scan Addressing

For scan addressing, an interface in each installed Type 3 or Type 3HS Scanner is addressed simultaneously. Each scanner derives the address of the interface it is scanning from the 8-bit address that the Type 2 Attachment Base places on a 'line address bus'. The line address bus is an internal bus that carries the scan address from the attachment base to each of the communication scanners. This address, possibly modified by a Type 3 Scanner (see "Upper Scan Limit" and "High Speed Select"), is used not only to select a particular interface but also to address the associated interface control word (ICW) that the scanner maintains in local storage. (See *Interface Control Word* in this chapter.) The scanner examines this ICW and, when an interface service function is required, performs that function; or, when a character service requires programming action, the scanner signals the attachment base that it needs a program level 2 interrupt.

Scan Counter

The 3705 Type 2 Attachment Base scan counter output provides the basic scan addresses for each Type 3 or Type 3HS Scanner.

Type 3 Communication Scanner: If the scan counter output is not modified, each Type 3 Scanner sequentially scans 96 interface addresses. Under these circumstances, the Type 3 Scanner cannot handle line speeds higher than 4800 bps without having the possibility of undetected bit overrun/underrun conditions. However, the ability to substitute some interface addresses (high speed select or address substitution) and set a limit on the number of interfaces scanned (scan limit), greatly extends the capability of handling higher-speed lines. These mechanisms cause the scan counter output to be modified to allow certain interface addresses to be scanned at higher rates than others.

Type 3HS Communication Scanner: The scanner output is modified by each Type 3HS Scanner to allow sequential scanning of only two interface addresses. Consequently, the Type 3HS Scanner is capable of operating at line speeds up to 230,400 bps. High speed select or address substitution and scan limit are not applicable to Type 3HS Scanner operations.

Upper Scan Limit (Type 3 Scanner Only)

The Type 3 Scanners have an upper scan limit that can be set and reset under program control by an Output X'42' instruction. Each scanner maintains its own upper scan limit and is independent of the limits set by any of the other installed scanners. Based on the state of its upper scan limit latches, a Type 3 Scanner may modify the scan counter output from the Type 2 Attachment Base in such a way as to limit the number of interface addresses scanned.

The actual modification of the scan address is done by the Type 3 Scanner hardware as the line address bus enters the scanner from the attachment base. Figure 8-2 shows the number of interfaces scanned and the LIB position affected for each setting of the upper scan limit. When the upper scan limit is set to any value other than binary 00, the scanner modifies the addresses above the limit to start at the first address again. For example, if the upper scan limit is set to allow only 16 interface addresses to be scanned, the address is modified to scan the first address again when the scan counter output to that scanner reaches the 17th address.

Upper Scan Limit (Note 1)	Number of Interfaces Scanned	Interface Addresses Scanned	Interface Addresses Not Scanned	Effective Scan Period (μsec)		
				(Note 3)	(Note 4)	(Note 5)
00	96 (Note 2)	Addr 0-F, LIB 1-6		153.6	192	172.6
10	48	Addr 0-F, LIB 1-3	Addr 0-F, LIB 4-6	76.8	96	86.4
11	16	Addr 0-F, LIB 1	Addr 0-F, LIB 2-6	25.6	32	28.8
01	8	Addr 0-7, LIB 1	Addr 8-F, LIB 1 and Addr 0-F, LIB 2-6	12.8	16	14.4

Notes:
1. Set by Output X'42' byte 1, bits 6-7
2. Scanner-1 contains 64 ICWs in local storage but only uses the first 48.
3. Scan periods for a 3705-I only (1.2 microsecond CCU clock).
4. Scan periods for a 3705-II having a 1.0 microsecond CCU clock.
5. Scan period for a 3705-II having 900 nanosecond CCU clock.

Figure 8-2. Upper Scan Unit (Not applicable to Type 3HS Scanners)

This decreases the period of time between successive scans of the remaining interface addresses to accommodate higher-speed lines. In this case, the scanner with an upper scan limit of binary 11 scans the first 16 interfaces four times in the same period of time as another scanner with no limit scans 96 addresses.

Address Substitution (Type 3 Scanner Only)

The output of the scan counter can be modified to cause certain addresses assigned to LIB position 1 to be substituted on the 'line address bus' in place of normal scan addresses. As a result, those addresses that are substituted are scanned by the Type 3 Scanner more frequently than the other addresses. Address substitution affects all installed scanners in the same manner. When operating with address substitution, each scanner in the 3705 scans the substituted address or addresses, every 12.8 microseconds (3705-I) or 16 microseconds (3705-II), because address substitution occurs every eighth time the scan counter changes state. This allows the substitution address or addresses in each scanner to handle higher line speeds independent of the state of the scan limit.

Address substitution is controlled by a four-bit register called the substitution control register. The bits of this register may be set under program control by Output X'41' byte 1, bits 2,3,4, and 5. Each bit of this substitution control register corresponds to one of four substitution addresses assigned to LIB position 1.

Programming Note

Any combination of the four substitution control register bits may be turned *on* to produce the desired substitutions. If address substitution is not used, Output X'41' must be executed with byte 1, bits 2 through 5 *off* in the register specified by the R operand.

When a given substitution control register bit is on, a corresponding address is substituted on the 'line address bus' every eighth time the scan counter changes state. Combinations of bits on in the substitution control register result in fixed-address substitution for each corresponding bit. Figure 8-3 shows which address is substituted and which addresses are not scanned as a result of that substitution when the various substitution control register bits are on.

Output X'41' Byte 1, Bit:	Fixed Address Substituted in Each Type 3 Scanner If Substitution Bit ON	Addresses Not Scanned In Each Type 3 Scanner If Substitution Bit ON
2	Adr 0 LIB position 1	Adr E in LIB positions 1-6 Adr F in LIB positions 1-6
3	Adr 2 LIB position 1	Adr C in LIB positions 1-6 Adr D in LIB positions 1-6
4	Adr 4 LIB position 1	Adr A in LIB positions 1-6 Adr B in LIB positions 1-6
5	Adr 6 LIB position 1	Adr 8 in LIB positions 1-6 Adr 9 in LIB positions 1-6

Figure 8-3. Address Substitution Control (Not applicable to Type 3HS Scanners)

High Speed Select Option (Type 3 Scanner Only)

The high speed select option is similar to address substitution in that bit settings within a register alter the scanning pattern so that a predetermined address is scanned several times per scanning cycle, at the expense of not scanning other addresses. This option differs from address substitution, however, in that up to eight addresses serviced by the Type 3 Scanner can receive the increased scanning frequency, and high speed select masks are individually specified for each of the installed Type 3 Scanners. Because the mask specified affects only one scanner, it has no influence on the selection of addresses scanned by other installed scanners. This independence allows more flexibility in selecting addresses to receive the increased scanning. No line interfaces associated with the unscanned addresses can be active while the high speed select option is in effect.

High speed select operation is controlled by an eight-bit scan substitution control register. The bits of this register may be set under program control by Output X'41' byte 0, bits 0-7. Figure 8-4 shows which address is substituted and

which addresses are not scanned as a result of that substitution when the various high speed select register bits are on.

Output X'41' Byte 0, Bit:	*Fixed Address Selected in Addressed Type 3 Scanner If High Speed Select Bit On*	*Addresses Not Scanned in Addressed Scanner If High Speed Select Bit On*
0	Adr 0 LIB position 1	Adr 1 in LIB position 1 Adr 0 & 1 in LIB positions 2-6
1	Adr 2 LIB position 1	Adr 3 in LIB position 1 Adr 2 & 3 in LIB positions 2-6
2	Adr 4 LIB position 1	Adr 5 in LIB position 1 Adr 4 & 5 in LIB positions 2-6
3	Adr 6 LIB position 1	Adr 7 in LIB position 1 Adr 6 & 7 in LIB positions 2-6
4	Adr 8 LIB position 1	Adr 9 in LIB position 1 Adr 8 & 9 in LIB positions 2-6
5	Adr A LIB position 1	Adr B in LIB position 1 Adr A & B in LIB positions 2-6
6	Adr C LIB position 1	Adr D in LIB position 1 Adr C & D in LIB positions 2-6
7	Adr E LIB position 1	Adr F in LIB position 1 Adr E & F in LIB positions 2-6

Figure 8-4. High Speed Select Control
(Not applicable to Type 3HS Scanners)

Program Addressing

Various input and output instructions exist that allow the program to control the operation of the Type 3 or Type 3HS Scanners, Type 2 Attachment Base, and the individual interfaces.

However, before the program can examine or modify fields in an interface control word (ICW) associated with a particular interface, the address of that interface must be placed in the attachment buffer address register (ABAR) of the attachment base. Similarly, before the program can access certain registers in a particular Type 3 or Type 3HS Scanner or perform control functions in that Scanner, the interface address in the ABAR must be one of those assigned to that scanner. Two events can cause the contents of the ABAR to be changed: (1) a program level 2 interrupt, and (2) execution of an Output X'40' instruction.

When a program level 2 interrupt occurs, the contents of the ABAR are automatically set by the Type 2 Attachment Base with the interface address from the highest interrupt priority register that is occupied. The control program can determine which interface address is in the ABAR by executing an Input X'40' instruction. The program can then examine and/or modify fields in the ICW associated with this interface. In the other interrupt program levels (1, 3, and 4), the program may find it necessary to gain access to the ICW associated with a specific interface. By executing Output X'40' under such circumstances, the program can set the ABAR according to the interface address in the register specified by the R operand.

To avoid conflicts with the automatic mechanism that sets the ABAR when a program level 2 interrupt occurs, programs executing at program level 3 or 4 should mask program level 2 interrupts before executing Output X'40'. (Program level 1 should save the value of the ABAR, change it to select the desired interface, and then restore the original value to the ABAR.) If more than one program level is likely to execute an Output X'40', additional interlocking conventions must be established within the control program.

Interface Control Word (ICW)

The Interface Control Word (ICW) provides the normal means by which the control program communicates with the scanner and the interface hardware.

Each ICW is 16 bytes long (17 bytes for Type 3HS Scanners) and is located in scanner local storage. Associated with the ICW is an array of eight parallel data fields (16 PDFs for Type 3HS Scanners), each eleven bits (plus parity bit) long. One of the PDFs is logically associated with the ICW at any moment via pointers in byte 12 of the ICW. Figure 8-5 shows the format of the ICW and the input/output instructions by which the ICW fields are set or accessed. Byte 0 and bytes 2-16 (2-17 for Type 3HS Scanners) are the bytes of the ICW proper. Byte 1 is the parallel data field which, though not actually part of the ICW, is shown because it is logically part of the ICW for the purpose of the associated Input/Output instructions. Each scanner contains one ICW for each possible interface. However, even though the scanner contains the maximum number of ICWs (96) only those ICWs associated with an attached and active interface are used.

ICW Access

The Type 3 Scanner hardware gains access to an ICW by using the interface address provided by the interrupt priority register in the Type 2 Attachment Base. When the level 2 interrupt occurs, the address from the interrupt priority register is loaded into the attachment buffer address register (ABAR). The program can then execute an Input X'40' instruction to get the interface address associated with the interface. Once the control program obtains the interface address, it has access to the various fields of the ICW through input and output instructions.

Programming Note

ICW access at program level 3 or 5 should be performed only when program level 2 interrupts are masked off; otherwise, the result is unpredictable.

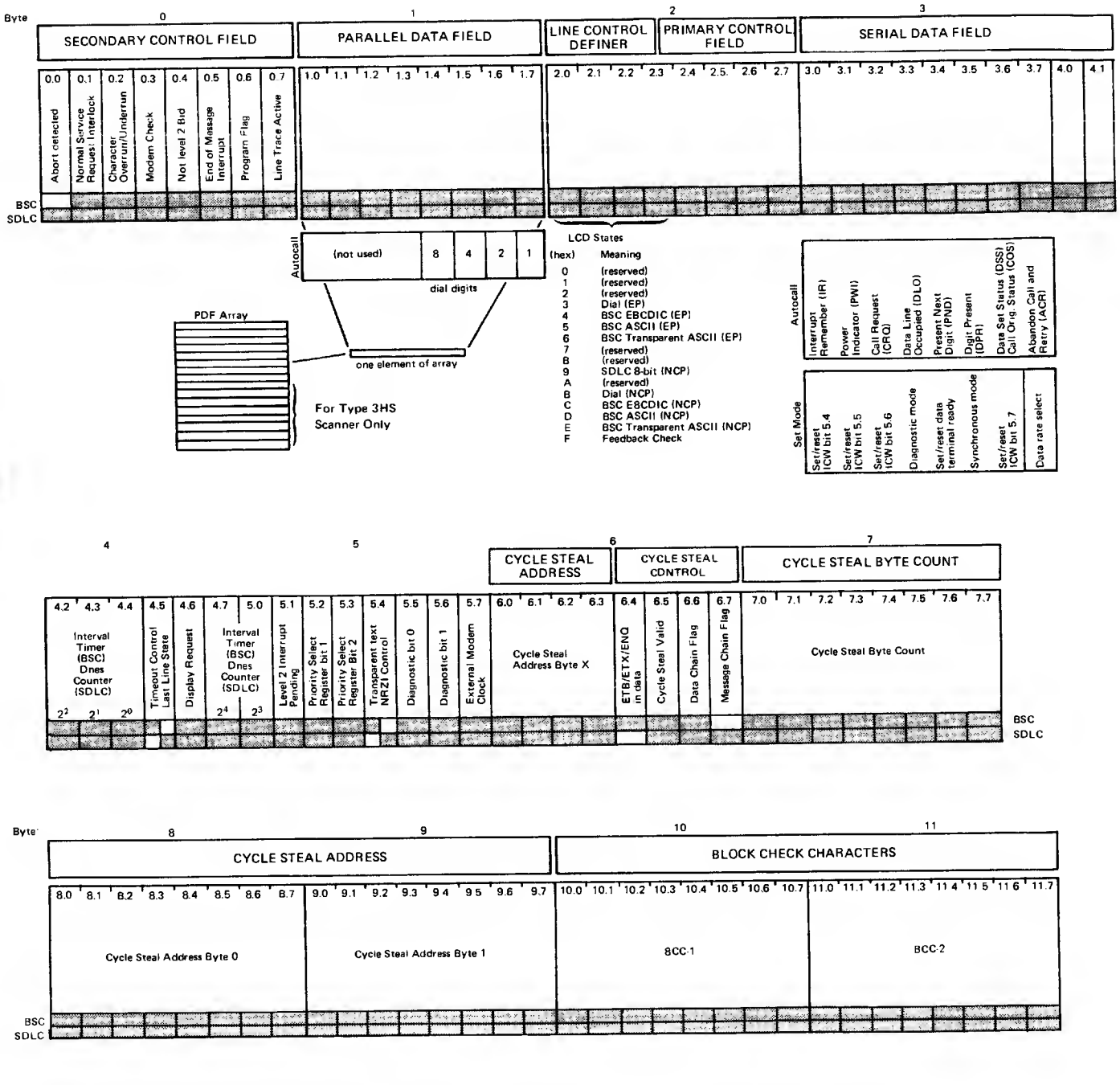


Figure 8-5. Interface Control Word Type 3 and Type 3HS Scanner (Part 1 of 2)

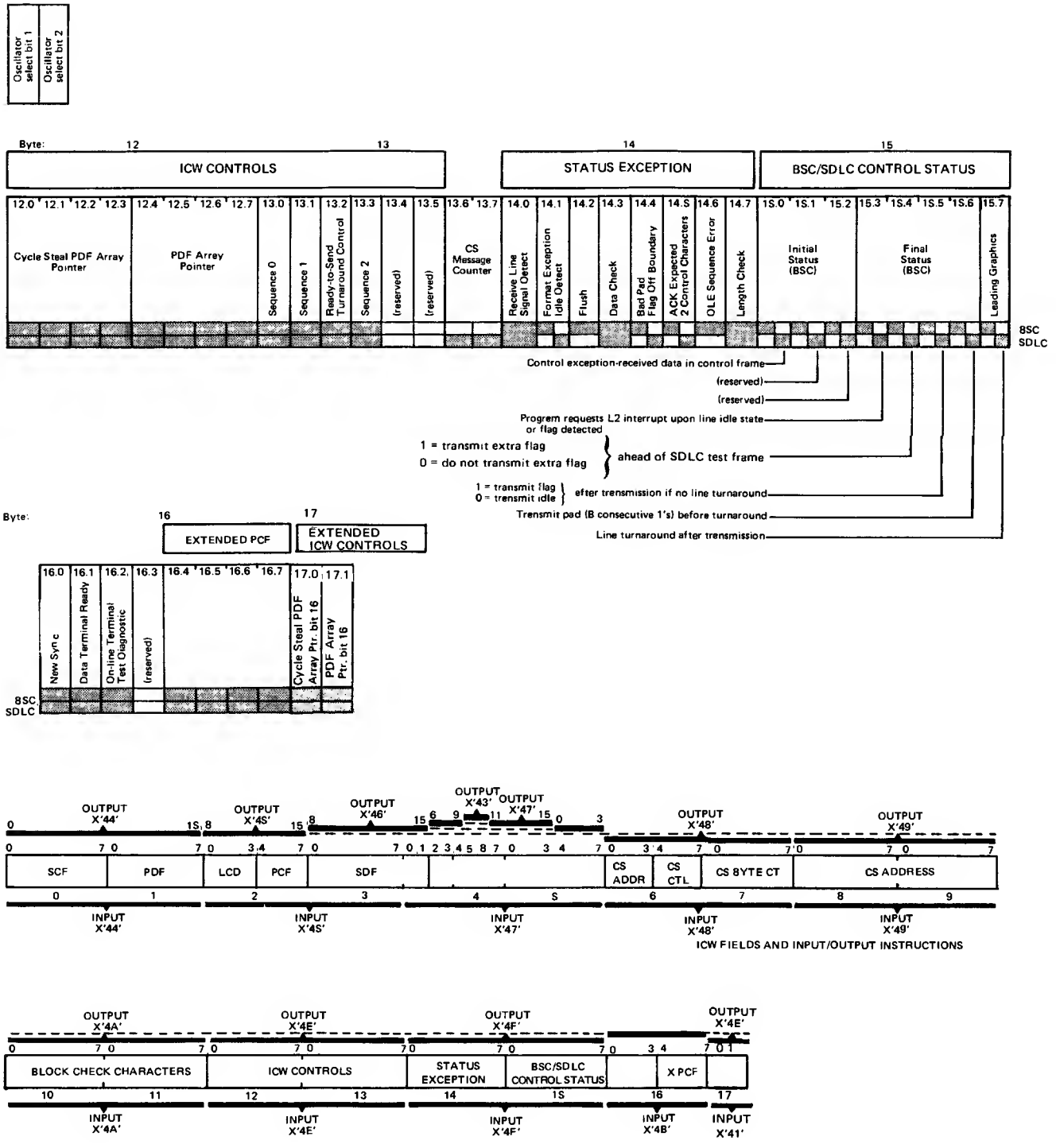


Figure 8-5. Interface Control Word Type 3 and Type 3HS Scanner (Part 2 of 2)

ICW Modification

Program access to the various fields in the ICW is through the use of input and output instructions. When the Input X'44'–X'4F' instructions are executed, the ICW bits assigned to those inputs are placed in the register specified in the R operand. See Appendix B for the input/output instruction bit definitions.

The information obtained by the input instructions comes from the ICW input register. There is one ICW input register in each communication scanner. This register is automatically loaded from the ICW work register when a level 2 interrupt occurs or when an Output X'40' instruction is executed in any program level other than level 1 or 2.

The ICW input register does not necessarily reflect the current state of the ICW associated with the interface address in ABAR. The actual ICW may have been modified by the scanner during scan addressing after the ICW input register was set.

Also, the actual ICW may have been altered by the execution of an Output X'43'–X'4F' instruction. Subsequent input instructions do not include these alterations because the ICW input register had been set by a previous Output X'40' instruction or scanner level 2 interrupt. In the event that an output instruction and scan addressing both occur during the same scan cycle, the output instruction is executed first; then the scanner performs its modification, if needed. This ensures that the latest modifications to the actual ICW will be included during the next scan addressing operation.

Refer to *Interface Control Word Format* in this chapter for a complete description of the individual ICW fields and the I/O instructions associated with each field.

Programming Note

Since the interface control words are asynchronously interrogated and modified by both the scanners and the control program, caution should be observed to ensure the ICW integrity when the program issues an output instruction. The scanner cannot check whether the control program has modified the ICW correctly. Therefore, errors in the modification itself may be difficult to isolate. To prevent control program modifications to the ICW (via output instructions) from being destroyed by the scanner, program modifications are not permitted during that portion of a scan when the scanner fetches, modifies, and restores the ICW for the line being scanned.

Interface Control Word Format

This section describes the ICW fields and their bit meanings. (See Figure 8-5.)

ICW Bits 0.0-0.7 (Secondary Control Field): The secondary control field (SCF) is used as a sense, status, and operation modifier field between the control program and the communication scanner. Bits 0.0-0.5 are set by the scanner hardware according to the conditions described below. Bits 0.6 and 0.7 are program controlled. This field may be tested by using the Input X'44' instruction. An Output X'44' instruction is used to reset bits 0.0-0.3 and 0.5, to set bit 0.4, and to set and reset bits 0.6 and 0.7. Refer to Appendix B for bit definitions of Input/Output instructions.

Bit 0.0–Abort Detected: The scanner sets this bit to 1 when it detects seven consecutive 1 bits in the received data stream while the PCF state is X'6' or X'7'. If this bit is 1, the service request interlock (ICW bit 0-1) is forced to 0. Bit 0 must be reset by the control program using an Output X'44' instruction.

This bit has no significance during a transmit operation.

Note: *A transmitted abort sequence consists of eight consecutive 1 bits. However, if the scanner detects seven consecutive 1 bits while receiving data, it will set the abort bit (ICW bit 0.0) to 1.*

Bit 0.1–Normal Service Request Interlock: This bit is set when the scanner detects that buffer servicing or control servicing is required between the control program and the addressed ICW. The control program must reset this bit after the interrupt is honored and all bits or bytes of the ICW have been modified. If this bit is already set when the scanner is prepared to set it on, and the scanner is in a transmit or receive state, a character overrun/underrun flag is set (ICW bit 0.2).

If this bit is 1, ICW bits 0-0, 0.2, 0.3, 14.1, 14.3, 14.4, 14.6, and 14.7 are 0.

Programming Notes

1. The control program should reset the normal service request interlock before setting the PCF state to monitor modem or autocall unit control lines.
2. For level 2 interrupt routines that change the cycle steal address and count, the cycle steal valid bit should be set before the normal service request interlock bit is reset.
3. An Output X'44' instruction that resets the normal service request interlock and/or EOM bits should be the last Output instruction executed for the scanner in program level 2.

Bit 0.2–Character Overrun/Underrun: This bit is set when the scanner attempts to set the service request interlock (ICW bit 0.1) and finds it already set. This error is normally caused by an instantaneous peak overload situation. Errors of this type should not occur in the average installation and should occur only infrequently in high-throughput installations.

If a character overrun occurs, the next character received overlays the previously received character in the PDF array. Thus, one or more characters are lost. When this occurs, the flush bit (ICW bit 14.2) is set, the PDF array is reset, and all subsequent data received is discarded until an ending sequence is received. At that point, the EOM bit (0.5) and the character overrun/underrun bit (0.2) are set.

If an underrun occurs (possible only on an SDLC transmit line), an Abort character is transmitted and the EOM and overrun/underrun bits are set.

An underrun condition cannot occur on a BSC line because the scanner automatically transmits SYN characters (non-transparent text) or DLE SYN sequences (transparent text) until the control program sets up another cycle steal operation.

If this bit is 1, the service request interlock (ICW bit 0.1) is 0.

Bit 0.3–Modem Check: During each bit interval (bit service time), the scanner checks the line interface for the proper modem conditions. This bit is set to 1 to indicate the following conditions:

1. The 'data set ready' line is inactive when the PCF field of the ICW is in states X'5', X'6', X'7', X'8', X'9', X'A', or X'B'.
2. The 'clear to send' line is inactive when the PCF field of the ICW is in states X'9' or X'B'.

If this bit is 1, the service request interlock (ICW bit 0.1) is 0.

Bit 0.4–Not Level 2 Bid: This bit is set whenever an Output X'44' instruction is executed, regardless of the contents of the register specified by R. It is reset by the scanner when a level 2 bid is accepted by the interrupt priority register of the Type 2 Attachment Base. When reset, this bit prevents the scanner from making another level 2 interrupt request for the line.

Bit 0.5–End-of-Message Interrupt: This bit is set to 1 by the scanner to indicate the end of a received or transmitted message. If both this bit and bit 0.1 are 1, the receive or transmit operation ended normally. The operation ended abnormally if both this bit and bit 0.0, 0.2, 0.3, 14.1, 14.3, 14.4, 14.6, or 14.7 are 1.

During an SDLC receive operation, the scanner sets this bit after storing the received data and checking the block check characters (BCC). During an SDLC transmit operation, the scanner sets this bit after sending an ending control character.

During a BSC receive operation, the scanner sets this bit upon detecting an ending sequence after the received data is stored and the BCC is checked. During a BSC transmit operation, the scanner sets this bit after transmitting the ending characters and BCC.

Bit 0.6–Program Flag: This bit provides a flag in the ICW that can be used by the control program for any desired purpose. It is not used by the scanner.

Bit 0.7–Line Trace Active: The control program sets this bit (SDLC only) to indicate to the scanner that the line represented by the ICW is to be traced. When this bit is set, the scanner stores the received BCC characters.

ICW Bits 1.0-1.7 (Parallel Data Field): The parallel data field (PDF) provides a path for diagnostic programs to alter the contents of the PDF array. An Output X'44' instruction in which bit 0.4 is on will store byte 1 of the register specified by R at the location specified by the PDF array pointer (ICW bits 12.4-12.7 for Type 3 Scanners, and 17.1 and 12.4-12.7 for Type 3HS Scanners). (Bit 0.4 need not be on to write autocall dial digits into the PDF (LCD state X'3' or X'B'.) The PDF array is normally loaded and unloaded automatically by the scanner in a manner that provides bytes of buffering between a cycle-steal operation to or from storage for receiving or transmitting data over the line. (See Note)

For an autocall interface, a dial digit must be placed in the PDF as shown in Figure 8-5.

Note: *Although referred to as ICW bits 1.0-1.7, the PDF for Type 3 Scanners is actually one of the eight elements (PDFs) of the PDF array. For Type 3HS Scanners, the PDF array consists of 16 elements.*

ICW Bits 2.0-2.3 (Line Control Definer): The line control definer (LCD) field defines the type of interface associated with the ICW. The LCD, set under program control by an Output X'45' instruction, must be in agreement with the installed interface type and the common-carrier or IBM equipment physically attached to the interface. The LCD field definition must also agree with the basic line control procedures to be executed. An LCD is generally set at initial program load (IPL) time and remains the same throughout normal operation.

The values of the LCD field are defined in detail, along with the effect of the LCD on the PDF and SDF fields, in the section describing LCD states.

ICW Bits 2.4-2.7 (Primary Control Field): The primary control field (PCF) defines the state of the interface at any particular time. An extended PCF is located in ICW bits 16.4-16.7; the extended PCF allows further differentiation of the basic PCF states. The interpretation of the PCF and extended PCF fields depends on the state of thc LCD. (See the section *Autocall Interface Operation* for a description of the PCF states for an autocall interface.)

The Output X'45' instruction can be used to set the state of the PCF and extended PCF. Also, an Input X'45' instruction can be executed to test the state of the PCF fields; an Input X'4B' can be used to test the extended PCF. Refer to Appendix B for bit definitions of Input and Output instructions.

ICW Bits 3.0-3.7, 4.0-4.1 (Serial Data Field): The serial data field (SDF) is primarily used as a character deserializer/serializer field. On receive operations, the data arriving from a line is placed in this field bit by bit to assemble a character. Once assembled, the character is transferred, under hardware control, to the PDF for transfer to 3705 storage via a cycle steal operation. For transmit operations, a character from the PDF is transferred into the SDF under hardware control and then transferred bit by bit to the line interface hardware.

The SDF is also used for autocall operations and for setting certain ICW bits using the Set Mode command. The SDF format depends on the values in the LCD and PCF fields. See *Interface Mode Set* and *Autocall Interface Operation* in this chapter for further definitions. Program access to the SDF is through Input X'45' and X'47' instructions. The SDF can be modified by an Output X'46' instruction. Refer to Appendix B for bit definitions of Input and Output instructions.

ICW Bits 4.2-4.4, 4.7, 5.0 (Ones Counter/Interval Timer): For SDLC, these five bits are used as a ones counter. This counter is incremented and reset by the scanner hardware. During a receive operation, this counter is used to detect:

- Inserted 0's that are to be deleted from the received bit stream while in PCF states X'6' and X'7'.
- Flag sequences (X'7E') occurring while in PCF states X'5' X'6', and X'7'.
- Abort sequences (seven consecutive 1 bits) received while in PCF states X'6' and X'7'.
- Idle sequences (fifteen consecutive 1 bits).

During a transmit operation, this counter is used to:

- Insert a 0 bit after each five consecutive I bits transmitted. This applies to PCF states X'9' and X'B' under certain extended PCF states.
- Generate a minimum of fifteen consecutive 1 bits for a line idle state.

For BSC, these five ICW bits are used as an interval timer to provide standard one- and three-second BSC timeouts.

ICW Bit 4.5 (Last Line State/Timeout Control): During an SDLC operation, this ICW bit retains the state of the last data bit transmitted or received between the scanner and the LIB. For BSC, this ICW bit is compared to the timer change latch and, if it is found to be different, causes the interval timer bits of the ICW (bits 4.2, 4.3, 4.4, 4.7, 5.0) to be incremented. This ICW bit is set to the same value as that of the timer change latch.

ICW Bit 4.6 (Display Request): This bit allows the state latches in the interface hardware and certain modem (or Autocall unit) signals to be loaded into the scanner display register when the interface associated with this ICW is scanned. The bit may be set and reset by an Output X'43' instruction when the interface address for that ICW is in the attachment buffer address register (ABAR) in the Type 2 Attachment Base.

The contents of the display register in a particular Scanner can be accessed by an Input X'46' instruction when that scanner is selected.

Because each scanner has only one display register, the program should ensure that the display request bit is never on in more than one ICW in each scanner. Only in this way can the information in the display register be meaningful.

Before executing an Input X'46', the program must also ensure that enough time has elapsed to guarantee that a bit service has occurred for the interface after setting the display request bit in the ICW associated with the interface. (See also the section *Display Register* earlier in this chapter.)

ICW Bits 4.7, 5.0: (See ICW Bits 4.2–4.4).

ICW Bit 5.1 (Level 2 Interrupt Pending): This bit is set:

- When the interrupt priority register (IPR) assigned to the interface is already occupied by another interface. This stacks the new interrupt until the next time the line is scanned and the IPR is not occupied.
- When the scanner wishes to interrupt the program to obtain another data buffer or a control byte is detected in the PDF array.

ICW Bits 5.2-5.3 (Priority Select Bits 1 and 2): These bits assign to the ICW for the interface one of the four interrupt priority registers inthe attachment base. All bit combinations are valid, with X'0' designating the lowest priority register and X'3' the highest.

ICW Bit 5.4 (NRZI Control/Transparent Text): For SDLC, when this bit is on and the PCF state is X'9' or X'B', the data that is transmitted is in NRZI mode (non-return-to-zero-inverted). When this bit is off, the data is transmitted in normal mode (with 0 and 1 bits unchanged by the scanner).

(In NRZI mode, the line level is complemented when a 0 is transmitted and unchanged when a 1 bit is transmitted. NRZI mode and zero insertion after five consecutive 1 bits ensure the occurrence of a line transition [that is, from 0 to 1 or 1 to 0] at least once every six bits regardless of the data pattern. NRZI mode is used to ensure bit synchronization when using modems that do not provide clocking for received data (or modems that are bit sensitive).

For BSC, this bit is turned on when transparent text transmission begins and is turned off when transparent text transmission ends. While transmission is in transparent text mode, normal BSC control characters are not recognized by the scanner.

This bit is set or reset from bit 0 of the serial data field (SDF) when a set mode operation is executed. SDF bit 0 is set by an Output X'46' instruction in which bit 0.0 is set. The control program should not set this bit for a BSC line.

ICW Bits 5.5-5.6 (Diagnostic Bits 0 and 1): These bits are set from SDF bits 1 and 2 when a set mode operation is executed. SDF bits 1 and 2 are set by an Output X'46' instruction in which bits 0.1 and 0.2 are on.

Diagnostic bit 0 is used to place a line interface in scanner wrap mode. Diagnostic bit 1 is used to inhibit the insertion and deletion of control characters for a line address, as follows. When bit 1 is on for a transmit operation, the scanner is inhibited from inserting SYN characters, 0-bits, and flag characters. When bit 1 is on for a receive operation, the scanner is inhibited from deleting all control characters and 0-bits.

These bits are on only for diagnostic operations; for normal data transmission they should be off.

ICW Bit 5.7 (External Clock): This bit is set from SDF bit 6 (ICW bit 3.6) when a set mode operation is executed. The bit in the SDF is set by an Output X'46' instruction in which bit 1.4 is on.

This bit is used by the scanner to control the type of bit synchronization to be used for the modem attached to the line interface associated with the ICW.

ICW Byte 6: (Cycle Steal Control): This byte contains control and addressing information for cycle steal operations of the scanner.

Bits 6.0-6.3 (Cycle Steal Address Byte X): These four bits contain the four high-order bits of the cycle steal address.

Bit 6.4 (ETB/ETX/ENQ in data): This bit is used as an internal control by the scanner. The scanner sets this bit while cycle stealing data from storage upon detecting an ETB, ETX, or ENQ character in transmitted data. If this bit is on when the scanner enters transparent text mode (setting bit 5.4), the cycle steal valid bit (6.5) is set because the ETB, ETX, or ENQ is actually transparent text and not an ending control character. The control program must reset this bit when the next interrupt for the line occurs.

Bit 6.5 (Cycle Steal Valid): This bit is set by the control program to signal the scanner that the cycle steal address, byte count, and transmit data chain bits are valid for use by the scanner. The program must update the cycle steal address bytes before setting this bit.

The scanner resets this bit when:

- The byte count reaches 0.
- An end-of-message character has been received and the scanner detects an EOM control byte in the PDF array.
- An end-of-message character is detected in the data stream when fetched from the CCU storage via a cycle-steal operation.

Note: *An Output X'48' that sets cycle steal valid should always be followed by an Output X'44' to reset the SCF bits in order to prevent possible double interrupts. This sequence normally occurs just prior to exiting from a program level 2 interrupt service.*

Programming Note

Care must be exercised to ensure that this bit is off before any modification is made to the LCD and PCF fields.

Bit 6.6 (Transmit Data Chain Flag): This bit is set by the control program when additional data is to be transmitted from another buffer. If this bit is off and the byte count reaches 0, indicating that the last byte of the message has been transferred to the scanner, the scanner examines the final status byte to determine which ending sequence to initiate. The level 2 interrupt is delayed until the ending sequence is completed.

Bit 6.7 (SDLC Transmit Message Chain Flag): This bit is set by the control program (for SDLC transmission only) when the buffer currently being transmitted represents the end of the message but another message is in the transmit queue. The scanner transmits the CRC and flag characters after all message data in the parallel data fields (PDF) have been transmitted. A level 2 interrupt is made for the cycle steal address to start transmission of the next message.

ICW Byte 7 (Cycle Steal Byte Count): This eight-bit field contains the data byte count of the buffer currently allocated to the ICW. In receive mode, the control program allocates a new storage buffer as needed by setting the cycle steal count to the number of character spaces the control program has made available.

In transmit mode, the program must set the cycle steal byte count to the number of data characters to be transmitted from the storage buffer. The maximum byte count is 255 bytes. The byte count should be set equal to the buffer size if the number of characters remaining to be transmitted exceeds the buffer size; the count should be set equal to the remaining number of bytes, if this value is less than the buffer size.

When the count reaches zero, the scanner issues a level 2 interrupt request according to the setting of the data chain and message chain flags. (Bit 7.0 is the high-order bit of the counter.)

During a transmit operation, the byte count is decremented by one for each data character fetched from storage and placed in the PDF array. During a receive operation, the counter is decremented by one for each character transferred from the PDF array to CCU storage.

ICW Bytes 8 and 9 (Cycle Steal Address): These two bytes contain the low-order sixteen bits of the cycle-steal address. This address (together with ICW bits 6.0-6.3) contains the current address for data to be fetched from or stored into main storage. As each byte is stored or fetched, the address is incremented by one. The scanner normally transfers two bytes at a time to or from storage.

ICW Bytes 10 and 11 (Block Check Characters [BCC]): The block check characters are accumulated in these two bytes for SDLC operation or for BSC operation using either the EBCDIC or ASCII codes.

Byte 12 (ICW Controls)

Bits 12.0-12.3 (Cycle Steal PDF Array Address): This field of four bits points to the PDF array address currently associated with the cycle steal data registers. In a transmit PCF state, this address is the next address to be used when transferring data from the cycle steal data register to the PDF array. An Output X'4D' instruction stores byte 0 at the location addressed by the cycle steal PDF counter and byte 1 at that location plus one. The addressed location plus two is stored back in ICW bits 12.0-12.3 for the next operation.

For information pertaining to Type 3HS Scanner operations, refer to "Byte 17 (ICW Controls Extended)" later in this chapter.

Bits 12.4-12.7 (PDF Address): This field of four bits points to the PDF array address currently associated with the serial data field (SDF). In a receive PCF state, this is the next address to be used when transferring data from the SDF to the PDF. An Output X'44' instruction in which bit 0.4 is on stores byte 1 at the location specified by the PDF array counter. An Output X'4C' instruction stores eleven bits at the location specified by the PDF array counter. Neither instruction increments the counter.

When a fetch buffer signal is generated (entering level 2 or executing Output X'40' in level 3 or 4), the input register is loaded with the contents of the PDF array address pointed to by the PDF array counter. Input X'44' or X'4C' instructions are used to read byte 1 or all eleven bits of this PDF address, respectively.

For information pertaining to Type 3HS Scanner operations refer to "Byte 17 (ICW Controls Extended)" later in this chapter.

ICW Byte 13 (ICW Controls)

Bit 13.0 (Sequence 0): This bit is used by the scanner for additional control within an extended PCF state. This bit is normally set for the first character of a two-character sequence and reset for the second character.

Bit 13.1 (Sequence 1): For SDLC receive operations, the scanner sets this bit to enable the cycle steal interface. This bit is not used for SDLC transmit operations.

For BSC receive operations, this bit is set when an ITB is received as the text ending character. When set, this bit prevents storing of the BCC characters when trace bit (ICW bit 0.7) is on. For BSC transmit operations, this bit is set when an ITB is transmitted as the text ending character. When this bit is set and the ending status byte (ICW byte 15) indicates skip after ITB, the scanner increments the PDF pointer so that the byte following the ITB is not transmitted.

Bit 13.2 (RTS Turnaround Control): The control program sets or resets this bit, which is used by the scanner to control the Request-to-Send (RTS) lead in the modem interface when changing from a transmit state to a receive state. When this bit is off, the RTS lead becomes inactive when the transition occurs. The control program must exercise caution when changing this bit; it should be set or reset only when the line is in a "no-op" state (PCF state 0).

Bit 13.3 (Sequence 2): For SDLC receive operations, the scanner sets the bit upon detecting an ending Flag character for a supervisory or non-sequence frame if no data bytes were received. This action allows the PDF array pointer to be decremented by two so that the BCC characters are not stored. At the next bit service, this bit causes the BCC to be checked and the EOM and BCC check result to be set in the PDF array as a control byte. At this time the scanner resets the bit. This bit is not used for SDLC transmit operations.

For BSC receive operations, the scanner sets this bit upon receiving the first data character after an SOH or STX character. If the LCD state for the line is for NCP mode

this bit causes a level 2 interrupt request for a data buffer when the first non-control character is received. The bit is then reset. If the LCD state is for emulation mode (bit 2.0 is 0), the level 2 interrupt request is not made.

This bit is also set when the last BCC character is received. At the next bit service, the BCC is checked and the EOM and BCC check results are set in the PDF array as a control byte. Then the bit is reset.

This bit is unused for BSC transmit operations.

Bits 13.4-13.5 (Reserved)

Bits 13.6-13.7 (Message Counter): The scanner uses these bits to keep track of multiple SDLC messages that may be queued in the PDF array during a receive operation. The counter is incremented by one when the scanner detects an information or control frame. So long as the counter is not equal to zero, a cycle steal operation can be activated. When an EOM (end-of-message) status is set in the ICW, the counter is decremented by one.

The message counter is not used for SDLC transmit or for BSC operations.

ICW Byte 14 (Status Exception)

Bit 14.0 (Receive Line Signal Detected): The scanner sets this bit to 1 at bit service time when the CF (carrier detect) lead from the modem is active and is reset when the CF lead becomes inactive.

Bit 14.1 (SDLC Idle Detect/BSC Format Exception): For SDLC receive operations the scanner sets this bit upon detecting an idle-line condition while receiving a frame. ICW bit 0.0 (Abort Detect) is also set in this case. Bit 14.1 is also set if the scanner is in PCF/EPCF state X'7'/'7', ICW bit 15.3 is on, and a line-idle condition is detected. A level 2 interrupt request is also generated.

This bit is unused for SDLC transmit operations.

For BSC receive operations, this bit is set when the scanner is in PCF/EPCF state X'5'/'01' and an ITB, ETB, or ETX character is received, or in PCF/EPCF state X'7'/'02' and an ITB, ETB, ETX, SOH, or STX character is received, or in PCF/EPCF state X'7'/'03' and an SOH character is received.

For BSC transmit operations, this bit is set when the Type 3 Scanner is in PCF/EPCF state X'9'/'02' or X'9'/'04' and the initial or final control sequence should be set in the SDF but is not specified by ICW byte 15. If this bit is on, ICW bit 0.1 is reset.

This bit is reset by an Output X'4F' instruction in which bit 0.1 is set.

Bit 14.2 (BSC Flush): This bit is set by the control program to inform the scanner to flush the received data. When this bit is on, the scanner discards data received from the line until it detects an ending control sequence.

Bit 14.3 (Data Check): This bit is set on by the scanner upon detecting a bad BCC character in the received data stream. If this bit is on, ICW bit 0.1 is reset. The data check bit is reset by an Output X'4F' instruction in which bit 0.3 is on.

Bit 14.4 (Bad Pad/Flag Off Boundary): For BSC, this bit is set when the next character received after an ending sequence is not a valid pad character. This bit is not set, however, if the ending sequence includes BCC characters.

For SDLC, this bit is set when a flag byte detected in received data is not on a character boundary. If this bit is on, ICW bit 0.1 is reset. This bit (14.4) is reset by an Output X'4F' instruction in which bit 0.4 is set.

Bit 14.5 (Ack Expected): For SDLC, the control program sets this bit to indicate to the scanner to expect multiple control (C) bytes. When this bit is on, the scanner expects two control bytes to follow the address (A) byte.

For BSC, the control program sets this bit to indicate which BSC Ack response is expected. If the bit is 0, an Ack-0 is expected; if it is 1, an Ack-1 is expected. An Output X'4F' instruction is used to set or reset this bit; the state of bit 0.5 of the instruction determines the state to be placed in bit 14.5.

Bit 14.6 (DLE Sequence Error): The scanner sets this bit upon receiving an invalid control character following a DLE character (for example, SOH or STX following a DLE character are considered invalid control characters when receiving a leading graphics sequence.) This bit is set by the scanner and reset by an Output X'4F' instruction in which bit 0.6 is on. (This bit is not used for SDLC operations.)

Bit 14.7 (Length Check): For SDLC, the scanner sets this bit upon detecting an ending flag after the address and control (AC) characters are received but before two more characters have been received.

For BSC, the scanner sets this bit upon detecting an ETB or ETX character in the transmitted data stream, if the LCD state does not indicate operation in emulation mode. (This bit is not set if the scanner detects ETB or ETX as part of a leading graphics sequence.) This bit is set by the scanner (when set, it forces the scanner to reset ICW bit 0.1) and is reset by an Output X'4F' instruction in which bit 0.7 is on.

ICW Byte 15 (Status Byte): For BSC, the scanner uses this byte during a transmit operation to determine the correct starting and ending control sequence to send, and during a receive operation to indicate to the program the control sequence that has been received. See the section

ICW Status Byte later in this chapter for the meanings of the status byte states.

For SDLC transmit operation, the control program sets the status byte to specify the action the scanner is to perform at the end of an SDLC frame:

Bits 15.0-15.3: (not used in transmit operations)

Bit 15.4 (Extra Flag): When this bit is set, the scanner transmits an extra flag ahead of an SDLC frame. The extra flag is not transmitted when this bit is off.

Bit 15.5 (Flag): When this bit is set, the scanner transmits consecutive flag characters at the end of the SDLC frame if no line turnaround is to be executed. When the bit is reset, the scanner transmits an ending flag followed by idle characters.

Bit 15.6 (Transmit Pad): When this bit is set, the scanner sends an all-ones character (eight consecutive one bits) before turning the line around. (See also bit 15.7.)

Bit 15.7 (Line Turnaround after Transmission): When this bit is set, the scanner changes from a transmit to a receive state after sending the frame.

For SDLC receive operation, the scanner sets the status byte to inform the control program of unusual conditions:

Bit 15.0 (Control Exception): The scanner sets this bit wher a control frame was indicated by the C (control) byte but the flag character was not received three bytes later.

Bit 15.1: (reserved)

Bit 15.2: (reserved)

Bit 15.3 (Idle): The control program sets this bit to request a level 2 interrupt if the receive line enters an idle state or the scanner detects a flag character.

Bits 15.4-15.7: (not used in receive operations)

ICW Byte 16

Bit 16.0 (New Sync): The scanner uses this bit to control the 'new sync' lead in the attached modem. The scanner sets this bit immediately after transmitting the first SYN character (BSC) or a flag character (SDLC) if the PCF state is X'B'. The scanner resets the bit upon transmitting the second BCC character if the PCF state is X'B'. (The program should use this bit only when the scanner is in ICW diagnostic mode.)

Bit 16.1 (Data Terminal Ready [DTR]): This bit is set or reset in accordance with the setting of ICW bit 3.4 (set/reset DTR) when a Set Mode command is executed. When this bit is on, the scanner does not force the clear-to-send condition when the line is in diagnostic mode. This bit can also be set with an Output X'45' instruction if bits 0.0 and 0.1 are set.

Bit 16.2 (OLTT Diagnostic): This bit is set or reset with an Output X'45' instruction according to the state of byte 0, bit 2 of the instruction if byte 0, bit 0 is set. When this bit (16.2) is set, the scanner does not reset the BCC characters before accumulating a new BCC. This action permits the OLTT program to transmit a message having a bad BCC value.

Bit 16.3: (reserved)

Bits 16.4-16.7 (Extended PCF): These bits contain the extended PCF field; the meanings of the states of this field are given under PCF/EPCF States later in this chapter.

Byte 17 (ICW Controls Extended - Type 3HS Scanner Only)

Bit 17.0 (Cycle Steal PDF Array Address): This bit, when combined with bits 12.0-12.3 of the ICW controls field, points to the PDF array address currently associated with the cycle steal data registers. This bit is used only for Type 3HS Scanner operations. In a transmit PCF state, this address is the next address to be used when transferring data from the cycle steal data register to the PDF array. An Output X'4D' instruction stores byte 0 at the location addressed by the cycle steal PDF counter and byte 1 at that location plus one. The addressed location plus two is stored back in ICW bits 17.0 and 12.0-12.3 for the next operation.

For information on ICW controls for Type 3 Scanner operations, refer to *Byte 12 (ICW Controls)* and *Byte 13 (ICW Controls)* earlier in this chapter.

Bit 17.1 (PDF Address): This bit, when combined with bits 12.4-12.7 of the ICW controls field, points to the PDF array address currently associated with the serial data field (SDF). This bit is used only for Type 3HS Scanner operations. In a receive PCF state, this address is the next address to be used when transferring data from the SDF to the PDF. An Output X'44' instruction, in which bit 0.4 is on, stores byte 1 at the location specified by the PDF array counter. An Output X'4C' instruction stores eleven bits at the location specified by the PDF array counter. Neither instruction increments the counter.

When a fetch buffer signal is generated (entering level 2 or executing Output X'40' in level 3 or 4), the input register is loaded with the contents of the PDF array address pointed to by the PDF array counter. Input X'44' or X'4C' instructions are used to read byte 1 or all eleven bits of this PDF address, respectively.

For information on ICW controls for Type 3 Scanner operations, refer to Byte 12 (ICW Controls) and Byte 13 (ICW Controls) earlier in this chapter.

Line Control Definer (LCD) States

This section describes the various states of the line control definer (LCD) field. This field is used during normal transmit and receive operations to define the hardware line control required by the type of line set associated with the interface control word.

Where the LCD states are shown in pairs, for example, X'5' and X'D', the first state applies to operation of the interface in emulation mode and the second applies to operation in network control mode.

LCD States X'0', X'1', X'2', X'7', X'8', X'A', X'B', and X'E': (Reserved)

LCD State X'9': This state causes the scanner to block all characters into eight-bit bytes and to search for SDLC control characters (Flag, Abort, Idle).

LCD State X'3': This state is for Autocall interfaces only. See the *Autocall Interface Operation* section in this chapter.

LCD States X'4' and X'C' (BSC EBCDIC Line Control): These states provide for serializing and deserializing eight-bit characters and searching for EBCDIC line control characters. LCD state X'4' is used for emulation mode operation in which initial and final control characters are stored in or fetched from data buffers.

LCD States X'5' and X'D' (BSC ASCII Line Control): These states have the same purpose as states X'4' and X'C' except that the scanner searches for ASCII control characters.

LCD State X'6' (BSC Transparent ASCII Line Control): This state has the same purpose as state X'5' except that it accommodates transmission of transparent text. The scanner accumulates a cyclic redundancy check (CRC) character instead of the longitudinal redundancy check (LRC) character.

LCD State X'F' (Feedback Check): The scanner sets this state in the LCD upon detecting a feedback check error (1) during scan addressing on any of the scanner 'data in' lines from the selected LIB, or (2) when a bit service reset error is detected on the line from the selected LIB. A set mode operation for an interface that has been incorrectly configured also sets this state.

Primary Control Field (PCF) States

This section describes the states of the primary control field (PCF) and extended PCF (EPCF) for BSC and SDLC lines.

PCF State X'0' (No-Op): This PCF state causes the Scanner to take no action (active or passive) upon subsequent scans. The scanner hardware can request a Type 3 Scanner L2 interrupt and set this PCF state for an interface if it determines that new control information is required from the control program. This PCF state can be set by the control program; however, no interrupts are generated by the interface.

PCF State X'1' (Set Mode): This PCF state causes the scanner to set and reset certain mode latches in the line interface hardware. These latches are specified by the SDF field. When setting this PCF state, the control program must ensure the integrity of the entire ICW. This may be done by first setting the PCF to state X'0' (no-op) so that the ICW will not be modified by a possible interrupt. The SDF can then be set to the proper value via Output X'46'. Finally, state X'1' (set mode) can be set into the PCF field. Execution of a set mode does not require a bit service request from the addressed interface. However, a bit service request must occur to allow the scanner to request a L2 interrupt to end the set mode operation. The set mode operation ends when the scanner hardware sets the PCF state to X'0' (no-op).

A set mode can be executed to change the state of the data rate selector bit and the oscillator select bits without requiring a disable. However, 'data terminal ready' must remain on.

PCF State X'2' (Monitor Data Set Ready): This PCF state places the interface in a wait-for-incoming-call condition. For switched lines, this state should normally be set by the control program following a PCF state X'F' (disable) and PCF state X'1' (set mode with data terminal ready bit = 1). When an interface is in this state, the scanner tests the 'data set ready' lead from the common carrier or IBM line adapter for an active condition when the ICW is fetched. When data set ready is *on*, indicating that a call is established, the scanner sets PCF state X'4' (monitor phase-data set ready check off) and requests an L2 interrupt.

Though not necessary, this state can also be used for leased lines. Data set ready should be on at the first bit service request when the interface is scanned.

PCF State X'3' (Monitor Ring Indicator or Data Set Ready): This PCF state, when set by the control program, places the line interface in a wait-for-incoming-call (ring indicator *on*) or wait-for-manual-call-out-connection condition (data set ready *on*). This state must be preceded by setting PCF state X'F' (disable), or a set mode that resets data terminal ready. When the PCF state is set to X'3', the Scanner tests the 'ring indicator' and 'data set ready' leads from the common carrier equipment for an active condition of either lead. When 'ring indicator' is active, a call is coming in and a pending connection is to be established. When either of these conditions occurs, the Scanner sets PCF state X'0' (no-op) and places the line in a L2 interrupt pending state. This PCF state must be followed by PCF state X'1'

(set mode) from the control program to set the 'data terminal ready' latch. After the scanner executes the set mode, it sets PCF state X'0' (no-op) and places the line in a L2 interrupt pending state. The interrupt handling program must then place the line in PCF state X'2' (monitor data set ready on), after which the operation proceeds as described in *PCF State X'2'–Monitor Data Set Ready.*

PCF State X'4'/EPCF State X'0' (Monitor Phase–Data Set Ready Check Off): This PCF state is identical to PCF state X'5' (BSC–monitor phase-data set ready check *on*) except that the inactive condition of 'data set ready' does not signal a check condition. PCF X'4' is intended to initialize the *first* receive operation after a switched network call connection has been established.

PCF/EPCF States–BSC

This section contains the PCF states X'5' through X'B' and associated EPCF states for BSC lines.

PCF/EPCF State X'5'/'0' (Monitor Phase–Data Set Ready Check On): This PCF/EPCF state places a BSC line into a *hunt for phase* condition. The SDF field is shifted each bit interval time, and the contents are examined by the scanner hardware for a comparison with the bit configuration of the 8-bit SYN character. If a compare is successful, PCF/EPCF state X'5'/'1' is set, the tag bit is inserted in the SDF, and the sequence 0 bit (ICW bit 13.0) is set.

PCF/EPCF State X'5'/'1' (Character Phase): In this state, with the Sequence 0 bit (ICW bit 13.0) set, character phase is monitored to detect a second SYN character. Upon detecting this character, the scanner hardware resets the Sequence 0 bit. The scanner then decodes the next character assembled in the SDF. Depending upon the character received the PCF/EPCF state changes to X'7'/'2' (Receive Leading Graphics), X'7'/'3' (Receive Control), X'7'/'4' (Receive Data), or (with the Sequence 0 bit off) X'7'/'6' (Receive Ending Pad).

PCF State X'7' (Receive Data): In this state, the scanner is in phase and is receiving control (C) and data characters. The scanner encodes the control characters and stores them in ICW byte 15, and stores data characters in main storage under cycle steal control. If the cycle steal byte count reaches zero or the scanner detects an ending control condition, the scanner generates a level 2 interrupt.

PCF/EPCF State X'7'/'2' (Receive Leading Graphics): This state is entered from state X'5'/'1' when the first character that is not a SYN or control character is assembled in the SDF. ICW bit 15.7 is set to indicate receipt of leading graphics. The scanner remains in this state, transferring characters from the SDF to the PDF at each character transfer time until it detects an ending character sequence. Upon detecting a single ending character, the scanner sets PCF/EPCF state X'7'/'6' (Receive Pad) and sets the appropriate final status bits (ICW bits 15.3-15.6). Upon detecting the DLE character of a two-character ending sequence, the scanner sets PCF/EPCF state X'7'/'5' (Received DLE in Leading Graphics) (with Sequence bit 0 on).

PCF/EPCF State X'7'/'3' (Receive Control Sequence): This state is entered from state X'5'/'1' when the first non-SYN character assembled in the PDF is a DLE. The scanner changes states at the next character transfer time unless it receives another DLE. If the second character of an ACK, WACK, RVI, DISC, or Stick sequence is received, the scanner sets PCF/EPCF state X'7'/'6' (Receive Pad) (with Sequence bit 0 off) and sets the appropriate final status bits (ICW bits 15.3-15.6). If the second character is a STX, the scanner sets PCF/EPCF state X'7'/'4' (Receive Text) (with Sequence bit 0 off), resets the BCC, sets Initial status (ICW bits 15.0-15.2), and sets the transparent mode bit (ICW bit 5.4).

PCF/EPCF State X'7'/'4' (Receive Text): In this state, the scanner transfers data characters from the SDF to the PDFs in the PDF array, and accumulates the block check characters (BCC). When the cycle steal byte count reaches zero, the scanner makes a level 2 interrupt request to obtain the next data buffer. This state is used for both normal and transparent text transmission.

If the scanner detects a DLE in normal text, it sets Sequence bit 0 on, transfers the character to the PDF, and accumulates the BCC. If the scanner detects a DLE in transparent text, the scanner sets Sequence bit 0 and deletes the DLE. If the scanner detects an ITB, ETB, or ETX ending sequence, the scanner sets PCF/EPCF state X'7'/'5' (Receive Ending) (with Sequence bit 0 off), sets the appropriate final status (ICW bits 15.3-15.6), and accumulates the BCC. If it receives an ENQ character, the scanner sets PCF/EPCF state X'7'/'6' (Receive Pad) (with Sequence bit 0 off), and sets final status. If it detects a time-out condition, the scanner sets PCF/EPCF state X'5'/'0' (Monitor Phase), sets final status, sets End of Message (ICW bit 0.5), and makes a level 2 interrupt request.

PCF/EPCF State X'7'/'5' (Receive Ending): In this state, the scanner is either completing the DLE sequence of a leading graphics sequence or receiving the check character of a text ending sequence.

If Sequence bit 0 is on, a DLE was received as the first ending character of a leading graphic sequence. If the second character of an ACK, WACK, RVI, DISC, or Stick sequence is received, the scanner sets PCF/EPCF state X'7'/'6' (Receive Pad) (with Sequence bit 0 off) and sets the appropriate final status (ICW bits 15.3-15.6).

If Sequence bit 0 is off, either an LRC check character (for normal ASCII transmission) or the first BCC (for EBCDIC or transparent ASCII transmission) is being

received. Upon receipt of the character, the scanner sets PCF/EPCF state X'7'/'6' (Receive BCC) (with sequence bit 0 on). If the LCD state is X'5' or X'D' (BSC ASCII line control), sequence bit 2 is set.

PCF/EPCF State X'7'/'6' (Receive BCC): In this state, the scanner is receiving either the second character of a BCC or (after a non-text ending) an ending pad character.

If sequence bit 0 is on (indicating a text ending), the next PCF/EPCF state entered is determined by the state of the sequence 1 bit. If this bit is on (indicating an ITB character), the next PCF/EPCF state will be X'7'/'4'. If sequence bit 1 is off (indicating an ETB or ETX ending), the next PCF/EPCF state will be X'5'/'0'. The sequence bit 2 is set when the last BCC character is received. For an ASCII line, this occurs on entering EPCF state X'6'; for an EBCDIC line, this occurs one character time after the last BCC character is received. On the next bit service, the BCC is checked, an EOM and BCC result control byte is written into the PDF array, sequence bit 2 is reset, and the new EPCF state is entered.

If sequence bit 0 is off, indicating a non-text ending, the scanner determines if the next four bits are all ones, indicating a Pad character. If so, an EOM control byte is written into the PDF array PCF/EPCF state X'5'/'0' is set, and a level 2 interrupt request is generated. If not, the scanner accepts the next character, sets a bad pad status indication in the PDF array, and sets PCF/EPCF state X'7'/'2'.

PCF/EPCF State X'7'/'8' (Receive Sync Idle): In this state, the scanner detects the SYN SYN or DLE SYN sequence to reset the three-second timeout (for receive operations). In this state the scanner also detects continuous SYN characters or DLE SYN sequences received for more than three seconds. The scanner then sets PCF/EPCF state X'5'/'0' (Monitor Phase), sets the appropriate final status (ICW bits 15.3-15.6), sets the end-of-message bit (ICW bit 0.5), and makes a level 2 interrupt request.

PCF/EPCF State X'7'/'C' (Receive Diagnostic Mode): In this state, the scanner stores all characters received, including SYN and DLE characters. This state is for use by diagnostic routines as a "do-nothing" state to test the scanner hardware. The scanner does not change the PCF/EPCF state while in the diagnostic mode; the control program must make any state changes required.

PCF/EPCF State X'8'/'0' (Transmit Initial): This state is set by the control program to turn on the request to send (RTS) latch and initiate text transmission. The program must initialize the following ICW fields:

- Transmit control (ICW byte 15)
- LCD (ICW byte 2)
- PCF/EPCF (ICW bytes 2 and 16)
- The low order cycle steal address (ICW byte 9)
- The cycle steal control (ICW byte 6) and cycle steal byte count (ICW byte 7). The cycle steal valid bit (ICW bit 6.5) must be set in order for the scanner to initiate a text transmission. (The cycle steal byte count should be set to zero if no data is to be transmitted.)

PCF State X'9' (Transmit Data): This PCF state is used to transmit message data and control characters, the specific kinds of characters being specified by the EPCF states. The scanner enters this state from PCF state X'8'/'0' when the 'clear to send' line of the modem interface becomes active.

PCF/EPCF State X'9'/'0' (Transmit Pad): In this serial state the scanner serializes the leading Pad character from the serial data field (SDF) to the line adapter. After the serializing is completed, the scanner sets the first clock sync or SYN character in the SDF.

PCF/EPCF State X'9'/'1' (Transmit Clock Sync): In this state the scanner serializes the clock sync characters from the SDF to the line adapter. After serializing two such characters, the first SYN character is placed in the SDF and the PCF/EPCF state is changed.

PCF/EPCF State X'9'/'2' (Transmit SYN): In this state the scanner serializes the initial SYN characters from the SDF to the line adapter. After doing so, the scanner places the first character to be transmitted in the SDF. This character is either obtained from the PDF array or generated by the scanner logic according to the current LCD state and ICW byte 15. The PCF/EPCF state is then changed to the appropriate state for the character placed in the SDF.

PCF/EPCF State X'9'/'3' (Transmit Control): In this state the scanner serializes a DLE character from the SDF to the line adapter. After serializing the character, the scanner places the next character to be transmitted in the SDF; the character is either obtained from the PDF array or generated by the scanner logic, as determined by the ICW control bits. The PCF/EPCF state is then set to serialize the character now in the SDF.

PCF/EPCF State X'9'/'4' (Transmit Text): In this state the scanner transmits message text. The scanner transfers each character from the PDF array to the SDF, from which it is serialized to the line adapter. The scanner accumulates the BCC for all characters except SYN or the first DLE character (in transparent mode). After all text characters to be transmitted have been serialized, the scanner sets the ending sequence by setting the appropriate character in the SDF and changing the PCF/EPCF state. Ending characters that the scanner detects in the data stream also cause the PCF/EPCF state to change and the ICW byte 15 to be set to indicate what ending sequence was detected.

PCF/EPCF State X'9'/'5' (Transmit End Sequence): In this state the scanner serializes the ending sequence from the SDF to the line adapter. Upon doing so, the scanner places the first BCC character or a line pad character in the SDF and changes the PCF/EPCF state.

PCF/EPCF State X'9'/'6' (Transmit BCC): In this state the scanner serializes the accumulated BCC character from the SDF to the line adapter. If the ending sequence is ITB, the last BCC character is serialized when the scanner is in PCF/EPCF state (X'9'/'4'). If the ending sequence is not ITB, an all 1's pad character is placed in the SDF after the BCC is serialized and the PCF/EPCF state is changed.

PCF/EPCF State X'9'/'7' (Transmit Final Pad): In this state the scanner serializes a Pad character comprising all 1's from the SDF to the line adapter. After transmission of this character, the scanner changes the PCF/EPCF state to X'5'/'0'. Bit 13.2 of the ICW determines when the change in state occurs. If ICW bit 13.2 is on, the scanner immediately changes the PCF/EPCF state to X'5'/'0'. If ICW bit 13.2 is off, however, the change in state does not occur until clear-to-send becomes inactive. After changing the PCF/EPCF state to X'5'/'0', the scanner sets the end-of-message bit (ICW bit 0.5) on and requests a level 2 interrupt.

PCF/EPCF State X'9'/'8' (Transmit SYN Idle): In this state the scanner serializes the first character of a SYN Idle sequence from the SDF to the line adapter. This state is entered when a one-second transmit timeout occurs in text mode. When the SYN character is set in the SDF the PCF/EPCF state is changed to X'9'/'4' and the one-second transmit timeout is started again.

PCF/EPCF State X'9'/'C' (Transmit Diagnostic Mode): In this state the scanner inhibits recognition of characters and insertion of control characters. Data from the PDF array is transmitted to the SDF to be serialized to the line adapter. After all data has been transmitted, the scanner places the line in 'mark' state before changing the PCF/EPCF state to X'9'/'7'.

PCF State X'A' (Transmit Initial with New Sync): This state is identical to PCF state X'8' (transmit initial) except that the 'new sync' interface lead to the modem will be controlled. This state must be used only with four-wire, duplex, multipoint leased-line modems where the associated interface is the master station. All of the EPCF states described for PCF state X'8' are valid for PCF state X'A'.

PCF State X'B' (Transmit Data with New Sync): This state is identical to PCF state X'9' (transmit data) except that the 'new sync' interface lead to the modem is activated when the second SYN character is transmitted and deactivated when the trailing pad character is transmitted. Activation and deactivation are controlled by the scanner's setting of ICW bit 16.0 (new sync). This state must be used only with four-wire, duplex, multipoint leased-line modems where the associated interface is the master station. All of the EPCF states described for PCF state X'9' are valid for PCF state X'B'.

PCF/EPCF States–SDLC

This section contains the PCF states X'5' through X'F' and the associated EPCF states for SDLC lines.

PCF/EPCF State X'5'/'0' (Monitor Flag–Allow Data Set Ready Check): This state is used in conjunction with LCD state X'9' to monitor received data for an SDLC flag character. To do so, the scanner uses the three low-order bits of the ones counter (ICW bits 4.2-4.4). Upon detecting a flag character, the scanner sets a tag bit in the SDF to block the next character into eight bits and enters PCF/EPCF state X'6'/'1'. If diagnostic bit 1 is set, the PCF/EPCF state is instead changed to X'7'/'C'.

PCF State X'6' (Receive Initiated): The scanner sets this state upon receiving a flag. In this state the scanner receives the address (A), control (C), and first two data characters. The scanner examines the control character to determine whether the frame is information or supervisory.

If the frame is information, the scanner stores the data. (Normally the control program has a two-byte area set up to receive the A and C characters; when these are stored, the scanner makes a level 2 interrupt to obtain a data buffer.) If the scanner does not receive four characters, the length check (ICW bit 14.7) and the EOM (ICW bit 0.5) or Abort Detect (ICW bit 0.0) bit is set and a level 2 interrupt is made.

If the frame is supervisory, on the other hand, the scanner waits for the two BCC characters and the flag that follow the control character before storing the A and C characters. If the Flag or Abort occurs before the fifth character is received in the PDF array, the scanner returns to monitoring for the flag character and does not set any error bits in the ICW. If the fifth character (not including the initial flag) is not a flag, the scanner sets the Control exception bit (ICW bit 15.0) and continues to receive data as if the frame being received were an information frame. If ICW bit 14.5 is on, the scanner adjusts the number of bytes expected to accommodate two control (C) characters.

PCF/EPCF State X'6'/'1' (Receiving Flags): In this state the scanner has received one or more consecutive flag characters. If the character assembled in the SDF is a flag, the scanner remains in this state. The first non-flag character it receives causes the scanner to change the state. Unless an abort condition is detected, the state becomes X'6'/'2' (Receive Address) the character in the SDF is transferred to the PDF and the BCC is accumulated.

PCF/EPCF State X'6'/'2' (Received Address): In this state, the scanner has received the address character and the control character is currently being received into the SDF. When the character is assembled in the SDF, the scanner changes to PCF/EPCF state X'6'/'3' (Receive Control), transfers the contents of the SDF to the PDF and accumulates the BCC. The scanner interrogates the control byte and if an information (I) frame is indicated, sets sequence bit 1 (ICW bit 13.1) and increments the cycle steal message counter (ICW bits 13.6-13.7), allowing cycle steal operation to be activated. If a supervisory (S) frame is indicated, the scanner waits for an ending flag character before allowing cycle steal operation to begin. If a flag character or an abort condition is detected, the scanner does not set sequence bit 1 or increment the message counter.

The scanner decrements the PDF pointer by one, erasing the A character, and sets the PCF/EPCF state to X'6'/'1' (if a flag character was received) or X'5'/'0' (if an abort condition was detected).

PCF/EPCF State X'6'/'3' (Received Control): The scanner enters this state from state X'6'/'2'. In this state the scanner has received the control character and the next character expected is either data or the first BCC character. (If ICW bit 14.5 is on, indicating that two control characters are expected, sequence bit 0 is set upon entering this state and the second control character is received before the PCF/EPCF changes to a new state.) After the character is assembled in the SDF, the scanner changes to state X'6'/'4' (receive data/BCC) with sequence bit 0 on unless a flag character or an abort condition is detected. The scanner transfers the contents of the SDF to the PDF and accumulates the BCC characters.

Upon detecting a flag character, the scanner sets PCF/EPCF state X'6'/'1'. If sequence bit 1 is off (indicating a supervisory frame), the PDF array pointer is decremented to erase the 'AC' characters from the PDF array. If sequence bit 1 is on, the scanner sets end-of-message and length check indicators (ICW bits 0.5 and 14.7) into a control byte in the PDF array for a level 2 EOM interrupt request.

Upon detecting an abort condition, the scanner sets PCF/EPCF state X'7'/'3' (if sequence bit 1 is on) or X'5'/'0' (if sequence bit 1 is off) and adjusts the PDF array pointer to erase the 'AC' characters.

PCF/EPCF State X'6'/'4' (Received Data 1 and 2): The scanner enters this state from state X'6'/'3'. In this state, when Sequence bit 0 is on, the scanner has received the first data or BCC character and expects as the next character the second data or BCC character. Upon receiving that character, sequence bit 0 is reset, the received character is written in the PDF array, and BCC is accumulated. Following this, the next character expected is a flag (for a supervisory frame) or data (for an information frame).

Receipt of a flag character if ICW bit 13.1 is off causes the PDF pointer to be decremented by two (this erases the BCC characters from the PDF array) and sets sequence bit 2 (ICW bit 13.3). This bit causes checking of the BCC accumulation at the next bit service time, writes an EOM control byte with the BCC result into the PDF array, increments the message counter, sets sequence bit 1, and changes the PCF/EPCF state to X'7'/'5'.

Receipt of a data character causes the scanner to write the character into the PDF array, accumulate BCC, and change to state X'7'/'4'.

Upon detecting an abort condition, the scanner enters PCF/EPCF state X'7'/'3' if sequence bit 1 is on. If sequence bit 1 is off, the scanner enters state X'5'/'0' and decrements the PDF pointer to erase the characters received, beginning with the 'A' character.

PCF State X'7' (Received Data): In this state, the scanner is receiving information (I) frames. Data is stored under cycle steal control. If the cycle steal byte count reaches zero or the scanner detects a flag character in the received data, the scanner generates a level 2 interrupt. The scanner must receive an ending flag or detect a line idle condition to leave this PCF state.

PCF/EPCF State X'7'/'3' (Received Abort): In this state, the scanner has received an Abort character between the starting and ending flags of a frame. The scanner remains in this state until it detects either a flag character or a line idle condition. If the scanner detects a flag character, the PCF/EPCF state changes to X'7'/'5' (received ending flag); if it detects an idle condition, the PCF/EPCF state changes to X'5'/'0' (monitor flag). In either case the scanner also sets end-of-message (ICW bit 0.5) and makes a level 2 interrupt. The abort bit (ICW bit 0.0) is also set and in the case of an idle condition—ICW bit 14.1 is set.

PCF/EPCF State X'7'/'4' (Received Data): In this state, the scanner is receiving message data (other than flag or abort characters). The data is transferred from the SDF to the PDF array and the BCC is accumulated. The PCF/EPCF state does not change while consecutive data characters are being received. If the scanner detects a flag character, the state changes to X'7'/'5' (received ending flags) or X'6'/'1' (received flag). In either case the scanner sets the EOM bit (ICW bit 0.5) and makes a level 2 interrupt request. If the scanner receives an abort character, the PCF/EPCF state changes to X'7'/'3' (received abort).

PCF/EPCF State X'7'/'5' (Receive Ending Flag): In this state the scanner has received an ending flag character. When the character is assembled in the SDF, the scanner changes state to X'6'/'1' (received flag) if a flag has been received or to X'7'/'7' if an abort character has been received. If the received character is neither a flag nor an abort character, the state changes to X'6'/'2' (received address); in this case the contents of the SDF are transferred to the PDF and the BCC is accumulated.

PCF/EPCF State X'7'/'7' (Receive Idle): This state is entered by the scanner either when the scanner detects an abort character following a good message or when the control program places the scanner in this state. The program uses this state to monitor received data for flag or idle characters. Upon detecting a flag, the state changes to X'6'/'1' (received flag). Upon detecting an idle character (when ICW bit 15.3 is on), the scanner changes state to X'5'/'0' (monitor flag) and requests a level 2 interrupt.

PCF/EPCF State X'8'/'0' (Transmit Initial): This state is set by the control program to initiate text transmission. The program must initialize the following ICW fields:

- Transmit control (ICW byte 15)
- LCD (ICW byte 2)
- PCF/EPCF (ICW bytes 2 and 16)
- The low order cycle steal address (ICW byte 9)
- The cycle steal control (ICW byte 6) and cycle steal byte count (ICW byte 7). The cycle steal valid bit (ICW bit 6.5) must be set in order for the scanner to initiate a text transmission.

This state may also be used in transmitting a supervisory frame by writing the 'AC' characters into the PDF array with an Output X'4D' instruction; the cycle steal address (ICW byte 9) and cycle steal control (byte 6) need not be set.

PCF State X'9' (Transmit Data): This PCF state is used to transmit message data and control characters, the specific kinds of characters being specified by the EPCF states. The scanner enters this state from PCF state X'8'/'0' when the 'clear to send' line of the modem becomes active.

PCF/EPCF State X'9'/'0' (Transmit Pad): In this state the scanner serializes the leading Pad character from the serial data field (SDF) to the line adapter. The address and control bytes are in the PDF array awaiting transmission. Any data to be transmitted is also in the PDF array. At the time the next character is transferred the scanner places a clock sync or flag character in the SDF and changes the PCF/EPCF state.

PCF/EPCF State X'9'/'1' (Transmit Clock Sync): In this state the scanner serializes the clock sync characters from the SDF to the line adapter. After the sync characters are transmitted, the scanner places a flag character in the SDF and changes the PCF/EPCF state.

PCF/EPCF State X'9'/'2' (Transmit Flags): In this state the scanner serializes consecutive flag characters until a data character is available in the PDF for transmission. The scanner then places that character in the SDF, resets the BCC accumulation, accumulates a new BCC for that character, and changes the PCF/EPCF state. Zero bit insertion is inhibited in this state.

PCF/EPCF State X'9'/'3' (Transmit Abort): This state is entered if the scanner is to transmit an abort sequence. After transmitting the abort sequence the scanner places a flag character in the SDF, aborts transmission of the current message, sets appropriate error flags in the ICW, changes the PCF/EPCF state to X'9'/'2' to send consecutive flag characters, and makes a level 2 interrupt request.

The scanner transmits an Abort sequence if the ICW control bits indicate that more data is to be transmitted but the PDF array is empty. This condition also sets the underrun bit (ICW bit 0.2). Zero bit insertion is inhibited in this state.

PCF/EPCF State X'9'/'4' (Transmit Data): In this state the scanner transmits message text. The scanner transfers each character from the PDF array to the SDF, from which it is serialized to the line adapter. When the cycle steal byte count reaches zero and the data chain flag (ICW bit 6.6) is on, the scanner makes a level 2 interrupt request to obtain the next buffer. If the data chain flag is not on (indicating that no more data blocks are to be sent), the scanner continues to transfer characters from the PDF array to the SDF until the PDF array is empty. At the next character transfer time the scanner places the first BCC character in the SDF and changes the PCF/EPCF state. Zero bit insertion is active in this state.

PCF/EPCF State X'9'/'5' (Transmit Ending Flag): This state is entered after the BCC characters are serialized, the ending flag has been placed in the SDF, and the need for a line turnaround is indicated by ICW bit 15.7. When leaving this state, the scanner places a two- or eight-bit pad of 1 bits in the SDF, as indicated by ICW bit 15.6. Zero bit insertion is inhibited in this state.

PCF/EPCF State X'9'/'6' (Transmit BCC): In this state the scanner serializes the two BCC characters from the SDF to the line adapter. After this is completed, an ending flag character is placed in the SDF and the PCF/EPCF state is changed. Zero bit insertion is active in this state.

PCF/EPCF State X'9'/'7' (Transmit Idle): In this state the scanner transmits continuous line idle characters (all one bits) if line turnaround is not specified by ICW bit 15.7 (line turnaround after transmission). If ICW bit 15.7 does specify line turnaround, the scanner transmits two or eight consecutive one bits before changing its state to X'5'/'0'. The two bits serialized from the SDF to the line set ensure that the modem has transmitted an ending flag bit before a line turnaround occurs. Zero bit insertion is inhibited in this state.

PCF/EPCF State X'9'/'C' (Transmit Diagnostic Mode): In this state the scanner transmits an unmodified bit stream corresponding to the data obtained from storage. When all the data is transmitted, the scanner enters PCF/EPCF state X'9'/'7' before performing a line turnaround. Zero bit insertion is inhibited in this state.

PCF State X'A' (Transmit Initial with New Sync): This state is identical to PCF state X'8' (transmit initial) except that the new sync interface lead to the modem will be controlled according to the setting of ICW bit 16.0. (The scanner sets and resets this bit.) This state must be used only with four-wire, duplex multipoint leased-line modems where the associated interface is the master station. All of the EPCF states described for PCF state X'8' are valid for PCF state X'A'.

PCF State X'B' (Transmit Data with New Sync): This state is identical to PCF state X'9' (transmit data) except that the new sync interface lead to the modem is activated when the address (A) character is transmitted and deactivated when the second BCC character is transmitted. ICW bit 16.0 (set and reset by the scanner) controls the activation of the new sync lead. This state must be used only with four-wire, duplex, multipoint leased-line modems where the associated interface is the master station. All of the EPCF states described for PCF state X'9' are valid for PCF state X'B'.

PCF State X'C' (Reserved)

PCF State X'D' (Reserved)

PCF State X'E' (Transmit Continuous): The control program can use this state to transmit the same character continuously. Before setting this state, the program must set the SDF via an Output X'46' instruction and the PDF via an Output X'44' instruction (bit 0.4 must be on to allow writing in the PDF). The scanner activates the 'request-to-send (RTS) lead to the modem. When the modem signals 'clear to send' (CTS), the scanner sets sequence bit 0 and transfers the SDF content serially by bit to the line set. At each character transfer time, the character in the PDF is transferred to the SDF to be serialized. The PDF pointer is not incremented. The control program must change this state to end the continuous transmission.

PCF State X'F' (Disable): The control program sets this state to cause the Type 3 Scanner to turn off the 'data terminal ready' lead to the modem. A disable command resets all control information that was provided by the last Set Mode instruction (PCF state X'1'). The scanner then causes the interface to be placed in an interrupt pending state when the 'data set ready' lead and the 'receive line signal detect' lead are deactivated. For Auto Call applications, other conditions on the automatic calling unit must be satisfied before another dial operation can be attempted following the Disable. The scanner sets PCF state X'0' (no-op) before requesting the interrupt. Because all control information in the line set is reset, the control program must set the proper control information in the line set via a Set Mode instruction (PCF state X'1') issued after the Disable command.

ICW Status Byte

The Type 3 or Type 3HS Scanner uses the status indicators in byte 15 of the ICW to determine the appropriate control sequences to send during a transmit operation. During a receive operation, the scanner uses these indicators to inform the control program what control characters were received.

ICW Status Indicators for BSC

The format of the status byte for BSC transmit operations in network control mode is:

Bit:	0 1 2	3 4 5 6	7
	Initial Control Sequence	Final Control Sequence	Leading Graphics Flag

For BSC transmit operations in emulation mode, the initial and final control sequences appear in the data stream received from the host processor except for transparent text ending sequences. For these sequences the program sets the final status bits (ICW bits 15.3-15.6) in the same manner as for BSC operations in network control mode.

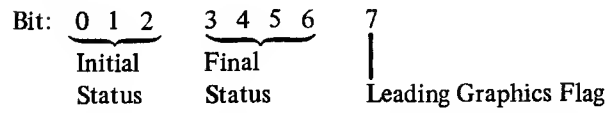
Initial Control Sequence: These bits determine the control characters to be sent at the beginning of message transmission If no initial sequence is to be sent, the final control sequence bits determine the response or control characters to be transmitted.

Bit: *0 1 2*	*Initial Status (Control Sequence)*
0 0 0	(none)
0 0 1	STX
0 1 0	DLE STX
0 1 1	SOH
1 0 0	Special
1 0 1	(reserved)
1 1 0	(reserved)
1 1 1	(reserved)

Final Control Sequence: These bits determine the control characters to be sent at the end of a transmission. The meanings of these bits depend on the initial control sequence bits as described above.

Bit:	0	1	2	3	4	5	6	*Final Status (Control Sequence)*
0 0 0	0	0	1	1				Transmit ENQ, then turn line around
	0	1	1	0				Transmit ACK-0, then turn line around
	0	1	1	1				Transmit NAK, then turn line around
	1	1	0	1				Transmit RVI, then turn line around
	1	1	1	0				Transmit ACK-1, then turn line around
	1	1	1	1				Transmit WACK, then turn line around
0 0 1	0	0	1	1				Transmit STX ENQ (TTD), then turn line around; set byte count to 0
	1	0	0	1				Transmit STX data ETX, then turn line around; do not skip byte for ITB in data
	1	0	1	0				Transmit STX data ETB, then turn line around; do not skip byte for ITB in data
	1	1	0	1				Transmit STX data ETX, then turn line around; skip byte if ITB occurs in data
	1	1	1	0				Transmit STX data ETB, then turn line around; skip byte if ITB occurs in data
0 1 0	0	0	1	1				Transmit DLE STX data DLE ENQ, then turn line around
	0	1	0	0				Transmit DLE STX data DLE ITB (no line turnaround)
	1	0	0	1				Transmit DLE STX data DLE ETX, then turn line around
	1	0	1	0				Transmit DLE STX data DLE ETB, then turn line around
	1	1	0	1				Transmit data DLE ETX, then turn line around (ITB sent previously via 010 0100 status byte)
	1	1	1	0				Transmit data DLE ETB, then turn line around (ITB sent previously via 010 0100 status byte)
0 1 1	0	0	1	1				Transmit SOH data ENQ, then turn line around
	1	0	0	1				Transmit SOH data ETX, then turn line around; do not skip byte for ITB in data
	1	0	1	0				Transmit SOH data ETB, then turn line around; do not skip byte for ITB in data
	1	1	0	1				Transmit SOH data ETX, then turn line around; skip byte if ITB occurs in data (Note: If DLE STX appears in data, scanner ends data with DLE ETX.)
	1	1	1	0				Transmit SOH data ETB, then turn line around; skip byte if ITB occurs in data (Note: If DLE STX appears in data, scanner ends data with DLE ETB.)
1 0 0	1	1	0	0				Transmit EOT, then turn line around
	1	1	1	0				Transmit DLE EOT, then turn line around

The format of the status byte for BSC receive operations is:



Initial Status: These bits are set in accordance with the first control character or sequence received from the line interface:

Bit: *0 1 2*	*Initial Status*
0 0 0	Control mode status (no text was received)
0 0 1	Text Mode status (first control character is STX)
0 1 0	Transparent text mode status (DLE STX first control characters)
0 1 1	Heading status (first control character is SOH)
1 0 0	Special status (DLE EOT (Disconnect) first control characters)
1 0 1	(reserved)
1 1 0	(reserved)
1 1 1	(reserved)

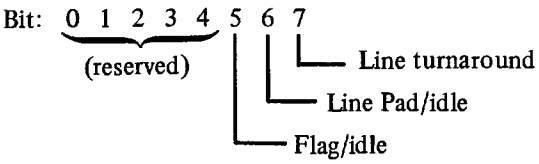
Final Status: These bits are set in accordance with the ending control character or sequence received from the line interface:

Bit *3 4 5 6*	*Final Status/Character received*
0 0 0 0	(Timeout occurred)
0 0 0 1	ITB received
0 0 1 0	(reserved)
0 0 1 1	ENQ received
0 1 0 0	EOT received
0 1 0 1	DLE *x* received (*x* = second character of any valid DLE sequence)
0 1 1 0	Wrong ACK received
0 1 1 1	NAK received
1 0 0 0	(reserved)
1 0 0 1	ETX received
1 0 1 0	ETB received
1 0 1 1	(reserved)
1 1 0 0	(reserved)
1 1 0 1	RVI received
1 1 1 0	Positive ACK (ACK-0 or ACK-1) received
1 1 1 1	WACK received

Leading Graphics bit (bit 7): Bit 7 is set on a BSC receive operation if the first character of the received message is not a control character.

ICW Status Indicators for SDLC

The format of the status byte for SDLC transmit operation is:

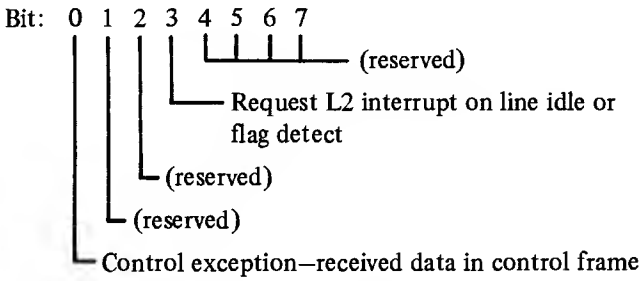


Bit 5: When set (1), this bit causes the scanner to transmit continuous flag characters at the end of the frame if bit 7 is not set to cause the line to turn around. When reset (0), this bit causes the scanner to assume a line idle state after sending the ending flag after a frame.

Bit 6: When set (1), this bit causes the scanner to send an all-1's character (8 consecutive 1's) before turning the line around if bit 7 is set to cause line turnaround.

Bit 7: When set (1) this bit causes the scanner to turn the line around (that is, change from a transmit to a receive state) after it transmits the ending flag character.

The format of the status byte for SDLC receive operations is:



Bit 0: The scanner sets this bit when a control (C) frame was indicated by the C byte but the flag character was not received three bytes afterward.

Bits 1 and 2: (reserved)

Bit 3: The control program sets this bit to request that the scanner make a level 2 interrupt request if the receive line assumes an idle state or a flag character is detected.

Interface Mode Set–SDF Values

The interface hardware latches are set and reset according to the value in the SDF field during PCF state X'1'. The SDF values for a set mode instruction are as follows:

SDF bit 0: This bit is set by bit 0.0 of an Output X'46' instruction. This bit is set to 1 to place the addressed line in NRZI mode. ICW bit 5.4 is set or reset according to the state of this bit when the set mode instruction is executed. The control program should not set this bit if the ICW is associated with a BSC line.

SDF bit 1: This bit is set by bit 0.1 of an Output X'46' instruction. This bit is set to 1 to place the addressed line in diagnostic mode 0. ICW bit 5.5 is set or reset according to the state of this bit when the set mode instruction is executed.

SDF bit 2: This bit is set by bit 0.2 of an Output X'46' instruction. This bit is set to 1 to place the addressed line in diagnostic mode 1. ICW bit 5.6 is set or reset according to the state of this bit when the set mode instruction is executed.

SDF bit 3: This bit is set to 1 to place the addressed interface in the line adapter wrap line diagnostic mode.

SDF bit 4: Data Terminal Ready—This bit controls the data terminal ready lead to the modem; this lead must be set to enable the line interfaces provided by all line sets except those used for Auto Call operation (line set 1E). ICW bit 16.1 (data terminal ready) is also set when the set mode instruction is executed.

SDF bit 5: Synchronous Bit Clock—This bit determines whether synchronous or start-stop clocking is used for the addressed interface when business machine clocking is specified. If SDF bit 6 is 1 (external clocking), this bit is ignored.

SDF bit 6: External Clocking—This bit determines whether business machine or modem clocking is used for the addressed interface; 1 indicates modem clocking and 0 indicates business machine clocking. ICW bit 5.7 (external modem clocking) is also set when the set mode instruction is executed.

SDF bit 7: Data Rate Selector—This bit selects a high speed or low speed data rate for the attached modem. A 1 = high data rate, and 0 = low data rate. If modem clocking is specified, this bit selects which of the two clock speeds in the modem is to provide the clock pulses. The low rate usually equals one-half of the high rate. In this case the business machine clock selected by the oscillator select bits must not exceed one-half the clock speed selected in the modem.

A feedback check occurs if this bit is on when the program executes a set mode to a line interface provided by line sets that allow only one data rate.

SDF bits 8 and 9: OSC Select Bits 1 and 2—The state of these two bits selects the business machine clock to be used by the addressed line interface. At least one business machine clock must be installed in each Type 3 or Type 3HS Scanner. See the following section, *Business Machine Clocks.*

Programming Note

The oscillator select bits can be changed without causing a switched network connection to be broken if SDF Bit 4 (Data Terminal Ready) is set when the set mode is executed.

Business Machine Clocks

Each Type 3 or Type 3HS Scanner must have at least one business machine clock card installed and the Type 3 Scanner may have two. The required clock has oscillator bit rates of 150, 600, and 1200 bps (designated by oscillator select bit values 0, 1, and 2). (See Figure 8-6.) The optional clock for a Type 3 Scanner may have a bit rate of 2000 or 2400 bps (designated by oscillator select value 3).

Modems attached to 3705s must provide clock pulses for line speeds above 2400 bps. Refer to the *Introduction to the 3704 and 3705* manual for a description of the individual LIB and line set types.

The installed business machine clock used for a given line is selected under program control by executing a set mode (PCF state X'1') with SDF bits 8 and 9 set to indicate the desired bit rate. Figure 8-6 shows the proper setting of the oscillator selcct bits to assign an installed oscillator to a given interface.

SDF 8	*Bits* 9	*Selected Business Machine Clock*	
0	0	150 bps	(OSC0)
0	1	600 bps	(OSC1)
1	0	1200 bps	(OSC2)
1	1	2000 or 2400 bps	(OSC3)

Figure 8-6. Type 3 and Type 3HS Communication Scanner Business Machine Clock Selection

No business machine clock is selected if the oscillator select bits are set to select an uninstalled oscillator (for example, bits 8 and 9 set to 11 when only the required clock is installed).

Every interface must have a business machine clock assigned whether it is specified to be business machine- or modem-clocked. For autocall interfaces and for line interfaces that are to use modem clocking, the assigned business machine clock is used to ensure that the interface is periodically accessed. The lowest speed oscillator must always be used for an autocall interface.

The oscillator select bits are set to 0 by a reset to the scanner. Therefore, the lowest speed oscillator is initially selected, and unless a set mode is executed to select another oscillator for a given interface, the lowest speed oscillator is used.

After a power-on-reset occurs, there is a warm-up period associated with the different clocks. This period is less than one second for each of the clocks available for the Type 3 or Type 3HS Scanner. During this warm-up period, a business machine clock cannot provide service requests.

Programming Notes

1. The oscillator select bits for a line interface can be changed without causing a switched network connection to be broken, if 'data terminal ready' is active when the Set Mode instruction is executed.
2. The business machine clock selected for a modem-clocked line interface must be less than one-half the rate of the modem clock.

I/O Programming Considerations

As a general rule, input/output instructions should be issued only when the status of the attachment buffer address register (ABAR) and the particular scanner ICW input register is known. An understanding of how those registers are set or loaded is needed for correct execution.

The ABAR is set under the following conditions:

1. The interface address in the highest priority program level 2 interrupt register located in the attachment base is loaded into ABAR just before program level 2 becomes the current program level.

   Therefore, if an Input X'40' is executed as the first instruction in program level 2, the register specified by the R operand contains the interface address for that interrupt.
2. When the program executes an Output X'40', the interface address in the register specified by the R operand is placed in ABAR.

The ICW input register of the selected scanner is loaded with the contents of the ICW associated with the interface address in the ABAR when:

1. The ABAR is loaded after a program level 2 interrupt occurs.
2. The Output X'40' instruction is executed in program level 3 or 4. This enables the level 3 or 4 routines to access any portion of the selected ICW associated with the interface address in the ABAR.

Figure 8-7 summarizes which program levels can set the ABAR in the attachment base and set the ICW input register in the selected scanner.

Program Level	*ABAR*	*ICW Input Register*
1	Output X'40'	Cannot be set
2	L2 Interrupts	L2 Interrupt
3 or 4	Output X'40'	Output X'40'

Figure 8-7. Setting ABAR and ICW Input Register

The following considerations are recommended for executing input/output instructions in the different program levels.

Program Level 1 (Error Routines)

Input X'40' can be executed to obtain the interface address from the attachment buffer address register (ABAR) in the Type 2 Attachment Base. This old interface address should be saved if a different address is required to select the scanner that has its L1 interrupt request set.

Output X'40' can be executed to select the appropriate scanner if needed. Only the selected Scanner can decode the input/output instructions. However, the scanner input register is not changed if an Output X'40' is executed at program level 1 or 2.

After the scanner is selected, other input and output instructions may be executed as needed. Output instructions may be executed in any order, but all output instructions (Outputs X'41' through X'4F') that set a portion of the ICW *must* be separated by at least one cycle. This is required because the output register in the scanner buffers the data from the general register and requires time to execute the instruction.

Before exiting from program level 1, the program may execute an Output X'40' to place the old interface address back in ABAR if it had been saved. However, one instruction cycle must separate it from any Output X'41'–X'4F'. The selected scanner ICW input register is not changed as a result of Output X'40'.

At least one instruction cycle must separate the last output instruction and an Exit instruction.

Program Level 2 (Character Service)

Input X'40' may be executed immediately to obtain the interface address. When Input X'40' is issued while in program level 2, the 'priority register occupied' latch associated with the interface address in ABAR is reset. This indicates that the character service request is being serviced and that the program level 2 interrupt priority register from which the ABAR was loaded is now available for another level 2 interrupt of the same priority. If all the 'priority register occupied' latches are reset, the Type 2 Scanner L2 interrupt request is reset. Inputs X'41'–X'4F' may be executed whenever necessary to obtain a portion of the ICW from the Type 3 or Type 3HS Scanner ICW input register. Outputs X'41'–X'4F' may be executed whenever necessary to set a portion of the ICW.

Output instructions may be executed in any order, but all subsequent Output X'41'–X'4F' instructions must be separated by at least one cycle.

The control program should not issue an Output X'45' instruction to change the LCD and PCF fields if the cycle steal valid bit (ICW bit 6.5) is on, because the results will be unpredictable. The program must issue an Output X'48' instruction to set the cycle steal valid bit before issuing an Output X'44' instruction that resets the SCF field. The Output X'44' instruction should be the last Output instruction issued to the scanner before the Exit instruction is executed.

At least one instruction cycle must separate the last output instruction and an Exit instruction.

Programming Note
Subsequent Input X'40' instructions within the same character service interrupt do not reset the 'priority register occupied' latches.

Program Levels 3 and 4 (Lower Level Routines)
Output X'7E' may be executed with a 1 in byte 1, bit 2 of the register specified by the R operand. This will 'mask off' program level 2 interrupts that could change the contents of the attachment buffer address register (ABAR) in the Type 2 Attachment Base by a character service L2 interrupt.

Output X'40' may be executed to load ABAR with the interface address of a line to be acted upon. The contents of the ICW associated with this interface address are placed in that scanner ICW input register.

After the scanner is selected, (1) Output X'41'–X'4F' may be executed (to alter the associated portion of the ICW), followed by some other instruction, or (2) some other instruction must be executed, followed by Input X'41'–X'4F' (to obtain the associated portion of the ICW that was loaded by Output X'40' into the ICW input register).

If Output X'41'–X'4F' was executed as in (1) above, the ICW content was altered, but the ICW input register still contains the contents of the ICW as it was before the alteration.

Output instructions may be executed in any order, but all subsequent Output X'41'–X'4F' instructions must be separated by at least one cycle.

The control program should not issue an Output X'45' instruction to change the LCD and PCF fields if the cycle steal valid bit (ICW bit 6.5) is on, because the results will be unpredictable. The program must issue an Output X'48' instruction to set the cycle steal valid bit before issuing an Output X'44' instruction that resets the SCF field. The Output X'44' instruction should be the last Output instruction issued to the scanner before the Exit instruction is executed.

It is recommended that all lines in the addressed Type 3 Scanner be disabled before executing an Output X'42' to change the upper scan limit.

Output X'7F' may be executed with a 1 in byte 1, bit 2 of the register specified by the R operand. This unmasks the program level 2 interrupts. This output instruction must be separated by at least one instruction cycle from the last Output X'43', X'44', X'45', X'46', X'47' X'41'– 'X'4F' instruction.

Autocall Interface Operation (Type 3 Scanner Only)

The Type 3 Communication Scanner supports operation of an autocall interface when the interface is attached to Line Set 1E and the line control definer (LCD) field of the associated ICW is set to X'3'. The primary control field (PCF) of the ICW is used to control the interface operation. Whenever an autocall interface that has a service request is scanned, the scanner interprets the PCF to determine what communication should occur between the scanner and the interface hardware. The scanner also determines, from the PCF, whether the interface should be placed in a level 2 interrupt pending state. The lowest speed business machine clock installed in each scanner (150 bps) is used to generate service requests for all autocall interfaces installed in that scanner. Service requests are generated at the same rate as the clock speed.

Interface Control Word for Autocall Operation
The following bits/fields are used for autocall operation.

ICW bit 0.1	Service Request
ICW bits 1.4–1.7	PDF bits 4-7
ICW bits 2.0–2.3	LCD
ICW bits 2.4–2.7	PCF
ICW bits 3.0–3.7	SDF bits 0-7
ICW bit 4.6	Display Request
ICW bit 5.1	L2 Interrupt Pending
ICW bits 5.2–5.3	Service Priority

Programming Note
A reset to the scanner sets the PCF state of each ICW to X'0' and sets and resets the following bits:

Sets:	Resets:
0.4	2.4–2.7
4.5	4.2–4.4
12.0–12.7	4.6–4.7
	5.0–5.1
	5.5–5.7
	6.5

However, when power is turned on in the controller, all other ICW bits are unpredictable. Therefore the program must ensure that during initialization ICW bits 0.0–0.3, 0.5, 14.1, 14.3, 14.4, 14.6, and 14.7 are reset.

PCF States for Autocall Operation
Five primary control field (PCF) states are available for autocall operation. Setting the PCF to an undefined value may result in improper operation. Each time the control program changes the PCF state, it should also set the LCD to X'3'. The following PCF states are valid for autocall interfaces.

PCF State X'0': Idle—This state resets the 'call request' and 'digit present' indications in the autocall interface each time the interface is scanned and a bit service is present. If the control program sets this state, no interrupt requests result from that interface until the program changes the PCF to one of the other valid states. If the scanner sets this state as a result of ending a PCF state X'F' (disable), the interface is placed in a level 2 interrupt pending state.

PCF State X'4': Monitor Call ACR, COS, PND— When the Type 3 Scanner fetches an ICW for an autocall interface in this PCF state, the autocall interface is monitored for the active state of the following leads:

ACR—Abandon Call and Retry
COS—Call Originate Status
PND—Present Next Digit

When any of these leads are found to be active, the appropriate SDF bit is set, and the interface is placed in a level 2 interrupt request pending state.

PCF State X'5': Monitor Call ACR, COS—This state is the same as PCF state X'4' except the active condition of 'present next digit' (PND) does not generate a level 2 interrupt request.

This PCF state can only be set by the control program.

Programming Note
The control program must ensure that the interrupt remember bit (SDF bit 0) is reset when it places the interface in this state. Otherwise no interrupt request can be generated because of active control leads.

PCF State X'8': Digit Valid—This state is set by the control routine after it has placed the next dial digit into the PDF. This digit is continuously presented to the ACU interface until PND falls; the scanner sets the PCF to X'4', and no interrupt is requested.

PCF State X'F': Disable—This state is used to reset the dial interface at the end of the data transfer operation. After all the control leads from the Autocall unit (ACU) have been reset, the Type 3 Scanner sets the PCF to X'0' and places the interface in a level 2 interrupt request pending state.

Serial Data Field for Autocall Operation
The control program can monitor the autocall interface by interrogating the serial data field (SDF) in the interface control word. The serial data field is updated with the current status of the autocall interface each time the interface is scanned and a bit service request is present. SDF bits 1-9 reflect the state of certain autocall control signals and have no effect on the interface operation. Bit 0 is the only SDF bit that affects operation. The following paragraphs describe each SDF bit and its meaning.

SDF Bit 0: Interrupt Remember (IR)—This bit is set by the scanner to indicate a level 2 interrupt pending state. In PCF state X'4' or X'5', the scanner monitors the respective autocall interface leads for an active condition. When one of the monitored leads becomes active, the scanner sets the interrupt remember bit to prevent further interrupts from that interface until the first interrupt has been serviced. This bit must be reset by the control program each time an interrupt is serviced in order to allow the next interrupt to be recognized.

Programming Note
The program should not reset the interrupt remember bit before changing the PCF state from X'4' or X'5' to some other state because an unexpected interrupt request may result.

SDF Bit 1: Power Indicator (PWI)—When this bit is 0 the automatic calling equipment is inoperative because of the lack of power.

SDF Bit 2: Call Request (CRQ)—A 1 in this position indicates a request to originate a call to the autocall interface. The scanner sets the CRQ in the autocall interface whenever (1) the interface is scanned, (2) a bit service request is present, and (3) the PCF state is X'4', X'5', or X'8'. If the condition of this bit does not agree with the state defined for the active PCF state, the LCD is set to X'F' to indicate a feedback check.

SDF Bit 3: Data Line Occupied (DLO)—A 1 in this position indicates that the autocall interface is in use. The program should not attempt to originate a call until this lead becomes inactive.

SDF Bit 4: Present Next Digit (PND)—A 1 in this position indicates that the autocall unit is ready to accept the next digit. The PND lead is used by the autocall unit to control the presentation of digits to the unit during a dialing operation.

When the 'present next digit' lead is active and the PCF state is X'4', the scanner sets the interrupt remember bit if it is not already on. If the PND lead is inactive and the PCF state is X'8', the scanner changes the PCF state to X'4'.

SDF Bit 5: Digit Present (DPR)—A 1 in this position indicates that a valid digit is present on the digit leads to the autocall unit. The scanner sets DPR via PCF state X'8' after present next digit comes on and the next dial digit has been placed into the parallel data field, bits 4-7. When the autocall unit turns PND off, the scanner changes the PCF state to X'4' and resets DPR. The scanner resets DPR when the PCF state is changed to X'0', X'4', X'5', or X F'. If the condition of this bit does not agree with the state defined for the active PCF state, the LCD field is set to X'F' to indicate a feedback check.

SDF Bit 6: Data Set Status (DSS)/Call Originate Status (COS)—A 1 in this position indicates that a connection has been established and that the modem is in data mode and can be used for data communications. In PCF state X'4', the scanner sets the interrupt remember bit when the DSS/COS lead becomes active.

SDF Bit 7: Abandon Call and Retry (ACR)—A 1 in this position indicates that a preset time interval in the autocall unit has elapsed since the last change of the 'present next digit' lead. This bit only alerts the control program to the time-out condition; it does not automatically abandon the call and retry. The control program is responsible for abandoning the call and retrying. In PCF state X'4', the scanner sets the interrupt remember bit when the ACR lead becomes active.

SDF Bits 8 and 9: These bits are not used.

PDF for Autocall Operation

For autocall operation the parallel data field is used to present the dial digits to the automatic calling unit. When the autocall interface is in PCF state X'8', the parallel data field bits 4-7 must contain a valid digit. In any PCF state other than X'8', the PDF is treated as if it contained all zeros. The valid digits that can be loaded into the PDF are from X'0' to X'9' and X'C' and X'D'. X'0' to X'9' represent the value of the dial digit and X'C' is an *end of number* bit configuration used to inform the autocall unit that the last digit of the called number has been provided. X'D' is a *separator* bit configuration used to inform the autocalling unit to wait for a second dial tone.

Note: *The external automatic calling unit (ACU) must have the appropriate features to use X'C' and X'D'.*

Input/Output Instructions

The Type 3 or Type 3HS Scanner input/output instructions enable the program to communicate between line interface bases (LIBs), program interrupt levels, interface control words (ICWs), and scanner registers. Some of the major functions of the I/0 instructions are to:

- Determine the interface address that caused a program level 2 interrupt.
- Determine the cause of a program level 1 interrupt once the scanner causing the interrupt has been identified (Input X'76' has been executed).
- Determine the status of a particular ICW.
- Determine the status of a scanner display register.
- Set the attachment buffer address register (ABAR) with the interface address required for:

a) addressing a particular ICW in program levels 3 or 4.
b) restoring an old ABAR address that had been saved while in the error routines of a program level 1 interrupt. This allows the program to resume normal operation with the same interface address in the ABAR as when the program level 1 interrupt occurred.
c) addressing a particular scanner in program level 1, 3, or 4.

- Set and reset bits in a particular ICW.
- Set scan limits in a particular scanner.
- Set control bits in a particular scanner.
- Set or read the cycle steal controls (address and byte count, ICW bytes 6-9) of a particular ICW.
- Access any of the parallel data field in the PDF array.
- Set the high speed select register in a particular scanner while setting the substitution control register (SCR) in the Type 2 Attachment Base.

Programming Note

Input/Output instructions are privileged instructions executable only at program level 1, 2, 3, or 4. Any attempt to execute these instructions improperly causes a program level 1 interrupt request by setting the 'input/output check L1' latch. Refer to *Input/Output Check* description in Chapter 5 for the conditions that cause the check to be set.

Input Instructions

Input instructions in the range X'40'—X'4F' allow the program to obtain the status of the ICW input register, display register, and error register in the scanner, and the and the interface address in the attachment base ABAR. (Appendix B defines the bits within each input instruction.)

Input instructions should be executed only when the status of the attachment buffer address register (ABAR) and the content of the ICW input register are known.

Programming Notes

1. With Extended Addressing, byte X of all input instructions and external registers is set to zero.
2. When an autocall interface is used, some of the input instructions have different bit definitions. Refer to the individual instruction descriptions for these differences.

Input X'40' (Interface Address): This instruction is used to obtain the line interface address from the ABAR in the attachment base. Conditions that set the ABAR are described in the *I/O Programming Considerations* section in this chapter.

If Input X'40' is issued during program level 2, the 'priority register occupied' latch associated with the interface address in the ABAR is reset. This indicates that the character service request is being serviced and that the program level 2 interrupt priority register from which the ABAR was loaded is now available for another level 2 interrupt of the same priority. If all the 'priority register occupied' latches are reset, the scanner L2 interrupt request is reset.

Programming Note
Subsequent Input X'40' instructions within the same character service interrupt do not reset the 'priority register occupied' latches.

Input X'41' (High Speed Select): For Type 3 Scanner operations, this instruction is used to obtain the settings of the high speed select register bits 0 through 7 for the scanner selected by the address in the ABAR.

Type 3HS Scanner Operations: This instruction is used to obtain ICW bits 17.0 and 17.1 from byte 1, bits 0 and 1 of a selected general register. (Refer to *Byte 17 (ICW Controls Extended)* earlier in this chapter.) An Output X'40' instruction must be executed before issuing an Input X'41' instruction to obtain byte 17, bits 0 and 1 of the ICW.

Input X'42' (DBAR/Check Register): This instruction is used to obtain the contents or value of the DBAR, the scan limit select bits, (See Note), the PDF array parity error bit, and the ICW parity error bits for the scanner selected by the address in the ABAR. For any parity error, PDF array error, or LIB select error, the content of the DBAR is the binary address of the ICW selected at the time the error occurred.

Note: Scan limit select bits are not significant to Type 3HS Scanner operations.

Input X'43' (Check Register 1): This instruction may be used to obtain the status of the check register of a Type 3 or Type 3HS scanner. Since it is possible for up to four scanners to be installed in the controller, the check register selected is determined by the interface address in the ABAR at time of instruction execution.

Programming Note
If any of the check register bits in the scanner are set to 1, the Type 3 or Type 3HS Scanner L1 interrupt request is set.

Input X'44' (ICW Input Register - Bytes 0-1): This instruction may be used to determine the state of the secondary control field (SCF) and the parallel data field (PDF) in the ICW that is set in the ICW input register. The interface address in the ABAR selects the proper scanner. Refer to *I/O Programming Considerations* for conditions that set the ICW input register. The SCF and PDF fields and bit definitions are described in the *Interface Control Word Format* section of this chapter.

Input X'45' (ICW Input Register - Bytes 2-3): This instruction may be used to determine the state of the LCD and PCF fields and SDF bits 0-7 in the ICW that is set in the ICW input register. The interface address in the ABAR selects the proper scanner. Refer to *I/O Programming Considerations* in this chapter for conditions that set the ICW input register. The LCD, PCF, and SDF fields and bit definitions are described in the *Interface Control Word Format* section of this chapter.

Input X'46' (Display Register): This instruction may be used to determine the state of the display register in the scanner selected by the interface address in ABAR.

The program, under control of the *display request* bit (ICW bit 4.6), can cause status information for a particular interface to be placed into the scanner display register when the interface is scanned. Input X'46' can then be used to examine this status information. The display register normally contains the status of the clear to send, ring indicator, data set ready, receive line signal detect, receive data bit buffer, diagnostic wrap mode, bit service request, and ICW diagnostic mode indicators for the line interface (or contains the Autocall unit indicators, for an Autocall interface). Alternatively, the display register contains the status of the scanner-to-line set *data out* lines (if the scanner is in diagnostic 0 mode [ICW bit 5.5 is on]) or the line set-to-scanner *data in* lines (if a feedback check has occurred for the line Interface [LCD state is X'7' or X'F']).

Input X'47' (ICW Input Register - Bytes 4-5): This instruction may be used to determine the state of SDF bits 8-9 (ICW bits 4.0-4.1) display request bit (bit 4.6) L2 interrupt pending bit (bit 5.1) and priority select bits 1-2 (bits 5.2-5.3). The ones counter (4.2-4.4, 4.7, 5.0) the last line state (4.5) the NRZI control bit (5.4) diagnostic 0-1 bits (5.5-5.6), and external modem clock (5.7) can also be examined by using this instruction. The interface address in the ABAR selects the proper scanner and associated ICW. See *I/O Programming Considerations* in this chapter for conditions that set the ICW input register. For an interpretation of these bits, see the *Interface Control Word Format* section of this chapter.

Input X'48' (ICW Input Register–Bytes 6-7): This instruction may be used to determine the state of the Cycle Steal Address byte X and byte count field, and the ETB/ETX/ENQ-in-data, cycle steal valid, data chain flag, and message chain flag bits. The interface address in the ABAR selects the proper scanner and the associated ICW. Refer to *I/O Programming Considerations* in this chapter for conditions that set the ICW input register. For an interpretation of the bytes and bits mentioned above, see *Interface Control Word Format* in this chapter.

Input X'49' (ICW Input Register–Bytes 8-9): This instruction may be used to determine the contents of the cycle steal address bytes 0 and 1. The interface address in the ABAR selects the proper scanner and the associated ICW. Refer to *I/O Programming Considerations* in this chapter for conditions that set the ICW input register.

Input X'4A' (ICW Input Register–Bytes 10-11): This instruction may be used to determine the state of the block check character bytes 1 and 2 in the ICW. The interface address in the ABAR selects the proper scanner and the associated ICW. Refer to *I/O Programming Considerations* in this chapter for conditions that set the ICW input register.

Input X'4B' (ICW Input Register–Byte 16): This instruction may be used to determine the state of the new sync, data terminal ready, and OLTT diagnostic bits and the extended PCF of the ICW. The interface address in the ABAR selects the proper scanner and the associated ICW. Refer to *I/O Programming Considerations* in this chapter for conditions that set the ICW input register. For an interpretation of the bits and extended PCF mentioned above, see *Interface Control Word Format* in this chapter.

Input X'4C' (ICW Input Register–Byte 1 and control bits): This instruction may be used to determine the contents of the PDF in the PDF array that is addressed by the PDF pointer, including the control bits. The interface address in the ABAR selects the proper scanner and the associated ICW. For an interpretation of the control bits of the PDF, see *PDF Array Format* in this chapter.

Input X'4E' (ICW Input Register–Bytes 12-13): This instruction may be used to determine the contents of the cycle steal-PDF array and PDF array pointers, (also see *Input X'41'* if the Type 3HS Scanner is installed), the sequence and cycle steal message count fields, and the state of the request-to-send turnaround control bit. The interface address in the ABAR selects the proper scanner and the associated ICW. Refer to *I/O Programming Considerations* in this chapter for conditions that set the ICW input register. For an interpretation of the fields and bits mentioned above, see *Interface Control Word Format* in this chapter.

Input X'4F' (ICW Input Register–Bytes 14-15): This instruction may be used to determine the state of the status fields and of the following bits: receive line signal detect, format exception/idle detect, BSC flush, data check, bad pad/flag off boundary, ACK expected, leading DLE error, and length check, and leading graphics bits of the ICW. The interface address in the ABAR selects the proper scanner and the associated ICW. Refer to *I/O Programming Considerations* in this chapter for conditions that set the ICW input register. For an interpretation of the fields and bits mentioned above, see *Interface Control Word Format* in this chapter.

Output Instructions

Output instructions in the range X'40'-X'4F' allow the program to set the status of the ICW and to set the upper scan limit and certain other controls in the scanner. The interface address in the ABAR and the substitution control register in the Type 2 Attachment Base may also be set. (Appendix B defines the bits within each output instruction.)

Programming Note

With Extended Addressing, byte X of all output instructions and external registers has no significance and can be ignored.

Output X'40' (Interface Address): This instruction may be used to set an interface address in the attachment buffer address register (ABAR) of the Type 3 Attachment Base. When this instruction is executed, byte 0, bit 6 through byte 1, bit 6 in the register specified by the R operand are placed in the ABAR.

The interface address placed in ABAR selects the scanner and the ICW associated with that address. Each CCU clock time, the 16 bytes of the ICW are placed in the ICW work register. If Output X'40' is executed in program level 3 or 4 the contents of the ICW work register are placed in the ICW input register where it is available for Inputs X'41'–X'4F'.

Output X'41' (Scan Substitution Control/High Speed Select): This instruction is used to set the substitution control register in the Type 2 Attachment Base and the high speed select registers in the selected Type 3 Scanner. See *Address Substitution* and *High Speed Select Option* in this chapter for the description and coding of the address substitution and high speed select mask bits. The substitution control bits (Byte 1, bits 2-5) must be set to 0 for Type 3HS Scanner operations.

Programming Note

Use of address substitution for a 3705 having one or more Type 3 Scanners installed is not recommended, because each substitution control register (SCR) bit used causes one high speed line position on each Type 3 Scanner to be unavailable for use. The high speed select option should be used instead because the high speed select mask affects only one scanner, not all installed scanners. This independence allows more flexibility in selecting addresses to receive the increased scanning.

Output X'42' (Upper Scan Limit Control): This instruction must be used to set the upper scan limit in the selected Type 3 Scanner. At least one Output X'42' must be executed for each Type 3 Scanner available. The scanner selected is determined by the interface address in the attachment buffer address register (ABAR) of the attachment base at the time of execution. This instruction also sets the diagnostic buffer address register (DBAR). Because upper scan limit control is not used for Type 3HS operations, byte 1, bits 6 and 7 should be set to 0.

Output X'43' (Control): This instruction may be executed to set or reset various control functions in a Type 3 or Type 3HS Scanner. The scanner is selected by the interface address in the attachment buffer address register (ABAR) of the attachment base.

Output X'44' (ICW Bytes 0 and 1): This instruction may be used to reset secondary control field (SCF) bits 0-3 and 5, to set or reset SCF bits 6-7, and to set SCF bit 4. It is also used to set or reset the parallel data field (PDF) if bit 0.4 is on in the register specified by the Output instruction or if the LCD state is for an Autocall interface. This instruction does not change the PDF array address specified by the PDF pointer (ICW bits 17.1 and 12.4-12.7). For a detailed description of these bits, see the *Interface Control Word Format* section of this chapter. The interface address in the attachment buffer address register (ABAR), located in the Type 2 Attachment Base, selects the scanner and the ICW associated with this address. Refer to the secondary control field of the ICW for an interpretation of the SCF bits (ICW bits 0.0-0.7). See *Interface Control Word Format* for the PDF format as it relates to various line control definer states.

Output X'45' (ICW Bytes 2 and 16): This instruction may be used to set the bits of the line control definer (LCD) and the primary control field (PCF) of the ICW. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. This instruction is also used to set the extended PCF and other control bits in ICW byte 16.

For a detailed interpretation of these bits, see the *Interface Control Word Format* section of this chapter.

Output X'46' (ICW Byte 3 and Bits 4.0-4.1): This instruction is used to set the bits (0-9) of the serial data field (SDF) and ICW bits 5.4-5.7 and 16.1 from bits in the SDF when a Set Mode PCF is executed. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a detailed interpretation of the SDF bits, see the *Interface Control Word Format* section of this chapter.

Output X'47' (ICW Bits 4.2-4.5, 4.7, 5.0-5.3): This instruction is used to set the state of the ones counter (bits 4.2-4.4, 4.7, 5.0), last line state/timeout control (bit 4.5), display request (4.6), and priority select bits 1 and 2 (5.2-5.3). The interface address in the ABAR at execution time selects the proper scanner and its associated ICW. For a detailed interpretation of these bits, see the *Interface Control Word Format* section of this chapter.

Output X'48' (ICW Bytes 6-7): This instruction may be used to set the bits of the cycle steal address byte X and the byte count, and the ETB/ETX/ENQ-in-data, cycle steal valid, data chain flag, and message chain flag bits. The interface address in the ABAR selects the proper scanner and the associated ICW. For an interpretation of the bytes and bits mentioned above, see *Interface Control Word Format* in this chapter.

Output X'49' (ICW Bytes 8-9): This instruction may be used to change the contents of cycle steal address bytes 0 and 1. The interface address in the ABAR selects the proper scanner and the associated ICW. For an interpretation of the bytes mentioned above, see *Interface Control Word Format* in this chapter.

Output X'4A' (ICW Bytes 10-11): This instruction may be used to change the block check character bytes 1 and 2 in the ICW. The interface address in the ABAR selects the proper scanner and the associated ICW. For an interpretation of the bytes mentioned above, see *Interface Control Word Format* in this chapter.

Output X'4C' (ICW Byte 1): This instruction may be used to write a control byte in the PDF array at the address specified by the PDF pointer (ICW bits 17.1 and 12.4-12.7). The PDF pointer is not changed by this instruction. The interface address in the ABAR selects the proper scanner and the associated ICW. For an interpretation of ICW byte 1, see PDF *Array Format* in this chapter.

Output X'4D' (ICW Byte 1): This instruction may be used to write two bytes in the PDF array at the address specified by the cycle steal PDF array pointer (ICW bits 17.0 and 12.0-12.3) and at that address plus one. (This instruction is normally used to start SDLC address (A) and control (C) characters in the PDF array.) The instruction places byte 0 in the first address and byte 1 in the second address. Execution of this instruction causes the cycle steal PDF array pointer to be incremented by two. The interface address in the ABAR selects the proper scanner and the associated ICW. For an interpretation of the bytes mentioned above, see *PDF Array Format* in this chapter.

causes the cycle steal PDF array pointer to be incremented by two. The interface address in the ABAR selects the proper scanner and the associated ICW. For an interpretation of the bytes mentioned above, see *PDF Array Format* in this chapter.

Output X'4E' (ICW Bytes 12, 13, and 17): This instruction may be used to set the contents of the cycle steal PDF array pointer and the PDF array pointer, the sequence and cycle steal message count fields, and the state of the request-to-send turnaround control bit. The interface address in the ABAR selects the proper scanner and the associated ICW. For an interpretation of the fields and bits mentioned above, see *Interface Control Word Format* in this chapter.

Output X'4F' (ICW Bytes 14-15): This instruction may be used to reset ICW bits 14.0, 14.1, 14.3, 14.4, 14.6, and 14.7. The remaining bits of byte 14 and all bits of byte 15 can be set or reset according to the state of the bits in the register specified by the Output instruction. For an interpretation of these bits, see *Interface Control Word Format* in this chapter.

Diagnostic Functions

The Type 3 or Type 3HS Communication Scanner has three diagnostic functions available to the control program: (1) the diagnostic wrap test, (2) the IBM moderm wrap test, and (3) the ICW diagnostic test. These tests are run under the control of the scanner program and provide online testing as described in the following sections. These diagnostics cannot be executed for an autocall interface.

For line interfaces attached through any one scanner, either a diagnostic wrap test or a modem wrap test can be performed, but not simultaneously. However, these tests can be performed on two different scanners simultaneously.

Diagnostic Wrap Test

The Type 3 or Type 3HS Scanner diagnostic wrap test provides a means of locating defects in the line control logic and line-interface transmit and receive logic. It also provides a method of online program testing. Diagnostic wrap tests can be performed online without affecting the normal program operation or the lines not in diagnostic mode. Three variations, or modes, of the diagnostic wrap test are available; these are specified by the settings of the diagnostic bits 0 and 1 (ICW bits 3.1 (5.5) and 3.2 (5.6), and the diagnostic mode bit (ICW bit 3.3).

In *normal diagnostic mode* (ICW bit 3.3 on), test data is transmitted from the scanner to one line interface and returned over another line interface. This test requires one installed line interface (line set) to act as the transmit line and one or more other line interfaces (line sets) to act as receive lines. Any line interface installed in the Type 3 or Type 3HS Scanner can be a transmit or a receive line; however, only one transmit line at a time in a scanner may be engaged in transmitting diagnostic test data.

In *diagnostic 0 mode* (diagnostic bit 0 on), the test data is wrapped internally within the scanner, instead of being passed from one line interface to the other. A receive line address and a transmit line address must be specified as in the normal diagnostic mode test, but no line sets need be installed at those addresses. The diagnostic 0 mode test allows the control program to test the scanner data out leads and to transmit data directly from one ICW to another within the same scanner. After the lines have been placed in diagnostic 0 mode, all normal line functions may be simulated.

In *diagnostic 1 mode* (diagnostic bit 1 on), the scanner is inhibited from modifying or reacting to the transmitted or received data stream. That is, it does not insert SYN characters, 0-bits, or SDLC flag characters into data it is transmitting over the transmit line, does not delete any control characters or 0-bits from data it is receiving over the receive line, and does not perform character translation on either transmitted or received data. Diagnostic 1 mode may be used in combination with either normal diagnostic mode or diagnostic 0 mode.

Test is initiated under program control by executing Output X'45' and Output X'46' instructions to all lines to be tested. The Output X'45' instruction is executed with byte 1, bits 0-3 set for proper line control and byte 1, bit 7 set to 1 to indicate PCF state X'1' (set mode). The remaining bits of this Output instruction are set to 0. See PCF state X'1' in this chapter for further information on set mode.

Output X'46' must be set as follows:

Byte 0, bit 0: NRZI (ICW bit 3.0): When set to 1, this bit causes bit 5.4 to be set. This bit is used to select NRZI operation of an SDLC line.

Byte 0, bit 1: Diagnostic bit 0 (ICW bit 3.1): When set to 1, this bit causes ICW bit 5.5 to be set, which in turn causes data to be transferred (wrapped) from the transmit line to the receive line at the scanner–LIB interface. (When the bit is set to 0, the transfer occurs at the line set if byte 1, bit 1 is set.) This allows the functioning of a line interface to be tested even if no line set is installed at that interface.

Byte 0, bit 2: Diagnostic bit 1 (ICW bit 3.2): When set to 1, this bit causes ICW bit 5.6 to be set, which in turn causes the scanner to assume a "do-nothing" state for transmit and receive operations. Recognition of control characters and insertion and deletion of zeros are inhibited when the scanner is in this state, thus allowing the program to control the bit stream when the scanner is in transmit mode.

Byte 0, bits 3-7: These bits are 0.

Byte 1, bit 0: This bit is 0.

Byte 1, bit 1: Diagnostic Mode (ICW bit 3.3)—This bit must be set to 1 for the normal diagnostic mode test.

Byte 1, bit 2: Data Terminal Ready (ICW bit 3.4)—This bit must be set to 0.

Byte 1, bit 3: Synchronous Clock (ICW bit 3.5)—This bit must be set to 1.

Byte 1, bit 4: External Clock (ICW bit 3.6)—This bit must be set to 0 to select a business machine clock.

Byte 1, bit 5: Data Rate Select (ICW bit 3.7)—This bit may be either 1 or 0.

Byte 1, bits 6-7: Oscillator Select 1 & 2 (ICW bits 4.0-4.1)—These bits are set to select an available line oscillator (business machine clock). For proper setting, see *Business Machine Clocks* in this chapter. All wrap test lines must select the same oscillator.

After the set modes are issued, the affected line interfaces can be exercised through any sequence of point-to-point or multipoint operations.

During diagnostic wrap operations both the 'data set ready' lead and the 'clear to send' lead are simulated active to prevent the Type 3 Scanner from setting a modem check (ICW bit 0.3).

The control program should set ICW bit 13.2 (RTS turn-around control) if half-duplex operation is required.

Programming Notes

1. Only one interface per Type 3 or Type 3HS Scanner may be in a transmit state at any given time during the operation.
2. The line used for transmit should be the last line to be issued the set mode instruction.
3. Diagnostic wrap tests cannot be executed on an autocall interface.
4. During a diagnostic wrap operation, the line control definer (LCD) of the line or lines in diagnostic receive mode must agree with the LCD of the line in diagnostic transmit mode regardless of the common-carrier or IBM equipment physically attached to the line.

Modem Wrap Test

The modem wrap test checks the scrambler circuits of IBM 3872, 3874, and 3875 modems under program control. The modem test can be performed online without affecting the normal operation of other lines, and may also be performed simultaneously on any or all interfaces for which the test function is defined.

To execute the modem wrap test, the control program must execute an Output X'46' instruction to set the interface control word SDF as follows:

SDF bit 0: When set to 1, this bit causes ICW bit 5.4 (NRZI control) to be set. This bit can be set to 1 to cause the SDLC line to operate in NRZI mode. For non-NRZI operation this bit should be 0.

SDF bit 1: When set to 1, this bit causes ICW bit 5.5 (diagnostic bit 0) to be set. This bit must be 0 to conduct a modem wrap test.

SDF bit 2: When set to 1, this bit causes ICW bit 5.6 (diagnostic bit 1) to be set. This bit should be set to 1 to conduct a normal modem wrap test; it can be set to 0 for a wrap test of a full-duplex modem.

SDF bit 3: This bit must be set to 1 to cause the 'diagnostic mode' latch to be set in the line interface hardware, which conditions the modem for testing.

SDF bit 4: This bit must be set to 1 to activate 'data terminal ready'. When this is set, together with the diagnostic bit, a modem wrap test can be performed instead of a diagnostic wrap test.

SDF bit 5: This bit must be set to 1 to provide synchronous clocking.

SDF bit 6: This bit must be set to 1 if the modem provides the clocking and to 0 if the modem does not provide the clocking.

SDF bit 7: This bit may be either 0 or 1.

SDF bits 8 and 9: These bits must select an internal oscillator whose speed is less than one-half the clock speed if the IBM modem provides the clocking. If the modem does not provide the clocking, the bits must select an internal oscillator whose speed matches that of the modem. For the proper setting, see *Business Machine Clocks* in this chapter.

After the set mode instruction is executed, the interface should be put in PCF state X'8' (transmit initial) to cause 'request to send' to be raised. Before this is done, the control program should set the RTS turnaround control (ICW bit 13.2) to allow a line turnaround to occur with the 'clear-to-send' lead active. Upon detecting 'clear to send,' the scanner transmits one pad character and then (assuming that the PDF array is empty) continuous marks, turns the line around (the scanner enters PCF state X'5'), and makes a level 2 interrupt request to the control program.

The program can now test the operation of the modem scrambler circuits by setting the PCF to X'7' (receiving in-phase) and checking the received data for all marks for a period of at least one second.

ICW Diagnostic Mode Test

The ICW diagnostic mode test permits the ICW local store to be exercised as a memory element. In this mode, the ABAR is used an an address register to allow access to the bits of a selected ICW; diagnostic programs may then set and reset the ICW bits as desired.

To place the scanner in diagnostic mode, an Output X'43' instruction in which bits 0.0 and 0.6 of the register specified by the R field are on must be executed. This instruction disables the scanner and places it in diagnostic mode. Individual bits can then be changed by placing the desired ICW address in the ABAR with an Output X'40' instruction and then using appropriate Output instructions to set and reset the bits. Figure 8-5 shows which Output instructions are associated with various ICW fields.

To restore the scanner to normal mode requires an Output X'43' instruction that sets the appropriate bits.

Chapter 9: Type 1 and Type 4 Channel Adapters

This chapter gives the reader a basic understanding of the operation of the Type 1 and Type 4 Channel Adapters and the requirements necessary to program the adapter.

With the Type 1 or Type 4 Channel Adapter (CA), the communications controller establishes and maintains communications with the byte-multiplexer channel of an IBM System/360 or System/370. With the Type 4 CA, the controller may also communicate with a block multiplexer channel or selector channel of a System/370 in native mode only. With the proper programming support, the Type 1 or Type 4 CA allows the controller to operate in a native 3704/3705 mode and/or in an emulation mode, emulating the 2701, 2702, or 2703 transmission control units.

The Type 1 and Type 4 CA rely heavily on the program to perform control operations. Data transfers across the channel interface occur in multibyte bursts with program intervention required before and after each burst. The Type 1 CA allows bursts of up to 4 bytes. The Type 4 CA, when operating in extended buffer mode, allows bursts of up to 32 bytes; when operating in cycle steal mode, the Type 4 CA allows bursts of up to 256 bytes. These modes of operation are described below. Channel I/O command decoding and interpretation, data transfers between the channel adapter and storage, ending status generation, and various other functions must generally be performed by the program.

Because the Type 1 and Type 4 Channel Adapters are similar in operation in most respects, only the differences are identified as pertaining to one type or the other. Otherwise, the term *channel adapter* (or CA) refers to both types of adapter.

Operation and Data Flow

The channel adapter receives an address from the host processor and determines whether the host wants to communicate with the controller in native mode or emulation mode. The mode of operation (native or emulation) is then set and initial selection completed. The CA then requests an initial level 3 interrupt to make this information available to the control program via input instructions.

Data from the host channel interface is received into the data buffers where the control program must retrieve it by executing input instructions and placing the bytes in storage. Channel End and Device End are generated by the control program when the complete message or block of data is received.

When data transfer is from the channel adapter to the host channel, the control program may request an attention interrupt from the host processor. The host processor must initiate an initial selection sequence, and the control program must load the data buffers with the byte to be transferred. Data from the data buffers can then be transferred across the channel interface. Channel End and Device End are generated by the control program when the complete message or block of data has been sent.

Type 1 and Type 4 CA Modes of Operation

The CA has two modes of operation—Native Subchannel Mode (NSC) or Emulation Subchannel Mode (ESC). With the proper programming support, the CA allows the controller to operate in NSC and ESC modes concurrently or separately.

Native mode permits servicing any number of lines up to 352 (32 for a 3704), using only one host subchannel address. The line address decoding is handled by the control program. Initial Program Load must always be handled in NSC mode.

Emulation mode allows the controller to emulate the 2701, 2702, and 2703 transmission control units using existing host programs and subchannel addresses.

Note: *Most operations of the CA are identical whether in native or emulation mode. Throughout this chapter, the exceptions and/or differences in operation due to native or emulation mode are noted by an NSC or ESC heading on the paragraph that describes the particular operation. All text that is not designated as either NSC or ESC can be assumed to apply equally to both modes of operation.*

Extended-Buffer and Cycle Steal Mode of Operation: The Type 4 Channel Adapter can operate in extended-buffer (EB) mode or in cycle steal mode (but not in both at once) instead of normal mode (non-EB, non-cycle steal mode).

Operation of the Type 4 CA in non-EB, non-cycle steal mode is identical to that of the Type 1 CA.

When operating in normal mode (non-EB, non-cycle steal mode), the Type 4 CA can transfer a maximum of four bytes over the channel to or from the host processor before interrupting the control program to obtain more data. When operating in EB or cycle steal mode, the Type 4 CA can (with proper control program support) transfer up to 32 bytes (in EB mode) or up to 256 bytes (in cycle steal mode) over the channel before interrupting the control program. Two bits in the EB/cycle steal mode control register determines whether the Type 4 CA is to operate in EB or cycle steal mode. An Output X'6C' instruction must be executed to set or reset these bits. An Output X'62' instruction in which bit 0.7 is 1 will also reset the EB/cycle steal control bit.

Programming Note

For a Type 4 CA cycle steal operation, an Output X'6C' instruction in which bit 0.1 (cycle steal mode bit) is 1

must be executed before data is placed in the cycle steal address register or byte count register.

Channel Adapter States

The CA operates in one of three active states under direction of the control program: (1) initial selection state, (2) data transfer state, or (3) status transfer state. When not active, the CA is in a ready mode; that is, the adapter can accept instructions but is not in one of the active states.

Initial Selection State

The initial selection state is entered when the host processor begins an initial selection sequence. The CA continually monitors the channel interface for one of its assigned addresses. If one of these addresses is detected, the CA traps this address and proceeds with the initial selection. If the command is received without error (correct parity), an initial status of all zeros is returned unless the command is a Test I/O or a No-Op. (See *Channel Adapter Status Presentation* in this chapter for Test I/O and No-Op exceptions.) If the command has bad parity, the CA returns Unit Check status to the host channel.

When the command from the host is a No-Op, the CA returns Channel End, Device End, and performs no further action.

During initial selection, the I/O device address and the command are stored in their respective channel adapter registers (see below). A level 3 interrupt is then requested by the initial selection hardware, and control is passed to the level 3 interrupt program.

Data Transfer State

The data transfer state is entered when the control program initiates a data transfer sequence. Data transfer can be from the host processor to the controller or from the controller to the host processor. The data is transferred across the channel under hardware control. When the data transfer ends, the channel adapter hardware signals the control program with a level 3 interrupt request.

Status Transfer State

The status transfer state is entered when the control program initiates a status transfer sequence. The status information byte is transferred to the host during this sequence.

Channel Adapter Registers

Various hardware registers are available to the control program for interface between the CA hardware and the levels 1 and 3 program routines. The following sections briefly describe these registers and the method of program access. See Appendix B for the bit definitions of the I/O instructions and the registers.

Initial Selection Control Register (ISCR)

This one-byte register contains information identifying the event that caused the CA Initial level 3 interrupt request. The register is available to the control program with an Input X'60' instruction.

Data/Status Control Register (DSCR)

This two-byte register contains control information used when passing data and status bytes across the channel interface. The bits in this register are set by the control program (Output X'62') and the CA hardware as a result of either a channel data or status transfer. This register is available to the control program with an Input X'62' instruction.

Initial Selection Address and Command Register (ISACR)

This two-byte register contains the I/O device address and the command byte presented to the channel adapter during initial selection. This register is available to the control program with an Input X'61' instruction.

Initial Selection Status Register

This one-byte register contains the status byte generated and presented by the channel adapter hardware during initial selection sequences except under the following conditions.

NSC: The NSC status byte from the NSC status register is presented instead of the hardware generated status when (1) an initial selection sequence occurs for the native mode subchannel and (2) the NSC status byte provided by the control program has not been accepted by the host (as in the case of stacked status).

ESC: The ESC status byte provided by the control program is presented instead of the hardware generated status when (1) an initial selection sequence occurs for an emulation address (Test I/O initial selection and addresses compare) and (2) the control program has signaled that both an ESC status transfer sequence is required and that ESC Test I/O status is available.

NSC Status Register

This one-byte register contains the current status of the NSC and is gated over the channel interface during NSC status transfer sequences. The control program should set the NSC status by executing an Output

Error/Control/Condition Register
This one-byte register contains detected hardware errors and asynchronous hardware control information. The register can be accessed by an Input X'67' instruction.

Local Store Registers
These two-byte registers provide buffering for the I/O device address used in all data and status transfer sequences initiated by the controller, and up to four bytes of data for inbound/outbound data transfer sequences in non-EB mode (up to 32 bytes of data for a Type 4 CA in EB mode). In EB mode a separate register stack is used to contain the data. When the controller is in emulation mode, the ESC final status is included along with the transfer address. These registers are as follows.

Transfer Address/ESC Status Register: This register can be accessed by executing an Input X'63' and loaded by executing an Output X'63'. The transfer address portion (byte 0) contains the I/O device address to be presented to the multiplexer channel when the controller initiates any data/status transfer sequence. The ESC status byte portion (byte 1) contains the status byte to be presented to the multiplexer channel on completion of an ESC command.

Data Buffer Byte 1/Data Buffer Byte 2 Register: This two-byte register contains the first and second data bytes transfered across the channel interface during an inbound or outbound data transfer sequence (in non–EB mode). The register can be loaded by executing an Output X'64' instruction or accessed by executing an Input X'64' instruction.

Data Buffer Byte 3/Data Buffer Byte 4 Register: This two-byte register contains the third and fourth data bytes transferred across the channel interface during an inbound or outbound data transfer sequence in non-EB mode. The register can be loaded by executing an Output X'65' instruction or accessed by executing an Input X'65' instruction.

Extended-Buffer Mode Local Store (Type 4 CA Only)
The local store register for operation of a Type 4 Channel Adapter in extended-buffer (EB) mode provides buffering for up to 32 bytes of data for both outbound and inbound data transfer sequences in either NSC or ESC mode.

This register can be loaded by first executing an Output X'6C' instruction to place the CA in EB mode and reset the EB mode address register, then executing a sequence of Output X'6D' instructions, each of which loads two bytes into the register. Thus 16 Output X'6D' instructions (preceded by an Output X'6C') are needed to load the maximum of 32 bytes into the register. (A delay of at least one instruction time is required between the Output X'6C' and the Output X'6D' instructions, and between successive Output X'6D' instructions.)

The EB mode local store can be accessed by executing an Input X'6C' instruction to reset the EB mode address register and then executing a sequence of Input X'6D' instructions, each of which loads two bytes from the local store into the register specified by the instruction. (The first and second bytes are moved into bytes 0 and 1 of the specified register. Thus 16 Input X'6D' instructions (preceded by an Input X'6C') are required to read 32 bytes from the EB mode local store. (A delay of at least one instruction time is required between the Input X'6C' and the first Input X'6D' instructions, and between successive Input X'6D' instructions.)

Note: *Powering on or resetting of the 3705 (via the control panel) does not ensure that the EB mode local store has correct parity. The control program must do this before accessing the local store by setting EB mode operation in the CA with an Output X'6C' instruction, executing 16 Output X'6D' instructions, then resetting the EB mode with an Output X'6C' instruction.*

Extended-Buffer Mode Control Register (Type 4 CA Only)
This register contains information that controls the operation of the Type 4 CA while it is operating in extended-buffer mode. The register can be accessed by an Input X'6C' instruction while the CA is in this mode. When servicing a Type 4 CA L3 interrupt, the control program can execute Output X'6C' instructions to set and reset individual bits in the register.

Extended-Buffer Mode Counter Register
This register is a six-bit counter used to address the 32-byte EB mode local store. The counter is incremented by two bytes while the CA is in EB mode when an Output X'6D' or Input X'6D' instruction is executed. It is reset to zero by an Output X'6C' instruction or (when the CA is in EB mode) by an Output X'62' or Input X'6C' instruction. An Input X'6C' instruction initially resets the counter and then increments it by two. Each subsequent Input X'6D' or Output X'6D' instruction increments the counter by two.

I/O Device Addresses

The channel adapter must determine whether to recognize the I/O device address presented when initial selection occurs. It must also determine which I/O device address to present when the control program signals the channel adapter to perform a data/status sequence. The following sections describe the methods of determining initial selection and data transfer addresses.

Initial Selection Address
The address byte presented during initial selection must have correct parity, or the channel adapter will not decode the address. The initial selection addresses that the channel

adapter recognizes are determined by plug options wired by the customer engineer from information supplied by the user.

The address assigned for the native subchannel (NSC) of a Type 1 CA or a single Type 4 CA can be within the range of addresses assigned for ESC but cannot also be used for emulation.

With a Type 4 CA, the following restrictions also apply.

1. If a 3705 contains two Type 4 CAs running under the standalone emulation program, the NSC address can be assigned within the range of ESC addresses; but (a) the NSC address cannot also be used for emulation, and (b) the NSC address can be used only with the channel that IPLs the 3705.
2. If a 3705 contains two or more Type 4 CAs and the N-ROS specify feature, the NSC address can be assigned within the range of addresses assigned for ESC but cannot also be used for emulation.
3. If a 3705 contains an IPL Select switch with two Type 4 CAs running under the PEP extension of NCP/VS, the NSC address cannot be within the range of addresses assigned for ESC.

Note: For proper IPL Select switch operations procedures, see Figure D-1 in Guide to Using the IBM 3705 Communications Controller Control Panel, GA27-3087.

4. For 3705 containing a single Type 4 CA, the NSC address can be assigned within the range of addresses assigned for ESC but cannot also be used for emulation.

The assigned NSC address can be checked by executing an Input X'67' when the channel is enabled.

When power is turned on, the channel adapter is placed in such a state that it will not recognize any ESC addresses until after the interface is enabled, the CCU is initialized, and the control program executes an Output X'67' instruction with byte 1, bit 5 = 1 (Set ESC Operational).

When a CA Initial L3 interrupt request is caused by an initial selection, the program can determine the I/O device address by executing an Input X'61'. This interrupt request can be caused by an initial selection sequence for any operational ESC address or for the native mode subchannel address. The program should be prepared to handle initial selection sequences for all operational addresses.

NSC: The NSC address can be assigned any value in the range of 0-255. If the Two Channel Switch Feature is installed, the NSC addresses for interfaces A and B are assigned separately and can be either two different addresses or the same address used for both interfaces.

Because the native mode uses only one subchannel address, the terminal address must be transferred from the host as data. The location and format of these addresses must be coordinated between the host program and the control program in the controller.

ESC: The ESC addresses must be a group of contiguous addresses. For the 3705, the lowest address (L) in the group can be set to 0 or any multiple of 16 from 16 to 240. The highest address (H) in the group can be set to any value greater than (L) that is one less than a multiple of 4, from 3 to 255. The range of recognizable ESC addresses can be set to include a minimum of 4 or a maximum of 256 addresses. For the 3704, the lowest address can be any even number and the highest address can be any odd number. The range of addresses can be a minimum of 2 or a maximum of 32. This range must be the same for both interface A and interface B if the Two Channel Switch feature is installed on the 3704 or 3705.

Note: *If emulation is not required, the machine can be wired (by the customer engineer) so that no ESC addresses are recognized.*

Transfer Sequence Addresses

When the control unit initiates a data/status transfer sequence, it must present the I/O device address associated with the transfer. Since this address is variable, it must be provided by the control program. This is done by executing an Output X'63'.

Since Output X'63' allows the control program to provide any I/O device address in the range of 0-255, and the channel adapter cannot determine if this is the address that should be presented, the control program must ensure that the address is correct. An incorrect address results in improper channel operation.

Channel Adapter Interrupt Requests

The Type 1 or Type 4 Channel Adapter can initiate interrupt requests for either level 1 or level 3 service. Level 1 requests are caused when the CA detects an error or check condition. Two different level 3 interrupt requests can be set for the purpose of controlling channel adapter operations: the CA Initial L3 and the CA Data/Status L3 interrupt request.

Level 1 Interrupt Request

When one of the following checks occurs, a level 1 interrupt request is set and the corresponding bit is set in error/control/condition register. This register is made available to the control program by executing an Input X'67' instruction. See Appendix B for the placement of the bits within this register.

1. Channel Bus In Check: This error is set when the CA hardware detects bad parity in the byte to be sent to the host.
2. In/Out Instruction Accept Check: This error is set when the CA hardware detects the execution of a valid input/output instruction at an invalid time (that is, the CA is actively handling a data or status transfer sequence and any Input or Output instructions except X'67' is executed).
3. CCU Outbus Check: This error is set when the CA hardware detects bad parity on the CCU Outbus.
4. Local Store Parity Check: This error is set when the CA hardware detects bad parity on data being read out of the local store registers.

See the *Error Indications* section in this chapter for information on how to handle these errors.

Level 3 Interrupt Request

Two different level 3 interrupt requests can be set: an initial L3 and a data/status L3. These are identified to the control program when Input X'77' is executed. Either one or both of these requests can be set. Several different events can cause either to be set.

If the CA initial L3 is the only interrupt request set, it can be serviced without being concerned that a CA data/status L3 interrupt request will occur. Any pending data/status transfer sequence is inhibited until the CA initial L3 request is reset. The level 3 interrupt can be reset by either an Output X'60' or Output X'62' instruction except that when a system reset occurs, an Output X'67' must be executed to reset the system reset. If an Output X'62' is executed to reset the CA initial L3 request, the control program must be prepared to re-initiate a data/status transfer if one was pending at the time the initial L3 interrupt was reset.

If just the CA data/status L3 interrupt request is set, the program must be aware that a system reset sequence can occur during servicing of the data/status interrupt request. If the system reset occurs before the Input X'62' is executed, the conditions that caused the interrupt are lost to the program. A system reset causes an initial L3 interrupt request and resets all hardware latches except the 'system reset' latch.

If both interrupt requests are set, the program must service both requests before executing the output instruction to reset them. If both are set and the initial L3 interrupt request was caused by a system reset, the conditions that caused the data/status L3 will be lost due to the system reset.

Initial L3 Interrupt Request: A CA initial L3 interrupt request is made when (1) an initial selection sequence occurs, (2) a system reset sequence occurs, or (3) NSC status is cleared because of an initial selection sequence. When an initial L3 interrupt occurs, Input X'60' can be executed to determine the cause.

Once the CA initial L3 interrupt request is set, the channel adapter automatically responds with a short control-unit-busy status (Control Unit End, Status Modifier, Busy) to all initial selection attempts. This status is indicated until the control program signals the channel adapter to reset the condition that caused the interrupt request to be set. During this period, no channel command can be accepted in either emulation or native mode. The control program should therefore signal the channel adapter as soon as possible to reset the cause of the interrupt request.

Once the CA initial L3 interrupt request is set, subsequent data/status transfer sequences are inhibited until the interrupt request is reset. This means that the initial L3 interrupt request and the data/status L3 interrupt request can both be set only if the data/status request occurs first, and only if the initial L3 interrupt request is not the result of a system reset.

The CA initial L3 interrupt request can be reset by executing an Output X'60', X'62', or X'67', depending on the cause of the interrupt. (See the preceding section, *Level 3 Interrupt Request,* for restrictions on resetting level 3 interrupts.)

Data/Status L3 Interrupt Request: A CA data/status L3 interrupt request can be set by

- any of the five data/status transfer sequences
- a suppress-out monitor interrupt
- a program-requested interrupt
- a selective service reset
- A CCU Outbus check when the adapter is in one of the five data/status transfer sequences (only during an Output X'62' for a 3704)
- a channel stop or interface disconnect
- recognition of an ETB or ETX character when a Type 4 CA is in EB mode and the ESC mode is enabled
- recognition by a Type 4 CA of a number of consecutive SYN characters (as specified in the Output X'62' instruction) when (1) the channel adapter is in EB or cycle steal mode, (2) the ESC mode is enabled, and (3) the 'monitor SYN' latch (Input X'6C' instruction bit 0.4) is on.

Automatic Priority Selection for multiple Type 4 CAs: If more than one Type 4 CA has a level 3 interrupt request pending, communications controller hardware automatically determines which CA is to be selected for handling of its interrupt request. (This function applies only to multiple Type 4 CAs. It is not available for other combinations of channel adapters.)

The selection is based on which of the Type 4 CAs has the higher-priority level 3 interrupt request pending. The priority sequence is:

Priority outbound data transfer sequence (highest)
Outbound data transfer sequence
Initial selection interrupt

Inbound data transfer sequence
Other data/status interrupts (lowest)

(Byte 1, bit 5 of the Output X'62' instruction specifies whether the outbound data transfer sequence has priority status or not.)

The automatic selection occurs only when requested by the control program. To do so, it must execute an Output X'67' instruction in which all bits are 0. The next Input X'77' instruction executed will then automatically select and access the states of the CA currently having the higher-priority interrupt request.

The control program can cause a data/status L3 interrupt by executing an Output X'67' instruction with the proper bits set for the operation desired. See Appendix B for the output instruction bit definitions. The program should not initiate another transfer sequence or monitor for the inactive condition of the 'suppress out' line unless the initial L3 or the data/status L3 interrupt has been set. The control program can signal the channel adapter at any time to cause a program requested interrupt when conditions permit. When a data/status L3 interrupt occurs, Input X'62' can be executed to determine the cause.

The data/status L3 interrupt request can be reset by executing an Output X'62' with the appropriate bits set. Refer to Appendix B, Output X'62' for bit definitions.

When a channel-stop or interface-disconnect condition is detected during an outbound or inbound data transfer, in EB mode, the number of bytes successfully transferred can be obtained by executing an Input X'6C' instruction and examining bits 2-7 of byte 1 of the register loaded by the instruction.

Channel Commands

The channel adapter recognizes any I/O command byte combination as a valid command if odd parity is maintained on the I/O channel interface and there is no pending activity on the channel. Except for those commands listed below, the channel adapter hardware accepts the command, returns an initial selection status of X'00' and causes a CA initial L3 interrupt request. The channel adapter hardware initially accepts the full range of commands (X'00' through X'FF'). It is the responsibility of the control program to decode the command, determine its validity and respond accordingly.

The hardware recognizes the following commands and takes the action listed.

NSC:

I/O No-Op (X'03')—When this command is presented to the NSC address, an immediate initial status of CE, DE is presented by the hardware if the channel adapter is free of commands. If the NSC has a pending status available (a previous NSC status byte has been stacked), the hardware presents it with the 'Busy' status bit as initial status to the No-Op command.

Test I/O (X'00')—When this command is presented to the NSC address, the hardware presents the current status of the NSC. If the NSC is free of commands, the hardware responds with a X'00' status byte during the initial status presentation to the Test I/O. If the NSC hardware has a pending status available in the NSC status register, this status is presented during the initial status presentation to the Test I/O. The busy bit does not accompany this status. If the NSC is currently executing a command, but no status is available, the Busy status bit is presented as initial status.

Test I/O and No-Op must be recognized by the control program if these immediate commands are stacked.

Write IPL (X'05')—When this command is presented to the NSC address, the hardware accepts the command, returns the initial status byte of X'00', and causes a CA initial L3 interrupt request. The hardware also notifies the CCU (Central Control Unit) of the reception of this command by raising an internal interface line to the CCU. See *Initial Program Load* in Chapter 5 for an explanation of the IPL procedures.

ESC:

I/O No-Op (X'03')—When this command is presented to a valid ESC address, the hardware presents an immediate CE, DE initial selection status.

Test I/O (X'00')—Refer to Emulation Mode Test I/O in this chapter for an explanation of this operation.

The following commands are standard channel I/O commands issued by the host access method for either native or emulation mode. The control program has the responsibility to decode the command and initiate the appropriate action. Refer to *Inbound Data Transfer* and *Outbound Data Transfer* in this chapter for the sequence of instructions that the control program must execute for proper data transfer.

Write (X'01')—The channel adapter hardware accepts this command and returns an initial selection status of X'00'. The purpose of the command is to transfer data from the host processor to the communications controller. The data may be either user data or control information to inform the control program of a function to be performed.

Read (X'02')—The purpose of this command is to transfer data from the communications controller to the host processor. The channel adapter hardware accepts the command and returns an initial selection status of X'00).

Sense (X'04')—This channel command should result in the transfer of one byte of sense data from the communications controller to the host. The channel adapter hardware

accepts the command and returns an initial status of X'00'. Normal ending status is CE, DE unless a Halt I/O is detected when the adapter is not initialized. In this case, a CE, DE, UC is returned to the channel. It is the responsibility of the control program to recognize the command, load the sense byte into a data register, and send it to the host. The transfer is the same as a data transfer with one byte of data. The sense byte for the Type 1 and Type 4 Channel Adapters are the same as for the Type 2 Channel Adapter. See Input X'53' in Appendix B for a definition of each bit.

Channel Adapter Status Presentation

Initial Selection Status
Initial Selection status is generated by hardware and presented to the channel during the initial selection sequence. The host processor must examine the status byte to determine whether the command was accepted by the channel adapter. If the command was not accepted, the status byte contains bits indicating the reason.

The following paragraphs describe the initial selection status bytes that can be returned to the host processor channel and their meanings.

X'00' (Zero Status):

NSC: The hardware accepts a command byte, other than a No-Op, and the NSC is free of commands.

ESC: The hardware accepts a command byte other than a Test I/O or No-Op command, and there is no initial select L3 interrupt request or no program requested L3 interrupt request pending.

X'02' (Unit Check): The hardware detects even parity in the command byte.

X'0C' (Channel End, Device End): This status is returned by the hardware as an immediate response to a No-Op command.

X'10' (Busy):

NSC: The NSC hardware is active with another command and has not presented final status to that command or, for the Type 4 CA only, an Output X'66' with bit 0.4 set to 1 was executed to place the CA in the 'long busy' state.

X'70' (Status Modifier, Control Unit End, Busy): This status is returned as a short control-unit-busy sequence to any initial selection sequence when any of the following conditions are present:

- The CA has an initial selection L3 interrupt request pending due to the acceptance of a previous command, and the control program has not yet reset the interrupt request.
- The CA hardware has previously detected a system reset indication and caused a CA initial L3 interrupt request, and the control program has not reset the initial select L3 interrupt request.
- The CA hardware has previously detected a selective reset during a service transfer and caused a CA data/status L3 interrupt request, and the control program had not reset this request.
- A program requested interrupt is pending, and the control program has not reset the request.

ESC: This is the normal initial selection status returned by the hardware when a Test I/O is issued to an ESC address.

Busy Bit and Status Information:

NSC: When an initial selection occurs for the NSC and status is pending in the NSC status register, the Busy bit, in addition to the pending status, is returned.

Pending Status:

NSC: When a Test I/O command is issued to the NSC and status is pending in the NSC status register, the pending status is returned without the Busy bit.

Final Status
The final status is a control program generated status and should be presented to the host processor upon completion of a command. Bit definitions for the final status byte must be coordinated between the control program and the host program for proper operation. Upon completion of a command, the control program should load the appropriate register with the status byte to be presented and initiate a final status transfer sequence. Refer to *Status Transfer Sequence* in this chapter for additional information.

Emulation Mode Test I/O
When a Test I/O command is issued to an ESC address, the hardware responds with initial selection status and also

causes CA initial L3 interrupt request. Although the initial selection status presented to the host is X'70' (Status Modifier, Control Unit End, Busy), byte 0, bit 0 of the CA initial selection control register (X'60') is set to 1 (normal initial selection). The control program should recognize the command and address and execute:

1. Output X'63'—To load the ESC address and the status byte to be presented to this Test I/O command.
2. Output X'62'—To set ESC Final Status Transfer Sequence, Reset Initial Selection, Reset Data/Status Control, and Set ESC Test I/O Status Available.

When the next initial selection sequence occurs, the hardware compares the address presented to the adapter with the address that had received the Test I/O command.

If these addresses compare and the subsequent command is a Test I/O command, the hardware presents the status byte that was loaded by the above instructions. The hardware then causes a CA data/status L3 interrupt request. When the control program executes an Input X'62', the ESC Final Status Transfer Sequence bit is on, indicating a successful completion of the Test I/O sequence.

The host access method must re-issue the Test I/O whenever the initial selection status is X'70'.

If the addresses do not compare during the initial selection sequence, or if the command is not a Test I/O, the hardware resets out of the ESC Test I/O mode and handles this sequence as a standard initial selection. If this occurs, the control program must reset the ESC final status transfer sequence by executing an Output X'62' instruction.

Between the time the Test I/O command is first issued and the time the control program executes the above Output X'62' and X'63' instructions, the hardware responds with an initial status of X'70' to any initial selection sequence from the host processor. In this case, an Output X'60' should not be used to reset initial selection because the address compare uses the address in the initial selection address control register. Refer to *Initial Selection Status* in this chapter for an explanation of X'70' status.

Native Mode Asynchronous Status

The control program initiates the presenting of asynchronous status to notify the host processor of an unusual condition or a required action.

Note: *The control program should not attempt to present asynchronous status when the interface is disabled (that is, byte 1, bit 4 of an Input X'67' instruction is 0).*

The control program initiates the action by requesting a CA program interrupt. This is done by executing an Output X'67' instruction. When the requested interrupt is allowed, the hardware sets a CA data/status L3 interrupt request.

The control program should then prepare to present the asynchronous status by:

1. Loading the address of the NSC (Output X'63').
2. Loading the NSC status byte to be presented (Output X'66').
3. Executing an Output X'62' with the NSC Final Status Transfer set to 1. Any Output X'62' instruction resets the program requested interrupt.

After the control program executes the Output X'62' instruction to present asynchronous status, it must execute an Input X'67' instruction to determine if the interface is enabled. If it is not, the program should then execute, in sequence:

1. Output X'67' (bit 1.7 must be on) to allow the interface to be disabled.
2. Output X'67' (bit 0.4 must be on) to reset the CA.
3. Output X'67' (bit 1.4 must be on) to allow the interface to be enabled.

Following these instructions, the control program must then reexecute the asynchronous status presentation.

At the completion of the status transfer, the hardware causes a CA data/status L3 interrupt to inform the control program of the results of the transfer. The control program should then execute an Input X'62' instruction. If the status byte is accepted, the NSC final status transfer sequence bit is one.

Stacked Initial Status

The host processor can stack all initial status responses except zero status (X'00') to a Start I/O. When an initial status is stacked, the hardware causes a CA initial L3 interrupt request. The control program must determine what status was stacked by analyzing the contents of the initial selection control register and the initial selection address and command byte register. This information is obtained by executing an Input X'60' and X'61'. The status and address of the stacked device must be presented later in a final status transfer. The control program must be able to distinguish between the NSC address and the ESC addresses to be able to load and transfer the proper status.

The following initial status is presented by the CA hardware and is capable of being stacked.

Channel End/Device End (X'0C') - The initial status is presented to an No-Op command. If the initial status is stacked, the initial status byte stacked bit is on in the initial selection control register (Input X'60'). The address and command byte can be obtained by executing an Input X'61' instruction.

Unit Check (X'02') - Unit Check is presented if the hardware detects even parity in the command byte. If this initial status is presented, the initial status byte stacked bit and the channel out bus check bit is on in the initial select control register (Input X'60'). The device address may be obtained by executing an Input X'61' instruction.

NSC: Zero or any pending status to a Test I/O addressed to the NSC.

If a Test I/O command is issued to the NSC and the status is stacked, the initial status byte stacked bit is on in the initial select control register (Input X'60'). The address and command may be obtained by executing an Input X'61' instruction. The control program should not execute an Output X'66' to load the stacked status in the NSC status register. The NSC hardware maintains the stacked status from a Test I/O command in the NSC status register until the host processor has accepted it.

ESC: Initial status byte to a Test I/O addressed to the ESC.

If a Test I/O command is issued to the ESC and the initial select status is stacked, the initial status byte stacked bit is on in the initial selection control register (Input X'60'). The address and command may be obtained by executing an Input X'61'. The control program should treat this the same as a stacked status while in an ESC final status transfer.

Stacked Final Status

When a final status or an NSC Channel End is stacked, the CA hardware causes a CA data/status L3 interrupt request. The control program should analyze the contents of the data/status control register (Input X'62') to determine which status was stacked. One of the following actions may be taken:

1. Test the level of the 'suppress out' line at the time the last Input X'62' was executed. If the 'suppress out' line was inactive, the control program can now attempt another transfer sequence. The suppressible status bit must be on for the second transfer.

NSC: Since the NSC stacked status is maintained in the NSC status register the stacked status should not again be placed in the NSC status register with an Output X'66' instruction.

ESC: The status byte along with the ESC address must be loaded by an Output X'63' when preparing an ESC final status transfer.

If the 'suppress out' tag line is active, the control program can queue the stacked status; or if no data services are required, it can set the suppress out monitor as described below.

2. The *suppress out monitor* may be used to notify the control program when the 'suppress out' line falls and when the status may be presented. To use this feature, the control program should execute an Output X'62' to reset the CA data/status L3 interrupt request and execute an Output X'67' to set a suppress out monitor interrupt. The hardware then causes a CA data/status L3 interrupt request when the 'suppress out' line becomes inactive. When the control program executes an Input X'62', the suppress out monitor interrupt bit is active. The stacked status can be transferred by loading the subchannel address and status (in the case of ESC final status) into a general register and executing an Output X'63' with the type of transfer indicated and reset suppress out monitor. The suppressible status bit (byte 1, bit 3) in Output X'62' must also be on.

NSC: When operating in NSC mode only, the control program can initiate another NSC status transfer immediately after being notified of a stacked status by executing an Output X'62' with the type of transfer indicated and the reset data/status L3 interrupt request bit on. The hardware does not attempt to transfer the status until the 'suppress out' line becomes inactive. It then transfers the status across the channel to the host. The suppressible status bit does not have to be on since the channel adapter hardware monitors the channel 'suppress out' tag line.

Programming Note

Whenever the channel adapter is in the ESC mode and the control program is presenting suppressible status, the suppressible status bit (byte 1, bit 3) must be on when an Output X'62' is executed. Status is suppressible if 'stacked status' is received for a particular line or when the line has been issued an interface disconnect. Refer to *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers Information* (GA22-6974) for further information on suppressible status.

Status Transfer Sequences

Upon completion of a command, the control program should present a final status associated with that command. The control program may choose to separate the Channel End and Device End on an NSC command. This status is transferred by executing the following output instructions.

ESC Final Status

Output X'63'—Loads the I/O device address that is presenting the status and the status byte that is to be presented.

Output X'62'—Sets the following control bits: (1) ESC final status transfer, (2) reset initial selection (if this status transfer is being initiated because of a stacked initial status), or (3) reset data/status interrupt (for final status transfer).

NSC Final Status

Output X'63'—Loads the address of the NSC (must be loaded only once at the beginning of the program if operating in NSC mode only).

Output X'66'—Loads the NSC status byte to be presented.

Output X'62'—Sets the following control bits: (1) NSC final status transfer, (2) reset initial selection (if this status transfer is being initiated because of a stacked initial status), or (3) reset data/status interrupt (for a final status transfer).

NSC Channel End Status

Output X'63'—Loads the address of the NSC (can be loaded only once at the beginning of the program if operating in NSC mode only).

Output X'62'—Sets the following control bits: NSC channel end transfer sequence and reset data/status interrupt.

When the NSC channel end transfer sequence bit is active during the execution of an Output X'62', the CA hardware loads Channel End Status (X'08') in the NSC status register.

When the Output X'62' instruction is executed in the above sequence, the CA hardware notifies the I/O channel that it requires service. In a hardware-controlled sequence, the CA hardware indicates that status is being passed to the host and gates the status byte out to the I/O channel. After this sequence is completed, the CA hardware causes a data/status L3 interrupt to inform the control program of the results of the status transfer.

The control program should react to the data/status L3 interrupt request by executing an Input X'62' instruction. If the status byte is accepted by the host processor, the related final status bit is on (that is, ESC or NSC final status transfer or Channel End transfer sequence).

If any unusual condition occurred during this transfer (that is, status stacked, selective reset, or interface disconnect), the related bits are on when the Input X'62' instruction is executed.

Data Transfer Sequences—Non-EB, Non-Cycle Steal Mode

Outbound or inbound data through a Type 1 CA or through a Type 4 CA that is not in extended-buffer mode or cycle steal mode is transferred through input and output instructions executed by the control program. As described in the following paragraphs, these I/O instructions must be in the correct sequence for proper transfer operations.

Outbound Data Transfer

When reacting to a read type I/O command, which requires data to be passed from the communications controller to the host processor, the control program must execute the following instructions.

Output X'63'—Loads the address of the I/O device sending the data.

NSC: If the CA is operating in NSC mode only, it is necessary to load this address only once. It remains constant for subsequent NSC transfers.

ESC: When operating in ESC mode, this address may change and must be updated when required.

Output X'64'—Places the first and second bytes of outbound data in the CA data buffer byte 1/data buffer byte 2 register.

Output X'65'—Places the third and fourth bytes of outbound data in the CA data buffer byte 3/data buffer byte 4 register.

Output X'62'—Sets the following control bits: (1) outbound data transfer sequence, (2) reset initial selection (if this transfer is the first after an initial selection), or (3) reset data/status interrupt and the request byte count. A maximum of four bytes may be transferred during one sequence.

When Output X'62' is executed, the CA hardware notifies the I/O channel that it requires service. In a hardware-controlled sequence, the CA then identifies itself by gating its I/O device address onto the I/O channel and passes the required data. The CA hardware then causes a CA data/status L3 interrupt to inform the control program of the completion of the transfer.

The control program should react to the CA data/status L3 interrupt by executing an Input X'62'. Assuming a normal data transfer, the outbound data transfer sequence bit

is on and the transferred byte count field reflects the number of bytes passed across the channel during this transfer sequence.

If any unusual conditions occurred during this transfer (that is, selective reset, interface disconnect or channel stop), their related bits are on when the Input X'62' was executed.

Inbound Data Transfer

When reacting to a write type I/O command, which requires data to be passed from the host processor to the communications controller, the control program must execute the following instructions.

Output X'63'—Loads the address of the I/O device that is transferring the data.

Output X'62'—Sets the following control bits: (1) inbound transfer sequence, (2) reset initial selection (if this is the first transfer after an initial select), (3) Reset data/status interrupt, and (4) the transferred byte count. A maximum of four bytes may be transferred during one sequence.

When the Output X'62' instruction is executed, the CA hardware notifies the channel that it needs service. In a defined sequence, the CA then identifies itself by gating its I/O device address onto the I/O channel and accepts the required number of bytes of data. The CA hardware then causes a CA data/status L3 interrupt to inform the control program of the completion of the transfer.

The control program should react to this interrupt by executing an Input X'62' instruction. Assuming normal data transfer, the inbound data transfer sequence bit is on and the transferred byte count field reflects the number of bytes of data passed from the host processor to the controller during this sequence.

If any unusual conditions occurred during this transfer (that is, selective reset, interface disconnect, channel bus out check, or channel stop), their respective bits are active when the Input X'62' is executed.

Data Transfer Sequences–EB Mode (Type 4 CA)

Outbound or inbound data through a Type 4 CA operating in extended-buffer (EB) mode is transferred via input and output instructions executed by the control program in the following sequences.

Outbound Data Transfer: When reacting to a read-type I/O command, which requests data to be passed from the communications controller to the host processor, the control program must execute the following instructions.

Output X'63'–Loads the address of the I/O device sending the data.

NSC: If the CA is operating in NSC mode only, it is necessary to load this address only once. It remains constant for subsequent transfers in NSC mode.

ESC: When operating in ESC mode, this address may change and must therefore be updated when required.

Output X'6C'–Places the CA in EB mode and requests the number of bytes to be transferred. (Byte 0, bit 0 of the instruction must be 1 to place the CA in EB mode; bits 3-7 of byte 1 specifies the number of bytes to be transferred. (00001 = 1 byte, 00010 = 2 bytes, . . . 11111 = 31 bytes, 00000 = 32 bytes). (A delay of at least one instruction time must precede execution of the Output X'6D' instruction.)

Output X'6D'–Loads two bytes into the EB mode local store. This instruction may be executed up to 16 times, one for each two bytes to be transferred to the CA (maximum: 32 bytes). (A delay of at least one instruction time must elapse between successive Output X'6D' instructions.)

Output X'62'–Sets the following control bits: (1) outbound data transfer sequence, (2) reset initial selection (if this data transfer was the first after an initial selection), or (3) reset data/status interrupt. In addition, bit 5 of byte 1 must be set to indicate a priority outbound sequence to the CA.

The control program should react to the CA data/status L3 interrupt by executing (1) an Input X'62' instruction (assuming a normal data transfer, the outbound data transfer sequence bit is on), and (2) an Input X'6C' instruction to determine the number of bytes transferred. Bits 2-7 of byte 1 indicate the number of bytes (000000 = no bytes, 000001 = 1 byte, 100000 = 32 bytes) transferred.

Finally, the control program should execute an Output X'6C' instruction to reset the EB mode of the CA (bit 0 of byte 0 is 0 to perform this reset), if data transfer in EB mode is no longer desired.

Inbound Data Transfer: When reacting to a write-type I/O command, which requests data to be passed from the host processor to the communications controller, the control program must execute the following instructions.

Output X'63'–Loads the address of the I/O device that is transferring the data.

Output X'6C'–Places the CA in EB mode, requests the number of bytes to be transferred, and activates the BSC control character recognition logic of the CA. (Byte 0, bit 0 of the instruction must be 1 to place the CA in EB mode, bits 3-7

of byte 1 specify the number of bytes to be transferred (00001 = 1 byte, 00010 = 2 bytes, . . . 11111 = 31 bytes, 00000 = 32 bytes). Bits 4, 5, 6, and 7 of byte 0 activate the control character recognition logic as follows:

bit 4 – SYN monitor control latch (1 = set, 0 = reset)
Note: *Any non-syn character received during the inbound sequence resets the 'syn monitor control' latch.*

bit 5 – DLE remember latch (1 = set, 0 = reset)
bit 6 – monitor for ASCII control characters (1 = yes, 0 = no)
bit 7 – monitor for EBCDIC control characters (1 = yes, 0 = no)

Output X'62'–Sets the following control bits: (1) inbound data transfer sequence, (2) reset initial selection (if this is the first transfer after an initial selection), (3) reset data/status interrupt, and (4) set SYN count (if 'SYN monitor control' latch was turned on with an Output X'6C' instruction). The bits of an Output X'62' instruction define the SYN count in the following manner.

Bit 1.6	*Bit 1.7*	*Number of SYNs*
0	1	1
1	0	2
1	1	3
0	0	4

When the Output X'62' instruction is executed, the CA hardware notifies the channel that it needs service. In a hardware-controlled sequence, the CA then identifies itself by gating its I/O device address onto the I/O channel and accepts the required number of bytes of data. The CA hardware then causes a CA data/status L3 interrupt to inform the control program of the completion of the transfer.

The control program should react to this interrupt by executing (1) an Input X'62' instruction (assuming a normal data transfer, the inbound data transfer sequence bit is on), and (2) an Input X'6C' instruction to determine the number of bytes transferred. Bits 2-7 of byte 1 indicate the number of bytes (000000 = no bytes, 000001 = 1 byte, . . . 100000 = 32 bytes) transferred. Bits 5, 6, and 7 of byte 0 indicate the state of the control character recognition latches, as follows:

bit 4 – SYN monitor control latch
bit 5 – DLE remember latch
bit 6 – ASCII monitor latch
bit 7 – EBCDIC monitor latch

(A delay of at least one cycle must precede execution of the instruction.)

Programming Note
Refer to "Data/Status L3 Interrupt Request" earlier in this chapter for other means of setting a CA data/status interrupt request.

Input X'6D'–Reads two bytes from the EB mode local store. This instruction can be executed up to 16 times, once for each two bytes to be read from the local store (maximun 32 bytes). (A delay of at least one instruction time must elapse between successive Input X'6D' instructions.)

Finally, the control program should execute an Output X'6C' instruction to reset the EB mode of the CA (bit 0 of byte 0 is 0 to perform the reset, if data transfer in EB mode is no longer desired.

Input/Output Instructions

The X'60' through X'6F' input/output instructions are used to manipulate data, status, and control information in the Type 1 and Type 4 Channel Adapters. (Not all values of X are used for both types of CA.) Refer to Appendix B for the definitions of the bits within the input and output instructions.

Input Instructions

Eight input instructions are assigned to the Type 1 Channel Adapter to monitor its operation and data flow; twelve are assigned to the Type 4 CA. Appendix B defines the bits within each input instruction.

Input X'60' (Initial Selection Control): This instruction loads the contents of the initial selection control register into the general register specified by R. The bits of the control register are set as a result of initial selection or system reset and reflect the status of the operation when completed.

This should normally be the first instruction executed after determining that the level 3 interrupt was caused by a channel adapter initial selection or a system reset.

Input X'61' (Initial Selection Address and I/O Command Byte): This instruction loads the initial selection address and the I/O command into byte 0 and byte 1 respectively of the general register specified by R.

The control program should normally execute an Input X'61' instruction when servicing a CA initial L3 interrupt request. If the cause of the interrupt (identified by executing an Input X'60') is found to be an initial selection sequence, the addressed subchannel and channel I/O command byte can be determined by executing an Input X'61' instruction.

Input X'62' (Data/Status Control): This instruction loads the contents of the CA data/status control register into the general register specified by R. An Input X'62' should normally be the first instruction executed by the control program when servicing a CA data/status L3 interrupt. It is used to determine the cause of the interrupt.

Input X'63' (Transfer Address and ESC Status Bytes): This instruction loads byte 0 and byte 1 of the general register specified by R with the I/O device address byte and ESC status byte respectively. These are the address byte and status byte given to the channel when the last Output X'63' was executed. This instruction can be executed for checking purposes immediately after Output X'63' is executed. When servicing a CA data/status L3 interrupt request due to a transfer sequence, the program can execute this instruction either for checking purposes or to obtain the information if not retained elsewhere.

Input X'64' (Data Buffer Bytes 1 and 2): This instruction loads the contents of data buffer bytes 1 and 2 into bytes 0 and 1 of the general register specified by R. The control program normally executes the Input X'64' instruction when servicing a CA data/status L3 interrupt caused by the ending of an inbound data transfer sequence in which one or more data bytes were transferred. (For a Type 4 CA this instruction is used when the CA is not in extended-buffer mode.)

Programming Note
Input X'62' should be executed before the Input X'64' instruction to determine the transferred byte count. Data buffer 1 contains valid information if the transfer count is greater than zero. Data buffer 2 contains valid information if the transfer count is two or more.

Input X'65' (Data Buffer Bytes 3 and 4): This instruction loads the contents of data buffer bytes 3 and 4 into bytes 0 and 1 of the general register specified by R. The control program normally executes the Input X'65' instruction when servicing a CA data/status L3 interrupt caused by the ending of an inbound data transfer sequence in which three or four data bytes were transferred. (For a Type 4 CA this instruction is used when the CA is not in extended buffer mode.)

Programming Note
Input X'62' should be executed before the Input X'65' instruction to determine the transferred byte count. Data buffer 3 contains valid information if the transfer count is three or four. Data buffer 4 contains valid information if the transfer count is four.

Input X'66' (NSC Status Byte): This instruction loads the contents of the NSC status byte register into bytes 0 and 1 of the general register specified by R. These bits reflect the status bits loaded into the NSC status byte register when an Output X'66' instruction is executed. These bits are reset either when the channel accepts an NSC status byte presentation or when the control program executes an Output X'67' instruction with byte 1, bit 3 or byte 0, bit 4 set to one.

Programming Note
Reset of this instruction by the control program (output X'67' byte 0, bit 4) should be only as a diagnostic aid and should not be used during active communication over the channel.

Input X'67' (CA Controls): This instruction loads a general register with the NSC address byte and the state of various check and control latches.

The control program should execute this instruction when (1) an asynchronous status sequence is required (determined by the control program and initiated by executing an Output X'67' with byte 1 bit 1 on) or (2) there is a CA L1 interrupt request and the control program wants to determine the cause of the interrupt.

This instruction can be used to determine which Type 4 CAs are selected, as follows:

Byte 0, bits 6-7:00—First Type 4 CA (CA-1) is selected.
01—Second Type 4 CA (CA-2) is selected.
10—Third Type 4 CA (CA-3) is selected.
11—Fourth Type 4 CA (CA-4) is selected.

Input X'6C' (EB/Cycle Steal Mode Control Register): This instruction loads the content of the CA control character recognition latches, the EB and cycle steal mode control bits and the transferred byte count into the general register specified by R.

Input X'6D' (EB/Cycle Steal Mode Data Buffer): This instruction loads the content of the two-byte EB mode buffer into the general register specified by R. The first (even) data byte is placed in byte 0 of the general register; the second (odd) data byte is placed in byte 1.

Input X'6E' (Cycle Steal Mode Error Registor and CSAR Byte X) (Type 4 CA Only): This instruction loads the contents of the cycle steal error register and byte X of the CSAR into the general register specified by R.

Input X'6F' (Cycle Steal Mode CSAR Bytes 0 and 1) (Type 4 CA Only): This instruction loads the 16 low order bits of the cycle steal address from the CSAR (bytes 0 and 1) into the register specified by R.

Output Instructions
Seven output instructions are assigned to the Type 1 channel Adapter to control its operation and data flow; eleven are assigned to the Type 4 CA. Appendix B defines the bits within each output instruction.

Programming Note
If the control program executes an Output X'61' instruction, (an assigned, but unused instruction) the hardware takes no action unless execution occurs during a data/status transfer. During data/status transfer, the hardware sets the in/out instruction accept check and causes a CA level 1 interrupt request.

Output X'60' (Reset Initial Selection): When this instruction is executed, the hardware resets both the initial selection hardware latches and the CA L3 interrupt request resulting from an initial selection sequence. This output

does not reset a system reset condition. See Output X'67' to reset a system reset. Since this instruction performs a function instead of an operation, the bit settings of the register are ignored.

Output X'62' (Data/Status Control): This instruction sets the data /status control register according to the contents of bytes 0 and 1 of the general register specified by R. This instruction, if bit 0.7 is 1, resets EB/cycle steal control mode.

Output X'63' (Transfer Address and ESC Status Bytes): This instruction loads the transfer address and ESC status registers with the contents of byte 0 and 1 respectively of the general register specified by R.

This instruction should be executed before signaling the CA that a data/status sequence is required. The I/O device address provided by the last Output X'63' executed is presented to the channel in all subsequent transfer sequences. The Output X'63' instruction must be executed each time a transfer sequence is required for a different I/O device address. This instruction must also be executed before signaling the channel adapter that an ESC final status transfer is required. This presents the I/O device address in addition to the status byte to the host channel.

Programming Note

For compatibility, the program should ensure that the bits of the ESC status byte that are set are consistent with the bits set under similar conditions in the operation of the IBM 2701/2702/2703 transmission control units.

Output X'64' (Data Buffer Bytes 1 and 2): This instruction loads data buffer bytes 1 and 2 with the contents of the general register specified by R. This instruction should be executed before signaling the CA that an outbound data transfer sequence is required. When an outbound data transfer sequence occurs, data buffer bytes 1 and 2 are the first and second data bytes transferred. (For a Type 4 CA this instruction is used when the CA is not in extended-buffer or cycle-steal mode.)

Programming Note

The request byte count (Output X'62', byte a, bits 6-7) must be set with the total number of valid data bytes loaded into data buffers 1-4 (by Outputs X'64' and X'65') to ensure data integrity.

Output X'65' (Data Buffer Bytes 3 and 4): This instruction loads data buffer bytes 3 and 4 with the contents of the general register specified by R. This instruction should be executed before signaling the CA that an outbound data transfer sequence is required. When an outbound data transfer sequence occurs, data buffer bytes 3 and 4 are the third and fourth data bytes transferred. (For a Type 4 CA this instruction is used when the CA is not in extended-buffer or cycle-steal mode.)

Programming Note

The request byte count (Output X'62', byte 1, bits 6-7) nust be set with the total numbcr of valid data bytes loaded into data buffers 1-4 (by Outputs X'64' and X'65') to ensure data integrity.

Output X'66' (NSC Status Byte): This instruction sets bits in the NSC status register according to the contents of the general register specified by R. The Output X'66' instruction should be executed before signaling the CA that an NSC final status transfer sequence is required.

When the NSC final status transfer sequence occurs, the status byte provided by this output is presented to the channel. If the status byte has previously been given to the channel adapter (but was stacked by the channel), it need not be given again. This output may be used to present an asynchronous status (for example, Attention) or the final status, ending a channel I/O command in the native mode.

For Type 4 CA only: By executing an Output X'66' instruction in which bit 0.4 is 1 (after requesting and receiving a Type 4 CA program interrupt), the Type 4 CA will respond with a 'busy' status (X'10') to complete initial selection sequence and will not interrupt the control program. This status is presented at the end of a complete normal initial selection sequence. The control program must end this 'long busy' state by requesting and receiving a program interrupt and present 'device end' status via an NSC final status transfer sequence.

Inhibition of level 3 interrupts does not occur in the case of a system reset, an initial selection interface disconnect, or an initial selection selective reset condition. In these cases the Type 4 CA does request a level 3 interrupt.

Programming Note

For compatibility, the control program should ensure that the bits of the NSC status byte that are set are consistent with the bits set under similar conditions in the operation of the Type 2 Channel Adapter.

Output X'67' (CA Controls): This instruction causes various control latches to be set or reset in the channel adapter according to the bits in the general register specified by R.

If a 3705 is equipped with from two to four Type 4 CAs, the control program uses this instruction to designate which of the CAs is to be selected. Bits 5, 6, and 7 of byte 0 are used for this purpose, as follows:

Bit 5: 0 - Leave the currently selected CA active.
1 - Select the CA indicated by bits 6-7.

Bits 6-7: 00 - First CA (CA-1)
01 - Second CA (CA-2)
10 - Third CA (CA-3)
11 - Fourth CA (CA-4)

Other functions specified by bit settings in the Output X'67' instruction apply to the CA selected in accordance with the value of bits 5, 6, and 7 above.

Output X'67' may also be executed to set a program-requested interrupt in a specific one of the multiple CAs, without regard for whether that CA is the currently selected one. Bits 3, 6, and 7 of byte 0 of the instruction are used for this purpose, thus:

Bit 3: 1 - Execute instruction for CA indicated by bits 6-7
Bits 6-7: 00 - First CA (CA-1)
01 - Second CA (CA-2)
10 - Third CA (CA-3)
11 - Fourth CA (CA-4)

Other functions specified by bit settings in the Output X'67' instruction apply to the CA specified, regardless of whether it or another CA is currently selected. Whichever one is selected remains so.

Programming Notes:
(1) Bits 3 and 5 of byte 0 of an Output X'67' instruction must never both be 1. (2) The CA Diagnostic Reset (byte 0, bit 4) resets the channel adapter only if both interface A and interface B are disabled.

Output X'6C' (EB/Cycle Steal Mode Control Register): This instruction sets the control character recognition latches, the EB and cycle steal mode control bits and the byte count bits of the Type 4 CA from the corresponding bits of the general register specified by R.

Output X'6D' (EB Mode Data Register): This instruction loads two data bytes from the register specified by R into the Type 4 CA EB mode/cycle steal mode data buffer. The first data byte (byte 0) of the general register is placed in the first (even) byte of the buffer; the second data byte (byte 1) of the register is placed in the second (odd) byte of the buffer.

Output X'6E' (CSAR Byte X) (Type 4 CA Only): This instruction sets the extended address bits of CSAR byte X from the general register specified by R.

Programming Note
Before this instruction is executed, an Output X'6F' instruction must be executed to set CSAR bytes 0 and 1 and reset CSAR byte X.

Output X'6F' (Cycle Steal Mode CSAR Bytes 0 and 1) (Type 4 CA Only): This instruction sets into CSAR bytes 0 and 1 the storage address of the first data buffer byte involved in a cycle steal data transfer. The address is updated to the next sequential storage halfword address when the cycle steal data transfer ends. This instruction also resets CSAR byte X to X'0'. (Resetting byte X allows the control program to set the storage address in the CSAR using only the Output X'6F' instruction if the storage address is not greater than 64K.

Error Indications

The programmer should decide what specific action to take in attempting to recover from an error condition. The various ways to handle errors depend on the application and installation.

The following indications require error recovery procedures.

Channel Bus In Check
When the CA hardware detects bad parity in the byte to be sent across the I/O Channel Interface, it generates good parity for that byte and gates it onto the 'I/O channel interface' bus. The hardware than causes a CA level 1 interrupt. The control program should interrogate the condition register by executing an Input X'67' and record the error conditions that occurred. The control program should then reset the level 1 interrupt and end the command by presenting a CE, DE, UC status.

Channel Bus Out Check in EB Mode: If a bus out check occurs on an inbound data transfer sequence in EB mode, bad parity may have been written into the EB mode local store. The control program must re-establish good parity by executing successive Output X'6D' instructions as described in this chapter under *Extended-Buffer Mode Local Store (Type 4 CA Only).* Failure to do so may cause a local store parity check level 1 interrupt to occur when the local store is next accessed.

In/Out Instruction Accept Check
An in/out instruction accept check is set when the control program executes an Input or Output X'60', X'61', X'62', X'63', X'64', X'65', or X'66' instruction when the CA is in the process of handling any data/status transfer sequence. A level 1 interrupt request is also set, and the instruction is prohibited from setting any hardware control latches. The control program should interrogate the condition register by executing an Input X'67' and record the error indication. An Output X'67' should be issued to reset the L1 interrupt request and the 'in/out instruction accept check' latch.

I/O Check on Input or Output X'6D' Instruction in EB Mode: If an I/O check occurs during execution of an Input or Output X'6D' instruction while the CA is in EB mode, the entire data transfer sequence must be re-executed. It is not sufficient simply to re-execute the instruction on which the error occurred. If the error occurred on an outbound sequence, the Output X'6C' instruction must be re-executed and the EB mode local store re-loaded from the beginning with successive Output X'6D' instructions.

If the error occurred on an inbound sequence, the Input X'6C' instruction must be re-executed and the EB mode local store re-accessed from the beginning with successive Input X'6D' instructions.

CCU Outbus Check
When the CA hardware detects bad parity on the CCU Outbus, it sets the 'CCU Outbus check' latch, causes a L1 interrupt, and prohibits reselection on the channel interface. The control program should interrogate the condition register by executing an Input X'67' and record the error indication. The control program should then issue an Output X'67' to reset the L1 interrupt and the 'CCU Outbus check' latches. If the CA was active on the channel in a data/status state when the error occurred, the hardware terminates the transfer and causes a CA data/status L3 interrupt request. The control program must reissue the output instructions to allow reselection to a channel interface.

CCU Out Bus Check on Output X'6D' Instruction in EB Mode: If a CCU Out Bus Check level 1 interrupt occurs on an Output X'6D' instruction when the CA is in EB mode, the entire data transfer sequence must be re-executed. It is not sufficient simply to re-execute the instruction on which the error occurred. The Output X'6C' instruction must be re-executed and the EB mode local store reloaded from the beginning with successive Output X'6D' instructions.

Local Store Parity Check
When the hardware detects bad parity on data bytes being gated out of local store registers, it causes a level 1 interrupt. The control program should interrogate the condition register by executing an Input X'67' and record the error indication. The control program should then issue an Output X'67' to reset the L1 interrupt request and end the command by presenting CE, DE, UC status and equipment check sense.

Chapter 10: Type 2 and Type 3 Channel Adapters

This chapter describes the basic operation of the Type 2 and Type 3 Channel Adapters and the requirements necessary to program these adapters.

The Type 2 Channel Adapter (Type 2 CA) and the Type 3 Channel Adapter (Type 3 CA) are high-performance, cycle-stealing adapters that support instantaneous channel data transfer rates of up to 276 kilobytes per second.

The Type 2 and Type 3 CAs are minimally dependent on the control program. Data transfer and control word chaining are handled without control program intervention. The Type 2 or Type 3 CA notifies the control program when a data transfer is complete with an "I/O interrupt".

The Type 3 CA has all the capabilities of the Type 2 CA, and appears to the 3705 control program as a Type 2 CA. In addition the Type 3 CA enables the 3705 to be attached to tightly-coupled multiprocessors as a symmetrically shared I/O unit. This means that the 3705 can be attached to two CPUs of a multiprocessor through one Type 3 Channel Adapter. The 3705 appears as the same I/O unit to each processor, and can be sequentially accessed in exactly the same manner by each processor. This feature allows the CPU access methods for the 3705 to run in either CPU without having to perform a "shoulder-tap" interrupt to the alternate CPU in order to perform an I/O operation to the 3705. The Type 3 CA can also provide an alternate path capability for uniprocessors.

Both channel interfaces of the Type 3 CA can be concurrently enabled, but concurrent data transfer is not permitted.

Because the Type 2 and Type 3 CAs are similar in operation, only the differences are identified as pertaining to the Type 2 CA or Type 3 CA. Otherwise, the term *channel adapter* or CA refers to both the Type 2 and Type 3 CA.

Operation and Data Flow

A host processor channel command is received by the CA, decoded, and placed into the command register. If the operation is a data transfer type (Read or Write), the CA checks the validity of the control word (CW) address contained in the inbound or outbound CWAR (control word address register). (See the *Channel Adapter Control Word* section in this chapter.) A valid control word address should have previously been placed into the CWARs by an output instruction from the control program.

If the address in the appropriate CWAR is not valid, Unit Exception initial status is returned to the channel, and no data transfer is attempted. If the CWAR is valid, a cycle-steal operation places the information from the first halfword of the CW into the CA. The information from this cycle-steal operation loads the command and flag fields of the CW into the CW command/flag registers and loads the count register. In addition, the first two bits (four bits for 3705 Models J–L) of the starting address of the storage area where data is to be read from, or written to, are placed into the cycle-steal address register (CSAR). Another cycle steal operation places the information from the second (and final) halfword of the CW into the CA. The second halfword, containing the remainder of the starting data address, is placed into the CSAR.

For 3705-to-channel data transfer, a halfword is transferred via cycle steal from storage to the data 1 and data 2 registers and then sent to the channel, a byte at a time.

For channel-to-3705 data transfer, a byte at a time is received from the channel and alternately loaded into the data 1 and data 2 registers. The contents of both registers (one halfword total) are then transferred to storage via a cycle steal using the CSAR address.

Each byte tranferred to or from the channel causes the count register to be decremented by one. Each halfword transferred to or from storage causes CSAR to be incremented by two in order to address the next halfword storage location.

When the count register is equal to 0, the data transfer for that CW is complete, and the next sequential CW is transferred to the CA if CW chaining is indicated. Otherwise, the operation ends by causing a level 3 interrupt after presentation of CE status.

On the byte-multiplexer channel, the CA disconnects from the host processor channel after two bytes have been transferred in burst mode across the channel. After a CA-to-storage cycle-steal operation, the CA reconnects to the channel to transfer another two bytes.

On selector and block-multiplexer channels, the total data transfer, from Initial Selection to Channel End status, is in burst mode.

Note: *The channel adapter should not be on line if the controller is in a program stop state. The code necessary to handle adapter interrupts is not running when in this state and any interrogation of the adapter across the channel interface will receive Busy if an interrupt request is present.*

Cycle Steal Operation

To relieve the system control program of the responsibility of transferring data and information between the channel adapter and storage, the CA uses cycle steal. Under hardware control, the CA "steals" machine cycles from the Central Control Unit. Cycle steal allows overlap of channel operations with control operations. When the channel adapter needs data from storage or has data to be stored, it requests a cycle steal from the CCU. A CA cycle-steal request has the highest priority in the controller. Therefore, the CCU, at the end of the current machine cycle, permits the CA cycle-steal request to be serviced. Two bytes of information are transferred into or out of storage during each cycle steal operation.

Channel Adapter States

Because of the problems associated with the handling of two asynchronous communications—the Central Control Unit communication and the host processor channel interface—the CA must be in a certain state with respect to one before access is allowed from the other.

A thorough understanding of these states is required to write or modify a CA control program or a host processor access method. More than one of these states may be present at the same time.

- CA Active State - The channel adapter is in the process of transferring data or information across the host processor channel. The active state exists from the time the CA accepts a channel command during initial selection until the channel accepts Device End status for that command.
- CA Level 3 Interrupt State - This state may have been initiated by the control program or by the completion of either a control word or a channel command. If the CA *is not* in the active state, the control program can gain access to all CA registers except the channel sense and status registers. If the CA *is* in the active state, all registers are available to the control program. See Output X'57' in Appendix B for an additional restriction on the channel adapter mode register.
- CA Level 1 Interrupt State - The channel adapter enters this state only when an error condition is detected during the execution of an input or output instruction directed at the CA, during a cycle steal operation, or during transfer of information across the channel interface. If the channel adapter is executing a channel command when a hardware detected error occurs, the command is ended with a hardware generated Channel End and/or Device End, and Unit Check status. A level 1 interrupt is requested by the adapter when the host processor accepts the ending status.
- CA Busy State - This state refers to the 'busy' status generation independent of the adapter's status register. This state exists when the CA is both active and engaged in an L1 or L3 interrupt and the channel attempts an initial selection sequence.
- Diagnostic Wrap State - This state is for diagnostic purposes and is entered when the control program executes an Output X'57' instruction with byte 1, bit 7 set to 1. In the diagnostic wrap state, the CA is forced to an offline status regardless of the position of the control panel Enable/Disable switch. All CA registers, including the IPL portion of Output X'57', are available to the control program to be used for test functions. Output instructions X'58' and X'5B' can be used to simulate the channel interface lines. The diagnostic wrap state remains in effect until Output X'57' is executed with byte 1, bit 7 off (0).
- Hard Stop State - This state is entered when the 'hard stop' latch is set in the Central Control Unit. The hard stop state causes the adapter to go offline, but the channel enable light on the control panel remains *on*. The channel adapter attempts to complete execution of any outstanding channel command by presenting CE-DE-UC, or DE-UC ending status. If the 3705 hard stops while the CA is active with a level 1 or level 3 interrupt request set, the hardware generated status will not be presented if the channel had 'suppress out' up. With a Type 3 CA, any initial selection attempt by the opposite channel receives a Busy initial status. Once 'suppress out' falls, the adapter raises 'request in' to present status, generated because of hard stop, to the interface over which data transfer was taking place, and goes offline when the channel accepts the status.

  Test I/O loops, to clear suppressible status, receive a continuous Busy if the 3705 has hard stopped with the CA in the active state with an interrupt pending. Once a 3705 hard stop occurs, the adapter goes offline as soon as the using channel accepts ending status for an outstanding channel command. If there is a pending Device End due to a previous Busy status offered to the opposite channel (Type 3 CA), it will be presented to that channel. When that channel accepts Device End status, the adapter goes offline to it also.

Channel Adapter Registers

The CA contains 13 external registers that are used by the control program for normal operations. Input/output instructions (X'50' to X'5F').

are used to gain access to these registers. See Appendix B for I/O instruction bit position assigments.

Channel Adapter Register Restrictions (Type 2 and 3 CAs)
The Type 2 and Type 3 channel adapter registers can be accessed only when the CA is selected and (1) a level 1 or 3 interrupt request is set, or (2) the CA is in diagnostic wrap mode. An input/output instruction issued to a Type 2 or a Type 3 CA under any other condition causes an I/O check.

Inbound Data Control Word Address Register (INCWAR)
The INCWAR (inbound data control word address register) contains the storage address of the control word (CW) to be fetched by the CA cycle-steal hardware when a channel Write, Write Break, or Write IPL command is being executed.

The control program can load this register with an Output X'50' instruction or use it as input by executing an Input X'50' instruction. The CA recognizes this input/output instruction only if channel adapter register restrictions are met. Refer to "Channel Adapter Register Restrictions (Type 2 and 3 CAs)" earlier in this chapter.

The address in INCWAR is incremented by 4 (bytes) each time a CW fetch is executed by the CA cycle-steal hardware.

Programming Note
All CWs must begin on a halfword boundary and reside in the lower 64K bytes of storage. Execution of a CW chaining operation or a TIC (transfer in channel) control word to an address above 64K causes a CW error condition resulting in a CA level 1 interrupt with register X'56', byte 0, bit 0 set to 1.

Outbound Data Control Word Address Register (OUTCWAR)
The OUTCWAR (outbound data control word address register) contains the storage address of the control word (CW) to be fetched by the CA cycle-steal hardware when a channel Read command is being executed.

The control program can load this register with an Output X'51' instruction or use it as input by executing an Input X'51' instruction. The CA recognizes this input/output instruction only if channel adapter register restrictions are met. Refer to "Channel Adapter Register Restrictions (Type 2 and 3 CAs)" earlier in this chapter.

The address in OUTCWAR is incremented by 4 (bytes) each time a CW fetch is executed by the CA cycle-steal hardware.

Programming Note
All CWs must begin on a halfword boundary and reside in the lower 64K bytes of storage. Execution of a CW chaining operation or a TIC (transfer in channel) control word to an address above 64K causes a CW error condition resulting in a CA level 1 interrupt with register X'56', byte 0, bit 0 set to 1.

Control Word Byte Count Register (CWCNTR)
At the completion of a control word fetch operation, the byte count register (CWCNTR) contains the value of the byte count that was loaded from the control word just fetched. As each byte is transferred across the channel interface, the CWCNTR is decremented by 1. When the count reaches zero, either CW chaining or a CA level 3 interrupt is initiated, depending upon the state of the chain flag and zero count override flag of the control word just ended.

The count contained in CWCNTR is precise and should be used by the control program to determine the location of the end of data in storage when a channel data transfer is complete.

The contents of CWCNTR are available to the control program by executing an Input X'52' instruction (control word byte count). The Input X'52' instruction can be recognized by the CA only if channel adapter register restrictions are met. Refer to "Channel Adapter Register Restrictions (Type 2 and 3 CAs)" earlier in this chapter.

Channel Adapter Sense Register (CASNSR)
Byte 0 of the CA sense register (CASNSR) provides data for the channel Sense command, and byte 1 provides CSAR byte X data for 3705-II Models J–L only. Byte 0 of the CASNSR conforms to the System/370 standard definition of sense bits 0 through 4. Bits 6 and 7, however, are unique to the 3705. All bits can be used as input to the control program by an Input X'53' instruction (sense register). With the exception of byte X in 3705 Models J–L, an Input X'53' instruction loads zeroes into the specified register and an Output X'53' instruction is ignored if the selected channel adapter is inactive or not in the diagnostic wrap state. Byte X data can be accessed with the channel adapter in the inactive state but CA register restrictions must be met. Refer to "Channel Adapter Register Restrictions (Type 2 and 3 CAs)" earlier in this chapter. CSAR byte X data is not available for output.

Programming Note
The setting of any CASNSR bit causes the Unit Check bit to be set in the CA status register and thus causes the termination of any data transfer that may have been in progress. CASNSR, with the exception of the not-initialized bit (bit 6), is reset during initial selection whenever the CA accepts a command other than Sense, Test I/O, or No-Op.

Channel Adapter Status Register (CASTR)
The channel adapter status register (CASTR) contains the standard System/370 status byte. The control program can load this register by executing an Output X'54' instruction (set status register bits) and can examine the register by executing an Input X'54' instruction (status register). This input/output instruction is recognized by the CA only if channel adapter register restrictions are met. Refer to "Channel Adapter Register Restrictions (Type 2 and 3 CAs) earlier in this chapter. An Input X'54' instruction loads zeroes into the specified register and an Output X'54' is ignored if the selected channel adapter is inactive or not in the diagnostic wrap state.

Channel Adapter Control Register (CACR)
The channel adapter control register (CACR) is a collection of control latches to be used by the control program when initiating or terminating a CA operation. The control program can set three of the latches in this register with an Output X'55' instruction (set control register bits) and can use it as input by executing an Input X'55' instruction (control register). These input/output instructions are recognized by the CA only if channel adapter register restrictions are met. Refer to "Channel Adapter Register Restrictions (Type 2 and 3 CAs)" earlier in this chapter.

Channel Adapter Check Register (CACHKR)
The channel adapter check register (CACHKR) is a collection of latches that cause the level 1 CA check interrupt request to be set. By examining this register, the level 1 interrupt program can determine what caused the CA level 1 interrupt. All of the latches in this register are automatically reset when an Output X'57' instruction is executed to reset the L1 interrupt request. An exception to this is the bus out check that is reset when a channel command other than Sense, TIO, or No-Op is accepted by the adapter. The control program can use this register as input by executing an Input X'56' instruction (check register). This input/output instruction can be recognized only if channel adapter register restrictions are met. Refer to "Channel Adapter Register Restrictions (Type 2 and 3 CAs)" earlier in this chapter.

Channel Adapter Mode Register (CAMR)
The channel adapter mode register (CAMR) can be loaded by the control program via Output X'57' (channel adapter mode register). Refer to "Output X'57' (Channel Adapter Mode Register–CAMR)" in Appendix B for more details.

Channel Bus Out Diagnostic Register (CBODR)
The primary function of the channel bus out diagnostic register (CBODR) is to simulate the channel interface 'bus out' when the CA is in the diagnostic wrap mode. The control program can load this register by executing an Output X'58' instruction (channel bus out diagnostic register) and can use it as input by executing an Input X'58' instruction. Byte 0, bits 0-7 and byte 1, bit 0 of this register are accessible only when the CA is selected and in the diagnostic wrap mode. Byte 1, bits 1-7 are accessible following the setting of a CA level 1 or level 3 interrupt request or when the selected CA is in diagnostic wrap mode.

Cycle Steal Address Register (CSAR)
This register is the interface to the 'cycle steal address bus'. It contains the current data address while data transfer is in progress. With each data halfword (two bytes) transferred to and from the channel, this address increases by two. The register is initially loaded with the control word (CW) address at the beginning of a CW-fetch operation and then is loaded with the starting data address when the CW fetch is complete.

The control program can use this register as input by executing an Input X'59' instruction. This input instruction is recognized only if channel adapter register restrictions are met. Refer to "Channel Adapter Register Restrictions (Type 2 and 3 CAs)" earlier in this chapter. The CSAR is not available for output.

Channel Adapter Data Buffer (CADB)
The channel adapter data buffer register (CADB) forms the CA buffer for all channel data being transferred through the CA for either normal or diagnostic operations. This register physically shares a local store array with the INCWAR and OUTCWAR. The control program can load this register or use it as input by executing an Output or Input X'5A' instruction. The control program should ensure good parity in this register by executing an Output X'5A' instruction before attempting an Input X'5A' instruction. This input/output instruction can be recognized only if channel adapter restrictions are met. Refer to "Channel Adapter Register Restrictions (Type 2 and 3 CAs)" earlier in this chapter.

Channel Tag Diagnostic Register (CTDR)
The channel tag diagnostic register (CTDR) contains two bytes used to simulate 'tag out' and interrogate 'tag in' signals for diagnostic purposes. The control program can load byte 0 of this register with an Output X'5B' instruction, and it can use the entire register as input by executing an Input X'5B' instruction. This register is accessible only if the selected CA is in the diagnostic wrap mode.

Channel Adapter Command Register (CMDR)
The CA command register (CMDR) indicates the current channel command being executed by the CA. It also indicates the current or last control word executed.

The control program can use this register as input by executing an Input X'5C' (command register) instruction. The CMDR is not available for output. This input instruction is recognized only if channel adapter register restrictions are met. Refer to "Channel Adapter Register Restrictions (Type 2 and 3 CAs)" earlier in this chapter.

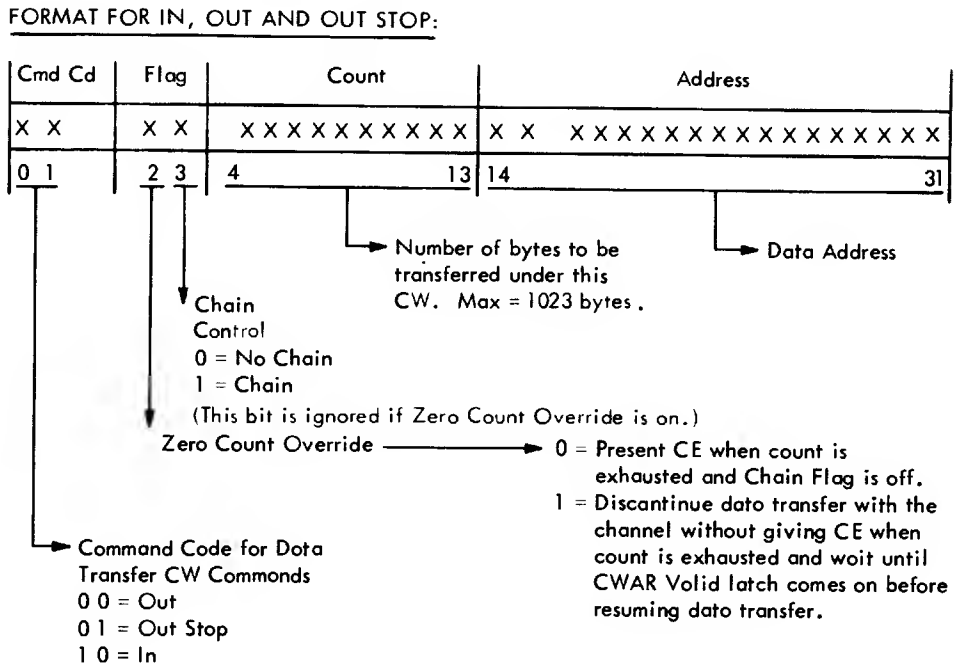
Channel Adapter Control Word

The channel adapter control word (CW) specifies the operation to be performed by the CA in conjunction with a host processor channel operation. Control words are built by the control program according to the operation to be performed and are model dependent. See Figure 10-1 and 10-2 for Type 2 and Type 3 Channel Adapter Control Words.

The following paragraphs describe the various fields of the CA control word.

Command Code: Bits 0-1 (bits 8-9 for 3705, Models J–L) specify the operation to be performed. See *Control Word Command Codes* in this chapter.

Zero Count Override: Bit 2 (bit 10 for 3705, Models J–L) is used with the command chain flag to determine what action the CA should perform when the current CW count



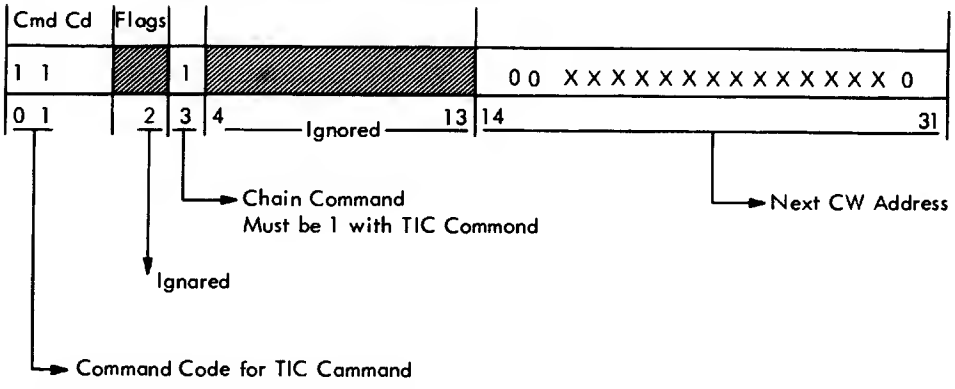
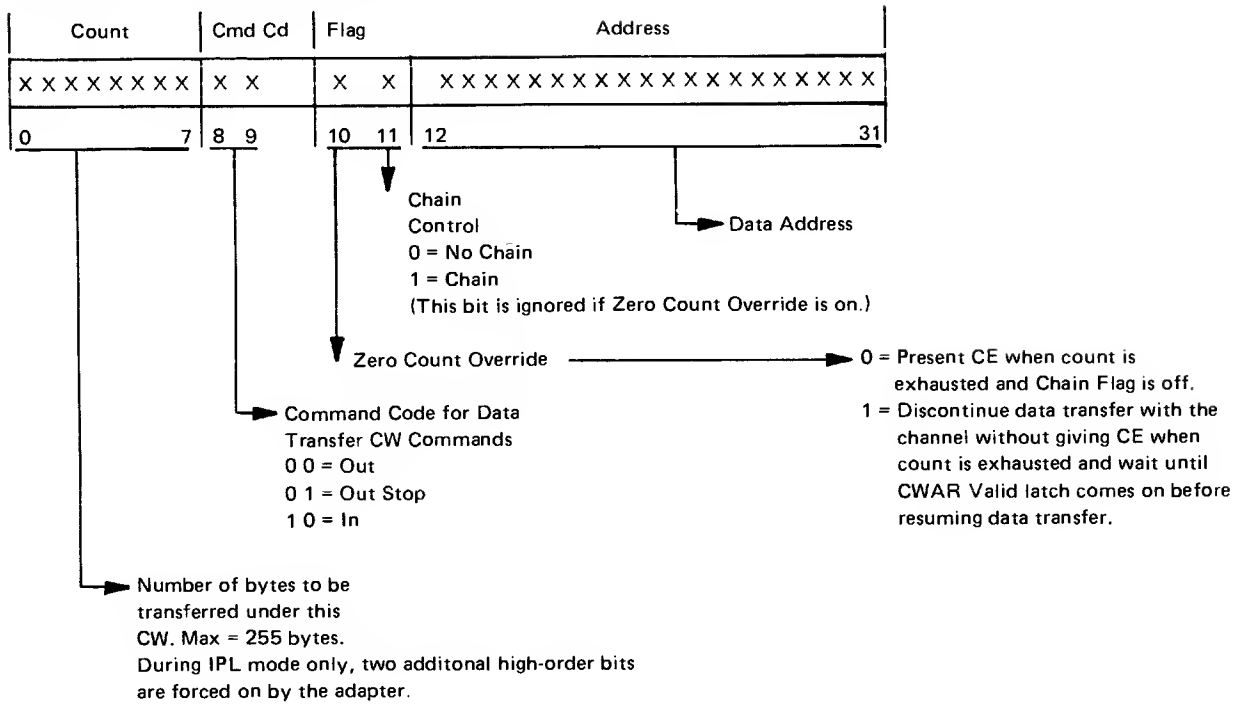


Figure 10-1. Type 2 and Type 3 Channel Adapter Control Word (Not applicable to 3705, Models J–L)

FORMAT FOR IN, OUT AND OUT STOP:



FORMAT FOR TRANSFER IN CHANNEL (TIC):

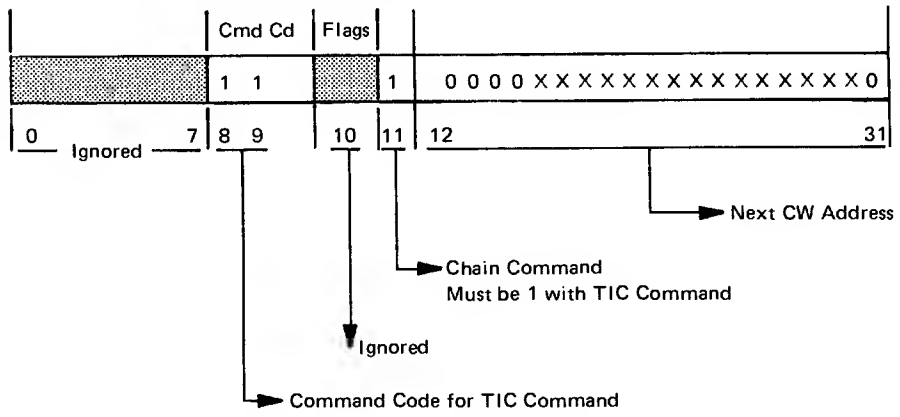


Figure 10-2. Type 2 and Type 3 Channel Adapter Control Word (3705 Models J L only)

is exhausted. When this bit is on, the CA requests a level 3 interrupt and discounts from the byte-multiplexer channel without giving Channel End or remains connected to the burst channels without giving Channel End. The CA resumes data transfer when an Output X'57' instruction is executed to reset the channel adapter's level 3 interrupt request. The purpose of this flag is to allow the CA to transfer multiple buffers under a single host processor channel command with a minimum assignment of buffers to the CA.

Chain Flag: Bit 3 (bit 11 for 3705, Models J–L) can cause multiple CWs to be used for one operation. When this bit is on, the appropriate 'CWAR valid' latch remains set during the CW-fetch operation. When the CW count reaches 0 while the CA is executing a Read, Write, Write Break, or Write IPL channel command, control word chaining to the next sequential CW occurs automatically. This bit must be on for a TIC (transfer in channel) control word.

Count: Bits 4-13 (bit 0-7 for 3705, Models J–L) specify the number of bytes to be transferred across the channel interface by the CW. The maximum count is 1023 bytes (255 bytes for 3705-II, Models J–L). This field is ignored for TIC control words.

Data Address: Bits 14-31 (bits 12-31 for 3705, Models J–L) contain the starting storage address for a read or a write operation, depending on the control word. For a TIC control word, this field contatins the address of the next CW to be executed.

Control Word Command Codes

The following four CW commands are recognized by the CA. The first three are operational and indicate the direction of data movement between the controller and the host processor. The fourth is used for chaining control words.

Out (B'00'): This control word command is used to control data transfer from the communications controller to the host processor via a channel Read command. If the count register decrements to 0, the zero count override flag is not on, and CW chaining is indicated, the CA immediately chains to the next CW without ending the channel command. If CW chaining is not indicated and the zero count override bit is not on, the current channel command is ended with CE status, and a level 3 interrupt request is set. If the zero count override bit is on, a level 3 interrupt is requested without presenting any status to the channel. If both zero count override and CW chaining are on, a level 3 interrupt is requested and the chaining indication is ignored.

Out Stop (B'01'): This control word command is also used to control data transfer from the communications controller to the channel. If the count register decrements to 0, the zero count override flag is not on, and CW chaining is indicated, the current channel command ends immediately with CE, DE. A level 3 interrupt is *not* requested. If CW chaining is not indicated and the zero count override flag is on, the current channel command is ended with CE status, and a level 3 interrupt is requested. If both zero count override and CW chaining are on, a level 3 interrupt is requested before chaining is executed.

In (B'10'): This control word command is used to control data transfer from the channel to the communications controller. If the count register reaches 0, the zero count override flag is not on, and CW chaining is indicated, the CA chains immediately to the next CW without ending the channel command. If CW chaining is not indicated and the zero count override bit is not on, a level 3 interrupt request is set after the current channel command is ended with Channel End status. If the zero count override bit is on, a level 3 interrupt is requested without presenting any status to the channel. If both zero count override and CW chaining are on, a level 3 interrupt is requested and the chaining indication is ignored.

TIC (B'11'): The Transfer-In-Channel control word causes the CA cycle-steal hardware to load the address field of the CW into the appropriate CWAR. This causes a transfer to another string of CWs. The CA must complete another CW fetch request before resuming data transfer across the channel interface. The zero count override flag is ignored for a TIC command.

Control Word Conventions

All control words must reside in the lower 64K bytes of storage. CW chaining or a TIC (transfer in channel) to an address above 64K causes a CW error condition resulting in a CA level 1 interrupt with register X'56', byte 0, bit 0 set on.

The data address portion of the control word can specify an odd or even address. If an odd address is specified by an Out or Out Stop control word, the data transferred to the host begins with the second byte of the halfword. If an odd address is specified by an In control word, the first byte from the host is stored in the second byte of the target halfword; the first byte remains unchanged.

The address specified by the address field of a TIC control word must be even.

The control word names include "In" or "Out" to denote the direction of data transfer with respect to the communications controller. Thus an In control word must be coupled with a channel Write, Write Break, or Write IPL command, and the Out and Out Stop CWs must be coupled with a channel Read command.

Channel Adapter Interrupt Requests

The CA has two interrupt requests assigned to it: a check interrupt request at level 1, and a normal service interrupt request at level 3. All programming operations for the CA are performed in these two interrupt levels with the use of input/output instructions.

A level 1 interrupt request is caused when a CA hardware or program error is detected. The error condition is set in the channel adapter check register. This register is available to the control program via an Input

X'56' instruction, and error recovery may then be attempted.

A level 3 interrupt request occurs whenever the channel adapter requires service. Any of the following conditions cause a level 3 interrupt.

1. The In, Out, or Out Stop control word being executed has ended because the data count has decremented to zero and CW chaining is not indicated.
2. An In, Out, or Out Stop control word is being executed, the count has decremented to zero, and the zero count override flag is on.
3. All zeros initial status is accepted during executon of a Write IPL command.
4. The CA is in the active state, not initialized, no status is pending or stacked, and a program requested interrupt is generated.
5. The CA is in the inactive state, chaining is not indicated, or there is no stacked or pending status, and one of the following occurred:
   a. The 'program level 3 request' latch was set by an output to register X'57' with byte 1, bit 0 on.
   b. Program abort was set with an output to register X'57' with byte 1, bit 1 on.
   c. A selective or system reset was recognized on the channel interface and is no longer indicated (Op Out is up again).
   d. A channel stop or halt I/O indication was recognized on the channel interface.
6. The channel adapter has received a nonstandard command during an initial selection sequence and has been enabled to accept these commands by an output to register X'56' with byte 1, bit 7 on.

Channel Commands

Because the control program handles most of the functions previously handled by the host access method, the number of commands accepted by the controller has been greatly reduced. Only Test I/O and the following six commands are accepted. All others cause a Unit Check initial status to be returned to the host processor and the Command Reject sense bit to be set in a subsequent Sense command unless the control program has enabled the channel adapter to accept a nonstandard channel command. See *Nonstandard Commands* in this section.

Write (X'01')

This channel command executes a data transfer from the host processor channel to the controller. The data may be user data or a control message to inform the control program of a function to be performed. The data transfer is terminated by (1) a Channel Stop indicated in response to a data service request, or (2) the control word count becoming zero and no further CW chaining being indicated.

Write Break (X'09')

This channel command causes the CA to perform the same functions as a Write command (X'01'). The only difference is that this command sets byte 1, bit 1 (Write Break command remember) in the CA control register (Input X'55'). This permits the host processor to inform the control program of the point it has reached in the host CCW chain.

Write IPL (X'05')

This channel command transfers object code from the host processor to controller storage. When all zeros initial status is accepted by the host processor, the CA presents a level 3 interrupt request and causes the Central Control Unit to initiate IPL phase 1 if the controller is currently initialized. When the CCU read-only-storage code resets the interrupt request, the CA initiates a CW fetch and begins data transfer across the channel. Each time two bytes are received from the channel, a CA cycle-steal operation places the data in storage and increments the CSAR by 2.

The communications controller ends this command in the same manner as a normal Write command; that is, Channel End is generated by the CA hardware, and Device End is generated by interrupt-driven code. This implies that the level 3 interrupt program must have been loaded by the Write IPL command just concluded. If a Halt I/O is received while a Write IPL command is being executed, the host processor must reissue the Write IPL command.

Refer to Chapter 5 for further information on IPL.

Read (X'02')

This channel command executes a data transfer from the communications controller to the host processor channel. The operation is normally ended when a Channel Stop is indicated or the CW count register reaches zero, and either of the following occurs:

1. The CA is executing an Out Stop control word that has CW chaining indicated. The CA presents Channel End and Device End status to the channel and does not request a level 3 interrupt.
2. The CA is executing either an Out CW or Out Stop CW with no CW chaining indicated and with the zero count override bit off. With this condition, the CA presents Channel End status to the

host processor channel and requests a level 3 interrupt. The control program must then signal the CA hardware to present Device End and any other appropriate status to the channel.

If the Read command is terminated by a Channel Stop or Halt I/O, the CA presents Channel End status immediately. When the host processor accepts this status, the channel adapter requests a CA level 3 interrupt. The control program must signal the CA to present Device End and other appropriate status.

Sense (X'04')
The Sense command transfers one byte of sense data from the controller to the host processor channel. This byte is described in the channel adapter sense register (CASNSR). The normal ending status for the Sense command is Channel End, Device End after the channel has accepted the sense byte. No interrupt request is generated.

Except for the not-initialized bit, the sense byte is reset during an initial selection when any host processor command, other than Sense, No-Op, or Test I/O, is accepted by the adapter.

No-Op (X'03')
The channel adapter responds to this command with Channel End, Device End initial status. No further action occurs, and no interrupt request is generated.

Test I/O (X'00')
The channel adapter presents the following initial status in response to a Test I/O:

1. Zero status indicates that the CA is command-free, and there is no pending or stacked status.
2. Busy status is indicated from the acceptance of a command until the generation of Device End. If CE or DE is pending, Busy and CE or DE are presented together.
3. Device End (and any other status) is presented if the ending status is pending or stacked from the previous host processor command.
4. Busy status is indicated if the CA has a level 1 or level 3 interrupt request set.

Once the initial status has been accepted, the Test I/O operation is complete. An interrupt request is not set, and no further action is taken.

Nonstandard Commands
The communications controller recognizes only Test I/O and the above six commands as valid. All other commands are considered nonstandard.

The control program can enable the channel adapter to accept nonstandard commands by executing an Output X'56' instruction to set byte 1, bit 7 on. The CA then responds to a nonstandard command by presenting Channel End rather than Unit Check initial status. The CA also requests a level 3 interrupt, with the CA in the active state, to allow the control program to examine the command register (Input X'5C') and the data buffer (Input X'5A'). A nonstandard command is indicated by byte 1, bit 4 being on in the command register and all other command decode bits being off. The channel command byte is stored in byte 0 of the data buffer (register X'5A'). During this level 3 interrupt, the program can set the command reject bit in the sense register by executing an Output X'53' instruction to turn byte 0, bit 0 on. This output instruction also sets Unit Check in the status register (X'54').

This ability of the channel adapter to accept nonstandard channel commands is reset whenever:

- The controller is powered-up.
- The LOAD or RESET buttons are pressed.
- A Write IPL (X'05') channel command is executed.
- An Output X'56' with byte 1, bit 6 on is executed.

Programming Note
The program must always set Device End in the status register (X'54') during a level 3 interrupt. When the level 3 interrupt is reset by the program, the CA presents the status to the channel.

Status Servicing
The status byte informs the host processor channel if the channel adapter is available to communicate. This status byte is generated by either the CA hardware or the control program and is stored in the channel adapter status register (CASTR).

The four acceptable status configurations for the channel adapter are described below.

Initial Status
Initial status is always generated by the CA hardware without control program intervention. The valid initial status combinations are:

All Zeros: The channel command is accepted.

Channel End, Device End: This is an unconditional response to a No-Op.

Unit Check: An error condition has occurred, and the channel command cannot be executed because:

a. The command is invalid.
b. The channel adapter is not initialized.
c. A bus-out parity error was detected in the command byte.

Further information on the error can be obtained by examining the sense byte.

Unit Exception: When the appropriate control word address register (CWAR) does not contain a valid address, this status is indicated for a Read, Write, or Write Break command. Also, in a controller containing two channel adapters, Unit Exception is returned as initial status to a Sense command if an IPL is in progress on the other channel adapter.

Busy: The controller is already in the process of executing a channel command or the channel adapter level 1 or level 3 interrupt request latch is set. If ending status has been generated for the command currently being executed, this ending status is presented along with Busy as initial status. The only exception occurs when the channel command indicated in the initial selection is a Test I/O.

Ending Status
At the termination of a channel command, the CA generates the following status bits to be passed to the host processor.

Channel End: This status is hardware-generated under normal circumstances for host processor Read, Write, Write Break, and Write IPL commands. Whenever the CA generates CE alone, it also requests a level 3 interrupt. The control program is thus informed of the circumstances that caused the Channel End and must complete the channel operation by signaling the CA to present Device End and any other appropriate status:

Channel End, Device End: This status is normally generated as the ending status for a channel Read command if combined with an Out Stop control word. Channel End, Device End is also the normal ending status for a No-Op or Sense command.

Channel End, Device End, Unit Check: This status is generated by the CA when any one of the following three conditions exists.

a. When a sense bit is set during the execution of a Read, Write, Write Break, or Write IPL command. The CA also requests a level 1 interrupt to inform the control program of the error.
b. When a program abort is indicated by the control program before Channel End status is set during any data transfer command. CASNSR bit 6 (abort sense) is also set, and a level 3 interrupt request is generated.
c. When the controller is in a 'hard stop' state due either to a hardware or program detected malfunction.

Channel End, Device End, Unit Exception: If the sense unit exception latch is on when a sense command is issued, a sense byte is transferred to the host processor followed by a final status of Channel End, Device End, Unit Exception. (See Output X'57' in Appendix B.)

Device End: This status is presented to the host processor when the CA level 3 interrupt request latch is reset after CE status has been presented. Only those status bits generated by the control program, including DE, are presented. Therefore, the control program must never reset the level 3 interrupt request without having set at least Device End in the status register via Output X'54'.

Stacked Status
Stacked status occurs when the channel adapter has status information to present to the channel, but the channel cannot accept it at that time.

When the channel indicates stacked status, the controller status is retained in the channel adapter status register until accepted by the host processor channel. All status except all zeros to a Start I/O is subject to being stacked by the channel.

Stacked ending status is handled in the same manner as stacked initial status. All ending status conditions can be stacked.

Asynchronous Status
The CA presents asynchronous status to the host channel under one of four conditions:

1. The channel adapter receives an Output X'55' instruction from the control program with byte 0, bit 6 set to 1 (set program requested attention), and the CA is not active. Attention status is presented to the host channel when the CA level 3 interrupt request is reset.
2. Execution of an Output X'57' instruction with byte 0, bits 3 and 4 (Set IPL Device End and Unit Check) set to 1 while in IPL Phase 3. This causes the CA to present an asynchronous status of Device End and Unit Check to the host channel and indicates that the controller requires an IPL from the host processor.

3. An asynchronous Device End is presented to the host channel when an interrupt is reset that caused a Busy initial status to be presented in response to an initial selection.
4. An asynchronous Device End is presented to the host channel when the control program executes an Output X'57' instruction with byte 0, bit 3 set to 1.

The Type 3 CA can present asynchronous status to either channel. If both channel interfaces are enabled, the first channel to poll the Type 3 CA is offered the status.

A channel receives a Busy status if it attempts an initial selection sequence while the Type 3 CA is logically connected to the opposite channel. The CA presents an asynchronous Device End to this channel as soon as the opposite interface's connection is terminated.

Multiple Channel Operation

A 3705 with more than one channel adapter installed is capable of multiple channel operation. The channel adapters can be installed only in the basic frame and first expansion frame of a 3705. Figures 1-5 through 1-8 show the available channel adapter configurations and the frames in which the adapters must be installed. The control program issues an Output X'57' instruction to select the desired Type 2 or Type 3 CA and an X'67' instruction to select the desired Type 4 CA. (Refer to Appendix B for Output X'57' and Output X'67' bit definitions.)

If two type 2 CAs are installed, both can be attached to the same channel or each to a separate channel. Both adapters operate independently and can be enabled concurrently.

If a Type 3 CA is installed, its two interfaces can be attached to a uniprocessor as an I/O unit with an alternate path capability, or they can each be attached to a separate CPU of a tightly-coupled multiprocessor. Both interfaces can be enabled concurrently, but simultaneous operation is not permitted. When a channel I/O operation over one interface is being executed, an initial selection sequence attempt by the channel associated with the other interface will cause a busy status to be presented to that channel.

Either of the Type 3 channel interfaces can be manually enabled or disabled by using the channel enable/disable toggle switches located on the 3705 control panel. These toggle switches may be alternately located on a remote configuration console of a multiprocessing system.

When both interfaces are enabled, the adapter is selected by the first channel to initiate a selection sequence. If both channels simultaneously poll the Type 3 CA, the adapter logic breaks the tie. If the enable/disable switch for either interface is moved to the disable position, that interface can go offline subject to the following conditions:

- The channel adapter is not executing a command on that interface.
- Command chaining is not being indicated for that interface.
- A Device End status is not pending on that interface.
- The CPU is in a wait state.
- An Input X'58' instruction is not being executed to examine the state of the 'enable' latch.
- 'Select Out' is not up on that interface.

If the switch is moved to the enable position, the interface can go online if the CPU is in a wait state and the 3705 is not executing an Input X'58' to examine the state of the 'enable' latch.

Note: *A pending asynchronous status, which is available to either channel, does not inhibit manually disabling an interface. If the CA is presenting asynchronous status to the channel when the disabling switch is thrown, that sequence is completed.*

Type 3 Channel Adapter-Channel Interface States

The Type 3 CA can be in one of three states in relation to the attached channel interfaces: disabled, neutral, or switched.

Disabled: When an interface of the Type 3 CA is disabled by the use of the enable/disable switch, the 3705 appears not-operational to the associated channel.

Neutral: In this state the adapter is enabled and available to both attached channels, but is not logically connected to either channel.

Switched: The adapter enters the switched state when it becomes logically connected to a channel when the channel or the channel adapter attempts an initial selection sequence. The adapter remains switched to a channel after an initial selection sequence ends if the channel accepts an all zero status from the adapter in response to a command for which (1) subsequent communication is required (data transfer and/or ending status required to complete the command), or (2) command chaining is indicated for a No-Op.

If the adapter remains switched after the initial selection sequence is completed, it maintains the logical connection to the channel until one of the following occurs:

- The channel accepts Device End status for the last command of a particular Start I/O that does not indicate command chaining,
- Command chaining is suppressed after the channel's acceptance of Device End status, but before reselection occurs.
- System or selective reset is received over that interface.

While in the switched state the adapter continually monitors the opposite interface and responds to an initial selection sequence over that interface in one of two ways:

- The CA temporarily suspends the selection sequence if it is already involved in an initial selection sequence with the first channel. If the CA returns to the neutral state as soon as the initial selection sequence is completed (as would be the case if the adapter had instigated the sequence to present asynchronous status), the opposite channel completes its initial selection sequence, which had been delayed.
- The adapter responds with a Device Busy status. In this case, the first channel has (1) already accepted an all-zero status from the CA in response to a command for which subsequent communication is required, or (2) sent a No-Op instruction for which command chaining is indicated.

The adapter does not remain in the switched state after the initial selection sequence is completed if the sequence was instigated by the Type 3 CA to present asynchronous status to a channel and the channel has accepted or stacked the status.

Error Condition: If the Type 3 CA ends a channel command with Unit Check status indicating an error condition, the adapter remains switched to that channel until one of the following occurs:

- The adapter decodes a command other than Test I/O or No-Op.
- A system or selective reset is detected over the channel to which the adapter is switched.
- A 3705 hard stop occurs.

In this way the Type 3 CA ensures the availability and use of the same channel path to return sense data after an I/O operation has ended with Unit Check status. A halt I/O presented over the channel to which the adapter is logically connected does not cause it to leave the switched state. Under any of these conditions, any selection attempt by the opposite channel will receive a Device Busy status.

Type 3 CA Response to Resets

There are several different reset combinations for the Type 3 CA. The following paragraphs describe those combinations.

System Reset Over the Interface To Which the Adapter Is Switched: A system reset from the channel to which the adapter is switched will always be recognized, will reset the adapter (CA returns to neutral state), and will cause a level 3 interrupt. Only a pending Device End due to a previous Device Busy over the opposite interface is not reset.

Selective Reset over the Interface to Which The Adapter Is Switched: A selective reset over the interface to which the CA is switched performs the same function as a system reset.

System and Selective Resets—Adapter Neutral: The only interface activity which may be reset when the adapter is neutral is a pending asynchronous status. A pending Device End due to a previous Device Busy is reset only if the reset indication is received over the interface for which the Device End is intended.

System Reset over the Opposite Interface: A system reset received over the channel opposite that to which the interface is switched resets only a pending Device End for the channel over which the reset is being signaled. No further action is taken, no level 3 interrupt is requested, and no further resetting of the adapter occurs.

Input/Output Instructions

The channel adapter input/output instructions enable the control program to communicate with the host

processor I/O channel. These instructions are available to the control program only when the CA is selected and (1) a level 1 or level 3 interrupt has been requested or (2) the CA is in the diagnostic wrap state. Type 2 and Type 3 CA instructions are specified by X'50' to X'5F'.

Input Instructions

Twelve input instructions allow the control program to obtain the status of various channel adapter registers. Listed below are the usable Type 2 and Type 3 CA input instructions and the registers associated with them. The register descriptions are found elsewhere in this chapter. See Appendix B for the input instruction bit definitions.

When the adapter is selected and a CA L1 or L3 interrupt request is set, or the CA is in the diagnostic wrap state, execution if Input X'57', X'5D', X'5E', or X'5F', results in loading all zeros into the general register specified by the R operand. If the CA is not selected or an interrupt has not been requested, any attempt to execute an Input X'50' through X'5E' results in an in/out check L1 interrupt request.

Input X'50':
Inbound Data Control Word Address Register (INCWAR).

Input X'51':
Outbound Data Control Word Address Register (OUTCWAR).

Input X'52':
Control Word Byte Count Register (CWCNTR).

Input X'53':
Channel Adapter Sense Register (CASNSR).

Input X'54':
Channel Adapter Status Register (CASTR).

Input X'55':
Channel Adapter Control Register (CACR).

Input X'56':
Channel Adapter Check Register (CACHKR).

Input X'58':
Channel Bus Out Diagnostic Register (CBODR).

Input X'59':
Cycle Steal Address Register (CSAR).

Input X'5A':
Channel Adapter Data Buffer (CADB)

Input X'5B':
Channel Tag Diagnostic Register (CTDR)

Input X'5C':
CA Command Register (CMDR)

Output Instructions

Eleven output instructions allow the control program to set the bits of various channel adapter registers. Listed below are the usable CA output instructions and the registers associated with them. The register descriptions are found elsewhere in this chapter.

One of these instructions (Output X'59') is for diagnostic purposes. It allows a diagnostic program to make either interface or both interfaces Busy. See Appendix B for output instruction bit definitions.

When the adapter is selected and a CA L1 or L3 interrupt request is set or the CA is in the diagnostic wrap state, the execution of an Output X'52', X'5C', X'5D', X'5E', or X'5F' instruction is ignored. If the CA is not selected or an interrupt has not been requested, any attempt to execute an Output X'50' through X'5F' results in an in/out check L1 interrupt request.

Output X'50':
Inbound Data Control Word Address Register (INCWAR).

Output X'51':
Outbound Data Control Word Address Register (OUTCWAR).

Output X'53':
Channel Adapter Sense Register (CASNSR).

Output X'54':
Channel Adapter Status Register (CASTR).

Output X'55':
Channel Adapter Control Register (CACR).

Output X'56':
Channel Adapter Control Register (CACR).

Output X'57':
Channel Adapter Mode Register (CAMR).

Output X'58':
Channel Bus Out Diagnostic Register (CBODR).

Output X'59':
Type 3 CA Diagnostic Control (CADC).

Output X'5A':
Channel Adapter Data Buffer (CADB).

Output X'5B':
Channel Tag Diagnostic Register (CTDR).

Error Indications

When the channel adapter hardware detects an error condition, a level 1 interrupt request is automatically set. With this request, a bit is also set in the channel adapter check register (X'56') to indicate the nature of the error. The level 1 interrupt handling routine, using an Input X'56' instruction, should then analyze the contents of this register to determine the cause of the error and execute appropriate recovery procedures.

Refer to the channel adapter check register (CACHKR) and Appendix B for the error bit definitions and register reset.

The following are the valid CA error checks:

- Invalid CWAR Address
- Invalid Control Word Format (See Note)
- Data Address Error
- Buffer Parity Error
- Outbus Parity Error
- Inbus Parity Error
- Channel Bus In Parity Error
- Channel Bus Out Check

Note: An Invalid Control Word Format check may also cause an Interface Control check on the system channel and "hang" the CPU. Whether this will occur depends upon the CPU and channel type.

Chapter 11: Remote Communications Controller

This chapter describes the requirements necessary to support a 3704 or 3705 at a remote location. (See the *Introduction to the IBM 3704 and 3705* manual for introductory information about the remote communications controller.) Throughout this chapter, both the controller attached to the host processor and the control program of that controller are referred to as the local communications controller and the local control program respectively. The 3704 or 3705 located at a site away from the host processor and connected to the local communications controller by a local/remote communication link is referred to as the remote communications controller. The control program that resides in the remote communications controller is called the remote control program.

A 3705-II can be equipped with both a remote program loader and one to three channel adapters, thus allowing it to function as either a local or a remote communications controller. The program it contains determines which of the two functions it performs. If the program can communicate with an attached CPU over one or more channel adapters, the 3705-II is a local controller. If the program cannot communicate with the CPU over a channel adapter, the 3705-II functions as a remote controller.

Local/Remote Communication Link

Communication between the local and remote controllers is over a local/remote communication link using the synchronous data link control (SDLC) discipline. Support of SDLC is required in both the local and remote controllers.

For information on the SDLC line discipline, refer to the *Synchronous Data Link Control General Information* manual.

Data flow through the local controller is the same as described in Chapter 1. However, in support of a remote controller, the data being transmitted to the remote unit exits the local controller via a communication scanner SDLC interface. The local/remote communication link attaches to an SDLC interface of a remote communication scanner; therefore, data enters the remote controller as a *received* message and the control program must turn this data around and *transmit* it to the proper communications line for the intended destination. (Refer to Figure 11-1.)

Remote Program Loader

The remote program loader provides a remote communications controller with an independent IPL capability and a source of resident diagnostics. The following functions and hardware are provided with the remote program loader.

- A diskette storage drive and diskette controller that provide a source for the load programs and diagnostic programs.
- A register for storing the type of program load and stimulus.
- A ROS bootstrap program and two load programs that (1) test the instructions used to load programs from the diskette, (2) perform a check of the diskette controller and, (3) control the transfer of a load program from diskette storage to main storage.

The diskette used in the diskette storage drive contains from one to three physical records on each of its 77 tracks and has a minimum access time of 150 milliseconds per track. The diskette is the source of load and diagnostic programs for the remote unit and therefore serves as read-only-storage. The ability to write on this diskette is normally disabled so as to provide file protection. The only time a write operation can be performed on the diskette is when the controller is in the *not initialized* state (for example, IPL Phase 2 or Phase 3), or when a jumper wire is placed on the write circuit for maintenance purposes.

The following table lists the contents of the tracks.

Track	*Content*	*Description*
0	Load Program 1 (LPG1)	(1) Program that is transferred to main storage by the ROS boot-strap to control further loading of programs. (2) Defines the local/remote communication link for LPG2 (IPL configuration data set).
1-3	(3705-I)	
1-4	(3705-II) Initial Test	A CCU diagnostic exerciser.
4-5	(3705-I)	
5	(3705-II) (Reserved)	
6-7	Load Program 2 (LPG2)	Controls the local/remote communication link for loading and dumping.
8	IFT Loader/CDS Writer	
9	Diagnostic Control Monitor	

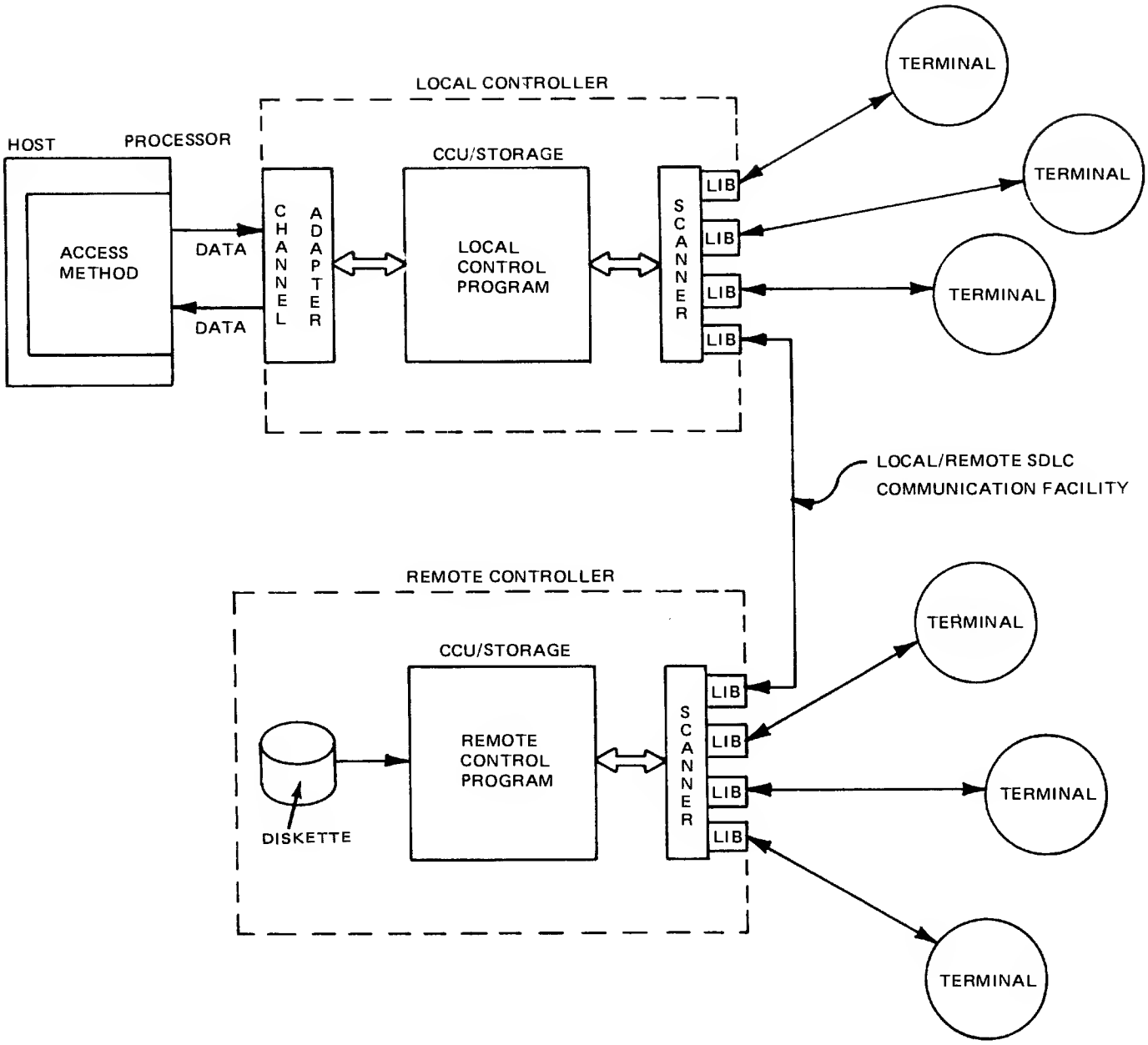


Figure 11-1. Data Communication System with Local and Remote Communications Controllers

10	Hardware Configuration Data Set (CDS) for Internal Functional Tests (IFT)	Defines the hardware configuration for the internal functional tests.
11	Load Program 1	Duplicate of track 0.
12-13	Load Program 2	Duplicate of tracks 6 and 7.
14-18	(Reserved)	
19-76	IFT	Internal Functional Tests.

Remote Program Loader Input Instructions
Four input instructions give the controlling program access to the various remote program loader registers. These instructions are listed below. For a description of each bit used in these instructions, refer to the *Remote Program Loader* section of Appendix B.

Input X'68' (Level 1 Status): This instruction allows the controlling program to examine the contents of the level 1 status register to determine the cause of a remote program loader level 1 interrupt.

Input X'69' (Level 3 Status): This instruction allows the controlling program to examine the contents of the remote program loader level 3 status register after a level 3 interrupt request or when the disk controller is in a reset state.

Input X'6A' (Parallel Data Register): This instruction is used to transfer data into main storage during a disk data transfer. It is also used for diagnostic purposes.

Input X'6B' (Control Program Load Data Register): This instruction is used to supply information required during IPL and program load phases.

Remote Program Loader Output Instructions
Four output instructions are used to allow the controlling program to initiate disk read, write, and control operations. Listed below are the remote program loader output instructions. The bit positions are described in the *Remote Program Loader* section of Appendix B.

Output X'68' (Control): This output is used to prepare the disk controller for subsequent read or write operations by controlling the access mechanism, engaging the read/write head, setting and resetting latches, and setting write current.

Output X'69' (Read/Write): This output commands the disk controller to perform read or write operations. A write operation can be performed only if (1) the communications controller is not initialized, or (2) the 'write enable' back panel jumper is installed.

Output X'6A' (Parallel Data Register): This output is used to load the register which holds data being transferred from the Central Control Unit (CCU) to the disk storage. It is also used for diagnostic purposes.

Output X'6B' (Control Program Load Register): This instruction is used to store information needed during the IPL and program load phases.

Remote Program Loader CCU Instructions
Two additional bits are required within existing CCU input instructions to support the remote program loader. They are byte 0, bit 7 of Input X'76', and byte 1, bit 1 of Input X'77'. See *CCU Input Instructions* in Appendix B for a description of these bits.

Disk Storage Controller

The disk storage controller is the logical connection between the disk storage drive and the Central Control Unit. This controller, under control of the program residing in main storage, controls all operations (read, write, access, etc.) of the disk storage.

Track Access
The head for the disk can be moved only one track at a time. Therefore, a move of multiple tracks must consist of a multiple of single track moves. For each track that the head is to be moved, the control program must execute an Output X'68' instruction with byte 1, bit 1 set to 1. This bit indicates to the controller that the head is to be moved. In addition, byte 1, bit 2 of Output X'68' must be set to indicate the direction of movement. When byte 1, bit 2 is *on*, the head moves in a forward direction (the next higher track number), and when this bit is *off*, the head moves in a reverse direction (toward track 0).

Each time the head is moved from one track to another, a counter in the level 3 status register is updated. By executing an Input X'69' instruction (level 3 status) and then examining byte 0, bits 2-5 of the general register specified, the control program can determine if the access mechanism has moved.Keeping track of the head position is the responsibility of the control program.

To recalibrate the disk head, the control program must reset the access counter by turning byte 0, bit 3 of Output X'68' on and then executing 80 single track moves in the reverse direction (Output X'68', byte 1, bit 1 on and bit 2 off). When these moves are com-

plete, the head is at track 0 (home position), and the access counter is also 0.

To prevent undue wear on the surface of the disk, the head should not be engaged during track to track movement. The head will automatically disengage after a read or write operation within two revolutions of the disk (332 milliseconds) unless one of the operations is re-initiated. Therefore, the control program should ensure that enough time has elapsed to disengage the head prior to a move. Because of this automatic disengage operation, a head engage (Output X'68', byte 1, bit 4 on) should precede each read or write operation.

Track Format

Because the disk used in the remote communications controller is not interchangeable with other machines, the format of the disk records does not follow any previously established standards. The record format is designed to meet the needs of the 3704/3705. The format is as follows:

```
*--GI--VFO SYNC--DS--BH--DATA--CRC--GF--*
Index                                Index
```

GI	= Initial Gap - 128 bytes of X'FF'
VFO SYNC	= 8 bytes of X'00'
DS	= Data Sync - 1 halfword X'0005'
BH	= Block Header - 16 halfwords
DATA	= Maximum of 4668 bytes - 1 physical record with three logical records
CRC	= Cyclic Redundancy Check Character - 2 bytes
GF*	= Final Gap to Index - X'FF'

Block Header Format:

Halfword	*Description*
1	Track ID (X'0000' through X'004C')
2	Control Information
3	Reserved
4	Reserved
5	Logical Record 1 Byte X Storage Address (Extended Addressing)
6	Logical Record 1 Bytes 0 & 1 Storage Address
7	Logical Record 1 Count (Two's complement)
8	Program Version Level
9	Logical Record 2 Byte X Storage Address (Extended Addressing)
10	Logical Record 2 Bytes 0 & 1 Storage Address
11	Logical Record 2 Count (Two's complement)
12	ZAP Count (Number Of Temporary Fixes To This Track)
13	Logical Record 3 Byte X Storage Address (Extended Addressing)
14	Logical Record 3 Bytes 0 & 1 Storage Address
15	Logical Record 3 Count (Two's complement)
16	Block Header CRC Character

The logical record storage address is the main storage address where the logical record is placed during a read operation. Each of the logical records may vary in length which is indicated by the *count.*

Note: *The CRC is compatible with the SDLC CRC. See the Cyclic Redundancy Check section of Chapter 5.*

Disk Read and Write Operations

The disk controller performs all read and write operations under the direction of the control program. Only single read or write operations are permitted. Prior to any read or write of the disk, the desired track must be located and the head engaged. The following paragraphs describe the read and write operations.

Read Operation: To initiate a read operation, the control program must execute an Output X'69' instruction with byte 0, bit 2 set to 1. Following this output, the next time the index is detected from the disk (detection of index is a hardware function), the controller begins to shift bits from the disk through the serializer/deserializer circuits and into the controller's parallel data register. When the data sync pattern (X'0005') is recognized by the sync decode circuits, the controller is considered to be in sync with the incoming disk storage data. From this point on, the controller requests a level 3 data service interrupt at each 16-bit (halfword) interval until the index is again detected. The second time the index is passed, the read operation is terminated.

While this read operation is in progress, the control program must service each level 3 interrupt to receive the incoming data and place it in storage. Because the information in disk storage is the IPL and diagnostic programs, the controller will not be executing any other program that would interfere with the processing of incoming data.

Servicing the level 3 interrupt must consist of at least the following sequence of instructions:

- Input X'77'—To determine the cause of the interrupt.
- Input X'69'—To determine the status of the read operation.

- Input X'6A'—To load contents of the controller parallel data register into a general register for subsequent transfer to storage.
- Output X'68'—To reset the level 3 interrupt request and the controller status registers and to set any other desired control information.
- Some type of store instruction to transfer the halfword just received in the general register to the proper storage location.

The read operation can be terminated by the control program with a controller reset (Output X'68', byte 1, bit 5). This reset is recommended after the CRC characters are read so as not to read the final gap into main storage.

Write Operation: To initiate a write operation the control program must execute an Output X'69' instruction with byte 0, bit 1 set to 1. Following this output, the disk controller immediately requests a level 3 interrupt. The control program can then transfer the first halfword of information to the controller. One halfword is transferred for each level 3 interrupt until the write operation is terminated.

Before executing the Output X'69' to request the write operation, the control program should have loaded a general register with the first halfword of information to be written on the disk. Servicing the level 3 interrupt must consist of at least the following sequence of instructions.

- Input X'77'—To determine the cause of the interrupt.
- Output X'68'—To set the proper control information.
- Output X'6A'—To load the contents of the general register (data to be written) into the controller parallel data register from which it is written on the disk.
- Output X'68'—To reset the level 3 interrupt request.
- Some type of load instruction to place the next halfword to be written into the general register specified in the Output X'6A' instruction.

The controller starts writing data on the disk at the index and continues to write halfwords until the next time the index is encountered. At this point the write operation is terminated.

The control program is responsible for writing the *complete* track on the disk. This includes the initial gap, VFO sync, data sync, block header, up to 4668 bytes of data, the CRC character, and the all ones field for the final gap. (See *Track Format* in this chapter.) The controller assures proper serialization of the data onto the disk as it is received from the control program.

A write operation can be done only when the write circuits are enabled. See *Remote Program Loader* in this chapter. Attempting to do a write operation when the write circuits are not enabled causes a level 1 interrupt. Normally, the only time a write operation is performed is when a dump is required during an IPL or when the customer engineer has to write for maintenance purposes.

Initial Program Load

The initial program load (IPL) mechanism controls the loading of an initial program into main storage from disk storage. Three phases of the IPL program (IPL Phase 1-3) control the loading operation. IPL is accomplished by successful completion of all three phases. These three phases are similar to the local IPL operation described in Chapter 5. Therefore, this chapter only points out the differences required for remote operation.

IPL phase 1 and phase 2 are identical to phases 1 and 2 of the local controller's IPL program except that the bootstrap program for the remote controller consists of 1024 bytes. Phase 3 of the remote IPL program is divided into three sections.

The first section performs the same checks and saves the same registers as section one of the local IPL program. The second section of the remote phase 3 tests the disk storage drive and the disk controller. Section three of phase 3 controls the loading of load program 1 from disk storage to main storage.

The remainder of the IPL operation is controlled by load program 1 (LPG1) and load program 2 (LPG2). See Figure 11-2 for a flow chart description. LPG1 determines if a dump of the remote controller's storage is required by examining register X'6B' and the ADDRESS/DATA switches (3705) or the Hexadecimal Readout Display (3704). If a dump is required, LPG1:

1. Turns on byte 0, bit 0 of register X'6B'.
2. Transfers contents of high 8K of main storage to tracks 15 and 16 of the disk.
3. Transfers LPG2 from disk tracks 6 and 7 to the high 8K of main storage.

LPG1 then passes control to LPG2.

If no dump is required, LPG1 transfers initial test from disk tracks 1-5 to main storage. LPG1 loads the internal function tests if they have been requested at the control panel. If there is no request to load the internal function tests, load program 2 (LPG2) is loaded and given control.

LPG2 controls loading the control program into main storage from the local/remote communication

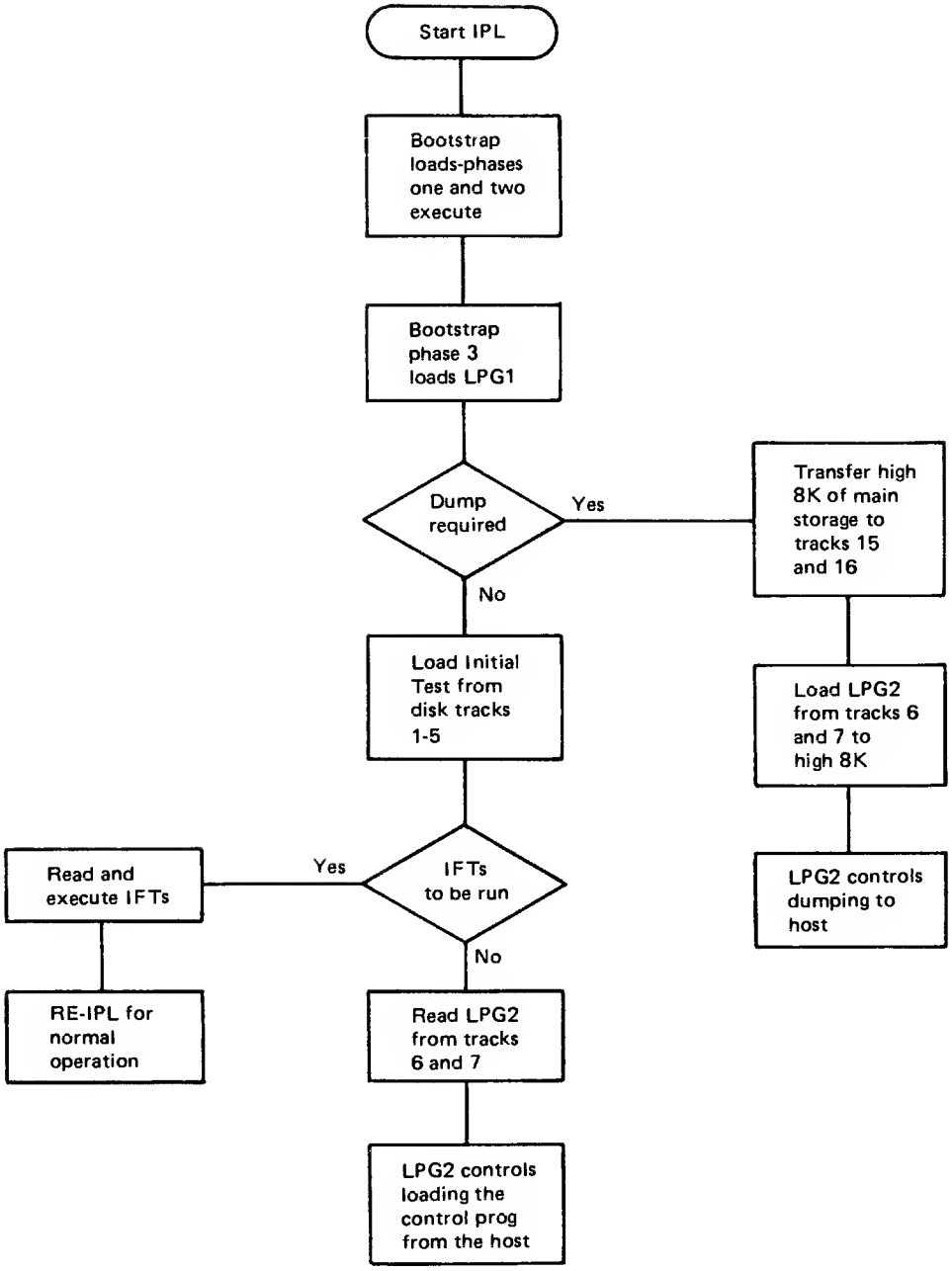


Figure 11-2. IPL–Remote Communications Controller

link; or, when a dump is required, it controls transferring the contents of main storage and disk tracks 15 and 16 over the local/remote communications link to the local communications controller.

Register X'6B' is available to a remote communications controller to store and pass information which may be required by the IPL and LOAD programs. Refer to Appendix B for a description of the bits of this register.

3705-II Equipped with Both RPL and CA

A 3705-II can be equipped with both a remote program loader and one to three channel adapters. A controller so equipped can be loaded either over the local-remote communication link or over one of the channel adapters. The conditions that determine which option is used are as follows.

The controller is loaded over the local-remote link if the control program executes (1) an Output X'6B' instruction in which the IPL source indicator bit (0.4) is 1 and (2) an Output X'79' instruction that sets the Set IPL latch bit (0.2), *provided that*:

- no CA Enable/Disable switch is in the Enable position; *and*
- no CA is currently in the enabled state.

The controller is loaded over a channel adapter if the control program has not requested an IPL from the communication link (that is, an Output X'6B' instruction in which bit 0.4 [IPL source] is 1 has not been executed), *and*:

- any CA Enable/Disable switch in the Enable position; *or*
- any channel adapter is currently enabled (regardless of the switch position).

Remote Power Off

This feature allows the user to power down the remote controller by issuing a command from the host processor. The command issued by the host causes the remote control program to execute an Output X'79' instruction with byte 0, bit 4 set to 1. When power is turned off this way it can only be restored manually at the control panel. (This feature is not available in a 3705-II equipped with both a remote program loader and one or more channel adapters.)

Appendix A: External Register Addresses

Input Register Addresses

E Field	Register/Function	
00	Gen Reg, Group 0	Reg 0
01		Rag 1
02		Reg 2
03		Reg 3
04		Reg 4
05		Reg 5
06		Reg 6
07		Reg 7
0B	Gen Reg, Group 1	Reg 0
09		Reg 1
0A		Reg 2
0B		Reg 3
0C		Reg 4
0D		Reg 5
0E		Reg 6
0F		Reg 7
10	Gen Reg, Group 2	Reg 0
11		Reg 1
12		Reg 2
13		Reg 3
14		Reg 4
15		Reg 5
16		Reg 6
17		Reg 7
1B	Gen Reg, Group 3	Reg 0
19		Reg 1
1A		Reg 2
1B		Reg 3
1C		Reg 4
1D		Reg 5
1E		Reg 6
1F		Reg 7
20	See Note 1	
21		
22		
23		
24		
25		
26		
27		
2B		
29		
2A		
2B		
2C		
2D		
2E		
2F		
30		
31		
32		
33		
34		
35		
36		
37		
38		
39		
3A		
3B		
3C		
3D		
3E		
3F		

E Field	Register/Function		
		Type 2 Scanner	Type 1 Scanner
40		Interface Addreaa	Unused
41		Unused	Interface Address
42		Unused	CNTL A
43		Check Register	CNTL B/C
44		ICW Input Rag 0-15	Status
45		ICW Input Reg 16-31	Unused
46		Diaplay Register	Unused
47		ICW Input Reg 32-45	Unuaed
4B	See Note 1		
49			
4A			
4B			
4C			
4D			
4E			
4F			
50	Type 2 or Type 3 CA	INCWAR	
51		OUTCWAR	
52		Control Word Byte Count	
53		Senaa Register	
54		Status Register	
55		Control Register	
56		Check Registar	
57		Sea Note 2	
5B		Channel Bus Out Diag Reg	
59		Cycle Steal Address Reg	
5A		Data Buffer	
5B		Tag Diagnostic Reg	
5C		Command Ragister	
5D		Sae Note 2	
5E		See Note 2	
5F		See Note 2	
60	Type 1 or Type 4 CA	Initial Selaction Control	
61		Initial Selection Address & Command	
62		Data/Statua Control	
63		Address end ESC Status	
64		Deta Buffer Bytes 1,2	
65		Data Buffer Bytea 3,4	
66		NSC Status Byte	
67		Controls	
6B	Remote Loader	Level 1 Status	
69		Level 3 Status	
6A		Parallel Data Reg	
6B		Control Program Load Reg	
6C	See Note 1		
6D			
6E			
6F			
70		Storage Size Inatalled	
71		Panel Address/Data Digits	
72		Penel Function Select Controls	
73		Insert Key	
74		LAR	
75		See Note 2	
76		Adepter Level 1 Interrupt Requests	
77		Adapter Level 2 or 3 Interrupt Requests	
7B		See Note 2	
79		Utility	
7A		Cycla Utilization Counter Register	
7B		BSC CRC	
7C		SDLC CRC	
7D		CCU Check Register	
7E		CCU Level 1 Intarrupt Requests	
7F		CCU Level 2,3,or 4 Interrupt Requests	

Note 1: A conatant of ell zeros is loaded into R end tha Input/Output check L1 request is set.

Nota 2: A constant of all zeros is loaded into R.

Output Register Addresses

E Field	Register/Function	
00	Gen Reg, Group 0	Reg 0
01		Reg 1
02		Reg 2
03		Reg 3
04		Reg 4
05		Reg 5
06		Reg 6
07		Reg 7
0B	Gen Reg, Group 1	Reg 0
09		Reg 1
0A		Reg 2
0B		Reg 3
0C		Reg 4
0D		Reg 5
0E		Reg 6
0F		Reg 7
10	Gen Reg, Group 2	Reg 0
11		Reg 1
12		Reg 2
13		Reg 3
14		Reg 4
15		Reg 5
16		Reg 6
17		Reg 7
1B	Gen Reg, Group 3	Reg 0
19		Reg 1
1A		Reg 2
1B		Reg 3
1C		Reg 4
1D		Reg 5
1E		Reg 6
1F		Reg 7
20		
21		
22		
23		
24		
25		
26		
27		
2B		
29		
2A		
2B		
2C		
2D		
2E		
2F		
30	See Note 1	
31		
32		
33		
34		
35		
36		
37		
3B		
39		
3A		
3B		
3C		
3D		
3E		
3F		

E Field	Register/Function	
	Type 2 Scanner	**Type 1 Scanner**
40	Interface Address	Set Mode Bit Override
41	Address Substitution Control	Start Scanner & Reset Bit L2
42	Upper Scan Limit Control	CNTL A
43	Control	CNTL B
44	ICW 0-15	General Control
45	ICW 16-23	Scanner Control
46	ICW 24-33,44	Set Char Service Pending
47	ICW 34-43	Force L2 Bit SVC Request
4B		
49		
4A		
4B	See Note 1	
4C		
4D		
4E		
4F		
50	INCWAR	
51	OUTCWAR	
52	See Note 2	
53	Set Sense Register Bits	
54	Set Status Register Bits	
55	Set Control Register Bits	
56	Reset Control Register Bits	
57	Channel Adapter Mode Reg	
5B	Channel Bus Out Diag Reg	Type 2 or Type 3 CA
59	Type 3 CA Diag Busy Reg	
5A	Channel Adapter Data Buffer	
5B	Tag Diagnostic Reg	
5C	See Note 2	
5D	See Note 2	
5E	See Note 2	
5F	See Note 2	
60	Reset Initial Selection	
61	Unused	
62	Data/Status Control	
63	Address and ESC Status	
64	Data Buffer Bytes 1,2	Type 1 or Type 4 CA
65	Data Buffer Bytes 3,4	
66	NSC Status Byte	
67	Control	
6B	Control	
69	Read/Write	Remote
6A	Parallel Data Reg	Loader
6B	Control Program Load Reg	
6C		
6D	See Note 1	
6E		
6F		
70	Hardstop	
71	Display Reg 1	
72	Display Reg 2	
73	Set Key	
74	See Note 2	
75	See Note 2	
76	See Note 2	
77	Miscellaneous Control	
7B	Force CCU Checks	
79	Utility	
7A	Cycle Utilization Counter Register Reset	
7B	See Note 2	
7C	Set PCI Level 3	
7D	Set PCI Level 4	
7E	Set Mask Bits	
7F	Reset Mask Bits	

Note 1:
The bits of R are ignored and the Input/Output check L1 request is set.

Note 2:
The bits of R are ignored.

Appendix B: Input/Output Instruction Bit Definitions

Type 1 Scanner Input Instructions

Input X'41' (Interface Address)
When operating in the bit service mode, this instruction causes a storage address associated with an interface to be loaded into the specified general register. The selected interface is where the scanner has stopped because of an interrupt request. The storage address is a fixed location, determined by the LIB position and the interface address assigned to the line causing the interrupt. Figure 3-5 shows the storage addresses associated with each interface address.

When operating in the character service mode, a fixed address of X'06F0' is loaded into the specified register.

Input X'42' (Control A)
The Input X'42' instruction should be executed only when the scanner is stopped on an interface. This input instruction can be used to check the state of the Output X'42' (control A) instruction. When executed for a particular line, the result in the register specified by the R operand is a bit-for-bit reflèction of the control information set by the Output X'42' instruction for that interface. Refer to the Output X'42' instruction for the definition of each bit position.

Input X'43' (Control B/C)
This instruction cannot be executed immediately following an Output X'43' for feedback checking.However, it can be executed after an Output X'43' to obtain other status indications.

Byte 0, bit 0: Receive Data Bit Buffer—This position indicates a mark or space condition received from the line interface (1 = a mark, 0 = a space).

Byte 0, bit 1: Feedback Check—This bit is set on if a bit to be transmitted is not transferred to the interface correctly or if the interface bit service request fails to reset.

Programming Note
After a feedback check occurs, the bit-service interrupt request cannot be reset and the scanner cannot be restarted until the control program has reset the check indication with an Output X'44' with byte 1, bit 6 set to 1.

Byte 0, bit 2: Interface Check Summary—This bit is set on to indicate (1) the detection of a feedback error, (2) bit overrun/underrun, or (3) 'data set ready' line not active. It is a summary of these check conditions and is set to 1 when byte 0, bit 1, or byte 1, bit 2 or bit 7 of this input is on.

Byte 0, bit 3: Received Data Lead—This bit indicates the level of the 'receive data' signal from the modem. A 1 indicates a space level and 0 indicates a mark level.

Byte 0, bit 4: Transmit Mode—A 1 in this position indicates that the line interface is set for transmit mode; a 0 indicates that it is set for receive mode.

Byte 0, bit 5: New Sync—This position indicates the state of the 'new sync' line to the modem. A 1 indicates that the line is active. A 0 indicates that the line is inactive.

Byte 0, bit 6: Request to Send (RTS)—A 1 in this position indicates that the 'request to send' line to the modem is active. A 0 indicates that the line is inactive.

Byte 0, bit 7: Send Data Bit Buffer—This position shows the setting of the line interface send data buffer. A 1 indicates a mark, and a 0 indicates a space.

Byte 1, bit 0: Not Clear to Send—A 1 in this position indicates that the 'clear to send' line from the modem is *inactive.* A 0 indicates that it is active.

Byte 1, bit 1: Ring Indicator—If this bit is 1, the 'ring indicator' line from the modem is active. A 0 indicates that it is inactive.

Byte 1, bit 2: Not Data Set Ready—When this position is A 1, the 'data set ready' line from the modem is *inactive.* A 0 indicates that it is active.

Byte 1, bit 3: Received Line Signal Detector—When the 'receive line signal detector' line from the modem is active, this bit is 1. A 0 indicates that the line is inactive.

Byte 1, bit 4: Telegraph Interface Echo Check—If this bit position is 1, a TTY echo check has occurred.

Byte 1, bit 5: Diagnostic Mode—A 1 in this position indicates that the line interface is set for the diagnostic wrap mode, and a 0 indicates that it is set for the normal read/write mode. See Type 1 Scanner *Diagnostic Wrap* in Chapter 6. If this bit is a 1, then byte 1, bit 2 of this input is forced to 0 and byte 1, bit

3 of this input is forced to a 1. If this bit is 1 and byte 0, bit 6 is 1, byte 1, bit 0 is forced to 0.

Byte 1, bit 6: Bit Service—A 1 in this position indicates that the scanned interface has requested a bit service.

Byte 1, bit 7: Bit Overrun/Underrun—A 1 in this position indicates that a bit overrun or underrun has occurred.

Autocall Interface Bits for Input X'43'

Byte 0, bit 0: This bit is 0.

Byte 0, bits 1-2: These bits are the same as for line interface.

Byte 0, bit 3: Digit Present (DPR)—A 1 in this position indicates that the 'digit present' signal to the autocall unit is active; a 0 indicates that the signal is inactive.

Byte 0, bits 4-7: These bit positions represent the autocall dial digit in BCD form.

Byte 1, bit 0: Not Abandon Call and Retry—A 1 in this position indicates that the 'abandon call and retry' signal from the autocall unit is *inactive.* A 0 indicates that it is active.

Byte 1, bit 1: Present Next Digit (PND)—A 1 in this position indicates that the 'present next digit' signal from the autocall unit is active; a 0 indicates that the signal is inactive.

Byte 1, bit 2: Not Data Line Occupied (Not DLO)—A 1 in this position indicates that the 'data line occupied' signal from the autocall unit is *inactive.* A 0 indicates that it is active.

Byte 1, bit 3: Power Indicator (PWI)—A 1 in this position indicates that the 'power indicator' signal from the autocall unit is active; a 0 indicates that the signal is inactive.

Byte 1, bit 4: Call Request (CRQ)—A 1 in this position indicates that the 'call request' signal to the autocall unit is active; a 0 indicates that the signal is inactive.

Byte 1, bit 5: Call Originating Status (COS)—A 1 in this position indicates that the 'call originating status' signal from the autocall unit is active; a 0 indicates that the signal is inactive.

Byte 1, bits 6-7: These bits are the same as for a line interface operation.

Input X'44' (Status)

Byte 0, bit 0: Mode Bit Override—When this position is a 1 the 'mode bit override' latch is set. When this latch is set, all interface mode settings, except 01 with high-priority, are overridden. See *Interface Modes of Operation* in Chapter 6.

Byte 0, bit 1: This bit is 0.

Byte 0, bit 2: Override Remember—When this position is a 1, the 'override remember' latch is set. See *Interface Modes of Operation* in Chapter 6.

Byte 0, bit 3: Scanner Enabled—When the scanner is enabled, this bit is 1. The bit is 0 when the scanner is disabled.

Byte 0, bit 4: Character Service Pending—This position indicates that the program has a character service request pending.

Byte 0, bits 5-7: These bits are 0.

Byte 1, bits 0-1: These bits are 0.

Byte 1, bit 2: LIB 1 Bit Clock Check—This bit is a 1 if a LIB-1 bit clock parity check has occurred.

Byte 1, bit 3: LIB 2 Bit Clock Check—This bit is a 1 if a LIB-2 bit clock parity check has occurred.

Byte 1, bit 4: LIB 3 Bit Clock Check—This bit is a 1 if a LIB-3 bit clock parity check has occurred.

Byte 1, bit 5: LIB 4 Bit Clock Check—This bit is a 1 if a LIB-4 bit clock parity check has occurred.

Byte 1, bit 6: LIB Select Check—This bit is a 1 if more than one LIB or more than one interface is addressed at the same time.

Byte 1, bit 7: CCU Outbus Check—This bit is a 1 when a CCU outbus parity check has been detected.

Type 1 Scanner Output Instructions

Output X'40' (Set Mode Bit Override and Override Remember)

This output is used to set the 'mode bit override' and the 'override remember' latches. Setting these latches causes the scanner to override all interface mode settings except 01 with high-priority. This instruction performs a function; and, therefore, the bit settings of the register specified by the R operand are ignored. See *Interface Modes of Operation* in Chapter 6.

Output X'41' (Start Scanner & Reset Bit Service L2 Request)

The Output X'41' instruction should be executed only when the scanner is stopped on an interface.

This instruction starts the scanner at the completion of the line interface servicing and resets the bit service request for the interface the scanner is addressing. It also resets the program level 2 bit service interrupt request. This instruction performs a function; and, therefore, the bit settings of the register specified by the R operand are ignored.

Output X'42' (Control A)

The Output X'42' instruction should be executed only when the scanner is stopped on an interface.

Byte 0, bits 0-5: These bits are unused.

Byte 0, bits 6-7: Mode bits—Each interface may be set to one of four level 2 interrupt modes as follows:

00 Disable level 2 interrupts—This mode disables all level 2 interrupts for a given interface.

01 Monitor for ring indicator or data set ready—This mode allows level 2 interrupts if 'ring indicator' or 'data set ready' becomes active for at least one bit time.

10 Monitor for receive data space—This mode allows a level 2 interrupt each time a space bit is received. An interrupt also occurs if 'data set ready' drops for at least one bit time.

11 Enable level 2 interrupts—This mode allows all level 2 interrupts to be enabled for a given interface.

For further discussion on the use of the mode bit setting, refer to *Interface Modes of Operation* in Chapter 6.

Byte 1, bit 0: Bit Service Priority—This bit determines the service priority for the interface the scanner is addressing. A 1 in this position sets a low priority; a 0 sets a high priority.

Byte 1, bit 1: Diagnostic Mode—A 1 in this position sets the line interface to the diagnostic mode, and a 0 sets it to the normal read/write mode. See *Diagnostic Wrap* and *Modem Self Test* in Chapter 6 for the description of operation in this mode.

Byte 1, bit 2: Data Terminal Ready (DTR)—This bit activates or deactivates the 'data terminal ready' line from the line interface to the modem. A 1 activates the line, and a 0 deactivates it.

Byte 1, bit 3: Synchronous Bit Clock—A 1 in this position sets the line interface for synchronous clocking, and a 0 sets it for start-stop clocking.

Byte 1, bit 4: External Clock—This bit position selects modem (data set) clocking, or business machine (data terminal equipment) clocking. 1 = modem, and 0 = business machine.

Byte 1, bit 5: Data Rate Selector—A 1 in this position selects the high data rate for the attached modem, and a 0 selects the low data rate.

Byte 1, bits 6-7: Oscillator Select Bits—These two bit positions select which one of the four *internal bit rates* available in the Type 1 Scanner is to be assigned to the line interface.

The internal bit rates available are determined by the bit clocks that have been installed in the Type 1 Scanner in conjunction with the line interface base types and line sets. See the description of *Business Machine Clocks* in Chapter 6.

Autocall Interface Bits for Output X'42'

The Output X'42' instruction for autocall is the same as for *line interface* except that byte 1, bits 1-7 are ignored.

Note: *The lowest speed oscillator is always assigned to autocall interfaces.*

Output X'43' (Control B)

The Output X'43' instruction should be executed only when the scanner is stopped on an interface.

Byte 0, bits 0-7: These bits are unused.

Byte 1, bits 0-3: These bits are unused.

Byte 1, bit 4: Transmit/Receive Mode—A 1 in this position sets the line interface to transmit mode; a 0 sets it to receive mode.

Byte 1, bit 5: New Sync—A 1 in this position activates the 'new sync' line to the modem; a 0 deactivates the line.

Byte 1, bit 6: Request to Send (RTS)—A 1 in this position activates the 'request to send' line to the modem; a 0 deactivates the line.

Byte 1, bit 7: Send Data—A 1 in this position sends a mark to the line interface 'send data buffer'; a 0 sends a space.

Autocall Interface Bits for Output X'43'

Byte 0, bits 0-7: These bits are unused.

Byte 1, bits 0-1: These bits are unused.

Byte 1, bit 2: CRQ—A 1 in this position activates the 'call request' line to the autocall interface; a 0 deactivates the line.

Byte 1, bit 3: DPR—A 1 in this position activates the 'digit present' line to the autocall interface; a 0 deactivates the line.

Byte 1, bits 4-7: These bit positions represent the dial digit in BCD form.

Output X'44' (General Control)

Byte 0, bits 0-7: These bits are unused.

Byte 1, bit 0: Diagnostic Bit Service—A 1 in this position sets a latch that causes continuous bit service requests for all 64 line interfaces (used and unused). A 0 resets the latch.

Byte 1, bit 1: This bit is unused.

Byte 1, bit 2: Reset Mode Bit Override—A 1 in this position resets the 'mode bit override' latch as described in the *Interface Modes of Operation* in Chapter 6.

Byte 1, bit 3: Reset Override Remember—A 1 in this position resets the 'override remember' latch in the Type 1 Scanner. See *Interface Modes of Operation* in Chapter 6.

Byte 1, bit 4: Reset Character Service Pending—A 1 in this position resets the 'character service pending' latch set by Output X'46'.

Byte 1, bit 5: Reset Level 1 Checks—A 1 in this position resets all level 1 check conditions resulting from the Type 1 Scanner.

Byte 1, bit 6: Reset Feedback Check—A 1 in this position resets the 'feedback error' latch.

Byte 1, bit 7: Reset Bit Overrun/Underrun—A 1 in this position resets the 'bit overrun/underrun' latch for the interface the scanner is addressing.

Output X'45' (Scanner Control)

This instruction may be used to disable one or more LIBs. A LIB should be disabled only when it is causing solid errors or solid level 1 interrupts.

Byte 0, bit 0: This bit is unused.

Byte 0, bit 1: Set Scanner Enable—A 1 in this position sets the 'scanner enable' latch, allowing normal operation of the scanner.

Byte 0, bit 2: Reset Scanner Enable—A 1 in this position resets the 'scanner enable' latch. This disables the scanner, prevents any further interrupts, forces all interfaces to be reset, and allows no bit services.

A 1 in both bit 1 and bit 2 of this byte is invalid, and the result is unpredictable. The scanner may be either enabled or disabled.

Note: *In a 3704, when this bit is on, all LIBs are forced to and held in the enabled state as long as the scanner is disabled, regardless of the setting of the Output X'45' instruction.*

Byte 0, bit 3: This bit is unused.

Byte 0, bit 4: Disable LIB 1—A 1 in this position disables L1 and L2 interrupts and bit service from LIB 1. A 0 resets the disable condition.

Byte 0, bit 5: Disable LIB 2—A 1 in this position disables L1 and L2 interrupts and bit service from LIB 2. A 0 resets the disable condition.

Byte 0, bit 6: Disable LIB 3—A 1 in this position disables L1 and L2 interrupts and bit service from LIB 3. A 0 resets the disable condition.

Byte 0, bit 7: Disable LIB 4—A 1 in this position disables L1 and L2 interrupts and bit service from LIB 4. A 0 resets the disable condition.

Byte 1, bits 0-7: These bits are unused.

Output X'46' (Set Character Service)
The Output X'46' instruction sets the 'character service pending' latch. It also starts the scanner and resets the level 2 bit service interrupt request. This instruction performs a function, and therefore, the bit settings of the register specified by the R operand are ignored.

Output X'47' (Force Bit Service Request)
This instruction is executed to force one level 2 bit service interrupt request. The storage address associated with the interface that is to cause the interrupt must be loaded into the register specified by the R operand. When this instruction is executed, the scanner determines the interface address from the storage address and requests a level 2 interrupt for that interface.

Programming Note
Forced bit service cannot be stacked. If an Output X'47' is executed before the previous Output X'47' has been serviced, the second address overlays the first address.

Byte 0, bits 0-5: These bits are unused.

Byte 0, bits 6-7, Byte 1, bits 0-3: Interface Address—These bit positions are loaded with the storage address associated with the interface that is to cause a bit service interrupt.

Byte 1, bits 4-7: These bits are unused.

Type 2 Scanner Input Instructions

Input X'40' (Interface Address)
This instruction obtains the line interface address from the ABAR in the attachment base. Conditions that set the ABAR are described in the *I/O Programming Considerations* section in Chapter 7. When this instruction is executed, the interface address from the ABAR is placed in byte 0, bit 6 through byte 1, bit 6 of the register specified by the R operand. Byte 0, bit 4 is always set to 1. The other register bit positions are set to 0.

Input X'43' (Check Register)
This instruction obtains the status of the check register in the scanner. Since there can be up to four Type 2 scanners, the check register selected is determined by the interface address in the ABAR at the time of instruction execution.

When this instruction is executed, the check register bits are placed in the register specified by the R field.

Programming Note
If any of the check register bits in the scanner are set to 1, the Type 2 Scanner L1 interrupt request is set.

Byte 0, bit 0: LIB 1 Bit Clock Check—This bit is set to 1 if a LIB position 1 bit clock control check is detected by the Type 2 Scanner; otherwise, it is set to 0.

Byte 0, bit 1: LIB 2 Bit Clock Check—Same as above.

Byte 0, bit 2: LIB 3 Bit Clock Check—Same as above.

Byte 0, bit 3: LIB 4 Bit Clock Check—Same as above.

Byte 0, bit 4: LIB 5 Bit Clock Check—Same as above.

Byte 0, bit 5: LIB 6 Bit Clock Check—Same as above.

Byte 0, bit 6: LIB Select Check—This bit is set to 1 if the Type 2 Scanner has detected a LIB address parity check on either LIB string 1 (LIB pos 1, 2, or 3) or LIB string 2 (LIB pos 4, 5, or 6); otherwise, it is set to 0.

Byte 0, bit 7: ICW Input Register Check—This bit is set to 1 if the Type 2 Scanner has detected a parity error in the ICW input register; otherwise, it is set to 0.

Byte 1, bit 0: ICW Work Register Check—This bit is set to 1 if the Type 2 Scanner has detected a parity error in the ICW work register; otherwise, it is set to 0.

Byte 1, bit 1: Priority Register Available Check—This bit is set to 1 if the Type 2 Scanner has detected even parity on one of the four *priority register available* lines; otherwise, it is set to 0. These four lines from the attachment base are parity-checked in the Type 2 Scanner.

Byte 1, bit 2: CCU Outbus Check—This bit is set to 1 if the Type 2 Scanner has detected even parity on the CCU Outbus. Otherwise, it is set to 0.

Byte 1, bit 3: Line Address Bus Check—This bit is set to 1 if the Type 2 Scanner has detected a scanner buffer address register bus parity error during program addressing (refer to the *Program Addressing* section in Chapter 7); otherwise, it is set to 0.

Byte 1, bits 4-7: These bits are 0.

Input X'44' (ICW Input Register–Bits 0-15)
This instruction determines the state of the 'secondary control field' (SCF) and the 'parallel data field' (PDF) in the ICW that is set in the ICW input register. The interface address in the ABAR selects the proper scanner. When this instruction is executed, the contents of the ICW input register, bit positions 0-15, are placed in the register specified by the R field. Refer to *I/O Programming Considerations* for conditions that set the ICW input register. The *Interface Control Word Format* and the *SDLC* sections of Chapter 7 describe the SCF and PDF fields and their bit definitions.

Input X'45' (ICW Input Register–Bits 16-31)
This instruction determines the state of the LCD and PCF fields and SDF bits 0-7 of the ICW that is set in the ICW input register. The interface address in the ABAR selects the proper scanner. When this instruction is executed, the contents of the ICW input register bit positions 16-31 are placed in the register specified by the R field. Refer to *I/O Programming Considerations* in Chapter 7 for conditions that set the ICW input register. The LCD, PCF, and SDF fields and bit definitions are described in the *Interface Control Word Format* and the *SDLC* sections of Chapter 7.

Programming Note
This input does not contain the complete serial data field. Only bits 0-7 of the field are available with this input. The remainder of the SDF (bits 8-9) are accessed by the Input X'47' instruction.

Input X'46' (Display Register)
This instruction determines the state of the display register in the Type 2 Scanner selected by the interface address in ABAR. When this instruction is executed, the contents of the Type 2 Scanner display register are placed in the register specified by the R field.

The hardware, because of the *display request* (ICW bit 38), can cause status information for a particular interface to be placed into the Type 2 Scanner display register when the interface is scanned. Input X'46' can then be used to examine this status information. Refer to Output X'43', which must be used to set/reset the display request bit in the ICW.

Before accessing the display register with an Input X'46', the program must ensure that enough time has elapsed to guarantee that the interface has been scanned at least once after it set the display request bit in the ICW.

Byte 0, bit 0: Clear To Send—This bit is set to 1 if the 'clear to send' line from the modem is on, or if the diagnostic wrap forces 'clear to send' on; otherwise, it is set to 0.

Byte 0, bit 1: Ring Indicator—This bit is set to 1 if the 'ring indicator' line from the modem is on; otherwise, it is set to 0.

Byte 0, bit 2: Data Set Ready—This bit is set to 1 if the 'data set ready' line from the modem is on, or if the diagnostic wrap forces 'data set ready' on; otherwise, it is set to 0.

Byte 0, bit 3: Receive Line Signal Detector—This bit is set to 1 if the 'receive line signal detected' line from the modem is on, or if the diagnostic wrap state forces 'receive line signal detected' on; otherwise, it is set to 0.

Byte 0, bit 4: Receive Data Bit Buffer—This bit is set to 1 if the line interface receive data buffer contains a mark (1). If the buffer contains a space (0), this bit is set to 0.

Byte 0, bit 5: Diagnostic Wrap Mode—This bit is set to 1 if the line interface is in diagnostic wrap state; otherwise, it is set to 0.

Byte 0, bit 6: Bit Service Request—This bit is set to 1 if the line interface 'bit service request' is on; otherwise, it is set to 0. Normally, bit service must be on before the Type 2 Scanner can access the line associated with the interface address or initiate transmit or receive operations.

Byte 0, bit 7: This bit is 0.

Byte 1, bits 0-7: These bits are 0.

Autocall Interface Bits for Input X'46'

Byte 0, bit 0: Abandon Call and Retry—This bit is set to 1 if the autocall unit 'abandon call and retry' (ACR) is active; otherwise it is set to 0.

Byte 0, bit 1: Present Next Digit—This bit is set to 1 if the autocall unit 'present next digit' (PND) is active; otherwise, it is set to 0.

Byte 0, bit 2: Data Line Occupied—This bit is set to 1 if the autocall unit 'data line occupied' (DLO) is active; otherwise, it is set to 0.

Byte 0, bit 3: Power Indicator—This bit is set to 1 if the autocall unit 'power indicator' (PWI) is active; otherwise, it is set to 0.

Byte 0, bit 4: This bit is 0.

Byte 0, bit 5: Call Originating Status—This bit is set to 1 if the autocall unit 'call originating status' (COS) is active; otherwise, it is set to 0.

Byte 0, bit 6: Bit Service Request—This bit is the same as for line interface.

Byte 0, bit 7: This bit is 0.

Byte 1, bits 0-7: These bits are 0.

Input X'47' (ICW Input Register–Bits 32-45)
This instruction determines the state of SDF bits 8-9, the ones counter (SDLC), the last line state bit (SDLC), the display request bit, the L2 interrupt pending bit, priority bits 1-2, and the NRZI control bit (SDLC). The interface

address in the ABAR selects the proper scanner and associated ICW. When this instruction is executed, the contents of the ICW input register, bit positions 32 through 45, are placed in the register specified by the R operand. Byte 0, bit 7 and byte 1, bits 0, 6, and 7 are set to 0. See *I/O Programming Considerations* in Chapter 7 for conditions that cause the ICW input register to be set. For an interpretation of these bits, see the *Interface Control Word Format* and *SDLC* sections in Chapter 7.

Type 2 Scanner Output Instructions

Output X'40' (Interface Address)
This instruction sets an interface address in the attachment buffer address register (ABAR) of the Type 2 Attachment Base. When this instruction is executed, byte 0, bit 6 through byte 1, bit 6 in the register specified by the R operand are placed in the ABAR.

The interface address, placed in ABAR, selects the Type 2 Scanner and the ICW associated with that address. When accessed, the ICW is placed in the ICW work register by the scanner hardware. If Output X'40' is executed in program levels 3 or 4, the contents of the ICW work register are placed in the ICW input register where they are available for access by Inputs X'44', X'45', and X'47'.

Output X'41' (Address Substitution Control)
This instruction sets the substitution control register in the Type 2 Attachment Base. See *Address Substitution* in Chapter 7 for a description and coding of the substitution control bits.

Execution of Output X'41' causes byte 1, bits 2-5 from the register specified by R to be placed into the substitution control register.

Programming Note
If address substitution is not used, Output X'41' *must* be executed with byte 1, bits 2-5 off in the register specified by R.

Output X'42' (Scan Limit Control)
This instruction sets the 'scan limit' in the selected Type 2 Scanner. At least one Output X'42' must be executed for each Type 2 Scanner available. The scanner selected is determined by the interface address in the attachment buffer address register (ABAR) of the Attachment Base at the time of execution.

When this instruction is executed, byte 1, bits 6 and 7 in the register specified by the R operand are placed in the 'scan limit' latches of the scanner.

Byte 0, bits 0-7: These bits are unused.

Byte 1, bits 0-5: These bits are unused.

Byte 1, bits 6-7: Scan Limit Select Bits 0 and 1—These bits are set as follows to indicate the desired scan limit for each Type 2 Scanner.

Bit 6 7	*Scan Limit*
0 1	8
1 1	16
1 0	48
0 0	96

Output X'43' (Control)
This instruction sets or resets various control functions in a Type 2 Scanner. The Type 2 Scanner is selected by the interface address in the attachment buffer address register (ABAR) of the Attachment Base. When this instruction is executed, the bit configuration in the register specified by the R field determines which control functions are set or reset.

Byte 0, bit 0: Set Function—A 1 in this position causes the functions of byte 0, bits 2-7 and byte 1, bits 0-7 of this output to be set when the corresponding bit is 1. This bit should not be 1 if byte 0, bit 1 is 1.

Byte 0, bit 1: Reset Function—A 1 in this position causes the functions of byte 0, bits 2-7 and byte 1, bits 0-7 of this output to be reset when the corresponding bit is 1. This bit should not be 1 if byte 0, bit 0 is 1.

Byte 0, bit 2: Display Request—A 1 in this position causes the display request (ICW bit 38) to be set or reset according to byte 0, bits 0 and 1.

Byte 0, bits 3-6: These bits are unused.

Byte 0, bit 7: Disable LIB Position 1—A 1 in this position causes LIB position 1 of the addressed scanner to be disabled or enabled. When this bit is on and byte 0, bit 0 (set function) is on, the LIB position is disabled. When this bit is on and byte 0, bit 1 (reset function) is on, the LIB position is enabled.

Byte 1, bit 0: Disable LIB Position 2—This bit is associated with LIB position 2 and functions the same as byte 0, bit 7.

Byte 1, bit 1: Disable LIB Position 3—This bit is associated with LIB position 3 and functions the same as byte 0, bit 7.

Byte 1, bit 2: Disable LIB Position 4—This bit is associated with LIB position 4 and functions the same as byte 0, bit 7.

Byte 1, bit 3: Disable LIB Position 5—This bit is associated with LIB position 5 and functions the same as byte 0, bit 7. This bit should be set for a Type 2 Scanner-1.

Byte 1, bit 4: Disable LIB Position 6—This bit is associated with LIB position 6 and functions the same as byte 0, bit 7. This bit should be set for a Type 2 Scanner-1.

Byte 1, bit 5: Type 2 Scanner Level 1 Request—This bit is for diagnostic purposes. A 1 in this position along with the set function (byte 0, bit 0) causes a level 1 interrupt request and sets the following check latches.

- LIB positions 1-6 Bit Clock Checks.
- LIB Select Check.
- ICW Input Register check.
- ICW Work Register check.
- Priority Register Available check.
- CCU Outbus check.
- LINEADDBUS check.

A 1 in this position along with the reset function (byte 0, bit 1) resets the level 1 interrupt request and resets the above check latches.

Byte 1, bit 6: Disable Interrupt Requests—This bit is for diagnostic purposes. A 1 in this position along with the set function (byte 0, bit 0) sets the 'power-on-reset' latch and resets the scanners and LIBs. A 1 in this position along with the reset function (byte 0, bit 1) resets the 'power-on-reset' latch, thereby ending the reset state.

Programming Note
During any 'power-on' sequence, the POR latch is set in each Type 2 Scanner. The program *must* reset this latch with an Output X'43' instruction for each Type 2 Scanner before the scanner can be initialized. Also, a minimum of two scan periods (307.2 microseconds) is required between setting and resetting this bit to ensure completion of the reset function.

Byte 1, bit 7: This bit is unused.

Output X'44' (ICW Bits 0-15)
This instruction resets secondary control field (SCF) bits 0-3 and 5 (bit 5 is for SDLC use only), and sets or resets bits 6-7 of the SCF. It is also used to set or reset the parallel data field (PDF). The PDF field is used as a character buffer. The interface address in the attachment buffer address register (ABAR), located in the Type 2 Attachment Base, selects the Type 2 Scanner and the ICW associated with this address.

When this instruction is executed, the bit configurations in the register specified by the R field determine what bits are to be set, reset, or left unchanged in ICW bits 0-3 and 5-15. Refer to the *Secondary Control Field* of the ICW (in Chapter 7) for a description of SCF bits (byte 0, bits 0-7). See *ICW Format* for the PDF as it relates to various LCD states. See the *SDLC* section of Chapter 7 for Synchronous Data Link Control descriptions of the SCF bits.

Byte 0, bit 0: When this bit is a 1, ICW bit 0 (stop bit check, receive break, or SDLC abort) is reset to 0; otherwise, it is unchanged.

Byte 0, bit 1: When this bit is a 1, ICW bit 1 (service request) is reset to 0; otherwise, it is unchanged.

Byte 0, bit 2: If this bit is a 1, ICW bit 2 (character overrun/underrun) is reset to 0; otherwise, it is unchanged.

Byte 0, bit 3: If this bit is a 1, ICW bit 3 (modem check) is reset to 0; otherwise, it is unchanged.

Byte 0, bit 4: This bit is unused.

Byte 0, bit 5: If this bit is a 1, ICW bit 5 (SDLC flag detection/disable zero-insert remembrance) is reset to 0; otherwise, it is unchanged.

Byte 0, bit 6: If this bit is a 1, ICW bit 6 (program flag) is set to 1; otherwise, it is reset to 0.

Byte 0, bit 7: If this bit is a 1, ICW bit 7 (pad flag or SDLC disable zero-insert control) is set to 1; otherwise, it is reset to 0.

Byte 1, bits 0-7: The settings of these bits are placed into the ICW bit positions 8-15 (PDF bits 0-7).

Output X'45' (ICW Bits 16-23)
This instruction sets the bits of the line control definer (LCD) and the primary control field (PCF) in the ICW. When this instruction is executed, byte 1, bits 0-7 in the register specified by the R field are placed in the LCD and PCF fields. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a detailed description of these bits, see the *Interface Control Word Format* section in Chapter 7. For a description of these bits when used for SDLC, refer to the *SDLC* section of Chapter 7.

Byte 0, bits 0-7: These bits are unused.

Byte 1, bits 0-3: The settings of these bits are placed into the ICW bit positions 16-19 (LCD bits 0-3).

Byte 1, bits 4-7: The settings of these bits are placed into the ICW bit positions 20-23 (PCF bits 0-3).

Output X'46' (ICW Bits 24-33)
This instruction sets the bits of the serial data field (SDF) in the ICW. When this instruction is executed, byte 0, bits 6-7 and byte 1, bits 0-7 in the register specified by the R field are placed in the SDF of the ICW. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a detailed description of these bits, see the *Interface Control Word Format* section in Chapter 7.

Byte 0, bit 0: NRZI Control (SDLC only)—The setting of this bit is placed into ICW bit position 44, which is used by SDLC to control the mode of data transmission. See the *SDLC* section of Chapter 7 for a description of NRZI mode.

Byte 0, bits 1-5: These bits are unused.

Byte 0, bits 6-7: The settings of these bits are placed into the ICW bit positions 24-25 (SDF bits 0 and 1).

Byte 1, bits 0-7: The settings of these bits are placed into the ICW bit positions 26-33 (SDF bits 2-9).

Output X'47' (ICW Bits 34-37 and 39-43)
This instruction sets the state of ICW bits 34-37 and 39-43. Execution of this instruction places bits from the register specified by R into the appropriate ICW bit positions. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a detailed description of these bits, see the *Interface Control Word Format* section in Chapter 7. For a description of these bits when used for SDLC, refer to the *SDLC* section of Chapter 7.

Byte 0, bits 0-5: These bits are unused.

Byte 0, bit 6: Ones Counter 0—The setting of this bit is placed in ICW bit position 34. ICW bit positions 34-36 form the SDLC ones counter.

Byte 0, bit 7: Ones Counter 1—The setting of this bit is placed in ICW bit position 35.

Byte 1, bit 0: Ones Counter 2—The setting of this bit is placed in ICW bit position 36.

Byte 1, bit 1: Last Line State (SDLC)—This bit is set by hardware, but it can be set and reset by this output.

Byte 1, bit 2: This bit is unused.

Byte 1, bits 3-4: The settings of these bits are placed into the ICW bit positions 39-40. (These bits are reserved and should be 0.)

Byte 1, bit 5: L2 Interrupt Pending—A 1 in this position sets ICW bit 41, which forces an interrupt for a particular interface without requiring the interface to have a service request set. A 0 leaves the ICW bit unchanged.

Byte 1, bits 6-7: The settings of these bits are placed into the ICW bit positions 42-43 (priority bits 1 and 2).

Type 3 and Type 3HS Scanner Input Instructions

Input X'40' (Interface Address)
This instruction obtains the line interface address from the ABAR in the attachment base. Conditions that set the ABAR are described in the *I/O Programming Considerations* section in Chapter 8. When this instruction is executed, the interface address from the ABAR is placed in byte 0, bit 6 through byte 1, bit 6 of the register specified by the R operand. Byte 0, bit 4 is always set to 1. The other register bit positions are set to 0.

Input X'41' (High Speed Select)

Type 3 Communication Scanner: This instruction determines the setting of the high speed select register. The contents of this register are placed in the register specified by the R field. Refer to *Type 3 or Type 3HS Scanner Addressing* in Chapter 8 for the meanings of the high speed select bits.

Type 3HS Communication Scanner: This instruction obtains ICW bits 17.0 and 17.1 from byte 1, bits 0 and 1 of a selected general register. Bits 17.0 and 17.1 of the ICW are an extension of the ICW controls field. These bits increase the number of elements in the PDF array from 8 to 16. ICW bits 17.0 and 12.0-12.3 represent, respectively, cycle steal PDF array pointer weights of 16, 8, 4, 2, and 1. ICW bits 17.1 and 12.4-12.7 represent, respectively, PDF array pointer weights of 16, 8, 4, 2, and 1. An Input X'41' instruction must be preceded by an Output X'40' instruction to obtain the contents of the ICW.

Input X'42' (DBAR/Check Register 0)
This instruction determines the state of check register 0, the diagnostic buffer address register (DBAR) and the upper scan limit bits. The contents of these registers and bits are placed in the register specified by the R field. For a Type 3HS scanner, byte 1, bits 6 and 7 are insignificant and unpredictable.

Input X'43' (Check Register 1)
This instruction obtains the status of the check register 1 in the scanner. Since there can be up to four Type 3 scanners, the check register selected is determined by the interface address in the ABAR at the time of instruction execution.

When this instruction is executed, the check register bits are placed in the register specified by the R field.

Programming Note
If any of the check register bits in the scanner are set to 1, the Type 3 Scanner L1 interrupt request is set.

Byte 0, bit 0: LIB 1 Bit Clock Check–This bit is set to 1 if a LIB position 1 bit clock control check is detected by the Type 3 Scanner; otherwise, it is set to 0.

Byte 0, bit 1: LIB 2 Bit Clock Check–Same as above.

Byte 0, bit 2: LIB 3 Bit Clock Check–Same as above.

Byte 0, bit 3: LIB 4 Bit Clock Check–Same as above.

Byte 0, bits 4 and 5: These bits are 0.

Byte 0, bit 6: LIB Select Check–This bit is set to 1 if more than one LIB was selected or more than one line (or no line) was accessed on the selected LIB, or a line was accessed on a LIB that was not selected.

Byte 0, bit 7: ICW Input Register Check–This bit is set to 1 if the Type 3 Scanner has detected a parity error in the ICW input register; otherwise, it is set to 0.

Byte 1, bit 0: ICW Work Register Check 1–This bit is set to 1 if the Type 3 Scanner has detected a parity error in the ICW work register; otherwise, it is set to 0.

Byte 1, bit 1: Priority Register Available Check–This bit is set to 1 if the Type 3 Scanner has detected even parity on one of the four *priority register available* lines; otherwise, it is set to 0. These four lines from the attachment base are parity-checked in the Type 3 Scanner.

Byte 1, bit 2: CCU Outbus Check–This bit is set to 1 if the Type 3 Scanner has detected even parity on the CCU Outbus. Otherwise, it is set to 0.

Byte 1, bit 3: Line Address Bus Check–This bit is set to 1 if the Type 3 Scanner has detected a scanner buffer address register bus parity error during program addressing (refer to the *Program Addressing* section in Chapter 8); otherwise, it is set to 0.

Byte 1, bit 4: Bad Inbound CS Data–This bit is set to 1 if the CCU detects a parity check on the data being transferred to storage via a cycle steal operation.

Byte 1, bit 5: CSAR Check–This bit is set to 1 if the CCU detects an even parity check in the CS address register.

Byte 1, bit 6: Address Exception–This bit is set to 1 if the CCU detects that the address in the CSAR exceeds the CCU storage size. The bit is set to 0 if byte 1, bit 5 is 1.

Byte 1, bit 7: ICW Work Register 0 Check–This bit is set to 1 if the CCU detects an even parity check from the ICW work register for byte 0 or 14.

Input X'44' (ICW Byte 0 and PDF Array)
This instruction determines the state of the secondary control field (SCF) and the parallel data field (PDF) from the PDF array. The interface address in the ABAR selects the proper scanner. When this instruction is executed, the contents of the ICW input register, byte 0, and the PDF input register are placed in the register specified by the R field. Refer to *I/O Programming Considerations* in Chapter 8 for conditions that set the ICW input register. The *Interface Control Word Format* section of Chapter 8 describes the SCF and PDF fields and their bit definitions.

Input X'45' (ICW Bytes 2 and 3)
This instruction may be used to determine the state of the LCD, basic PCF, and SDF fields of the ICW that is set in the ICW input register. The interface address in the ABAR selects the proper scanner. When this instruction is executed the contents of the ICW input register bit positions bytes 2 (LCD, PCF) and 3 (SDF) are placed in the register specified by the R field. Refer to *I/O Programming Considerations* in Chapter 8 for conditions that set the ICW input register. The LCD, PCF, and SDF fields and bit definitions are described in the *Interface Control Word Format* section of Chapter 8.

Programming Note
This input instruction does not contain the complete serial data field. Only bits 0-7 of the field are available with this input. The remainder of the SDF (bits 8-9) is accessed by the Input X'47' instruction.

Input X'46' (Display Register)
This instruction may be used to determine the state of the display register in the Type 3 Scanner selected by the interface address in ABAR. When this instruction is executed, the contents of the scanner display register are placed in the register specified by the R field.

The hardware, because of the *display request* (ICW bit 4.6), can cause status information for a particular interface to be placed into the Type 3 Scanner display register when the interface is scanned. Input X'46' can then be used to examine this status information. Refer to Output X'43', which must be used to set/reset the display request bit in the ICW.

Before accessing the display register with an Input X'46', the program must ensure that enough time has elapsed to guarantee that the interface has been scanned at least once after it set the display request bit in the ICW.

Line Interface Bits for Input X'46'

Byte 0, bit 0: Clear to Send–This bit is set to 1 if the 'clear to send' line from the modem is on, or if the diagnostic wrap forces 'clear to send' on; otherwise, it is set to 0.

Byte 0, bit 1: Ring Indicator–This bit is set to 1 if the 'ring indicator' line from the modem is on; otherwise, it is set to 0.

Byte 0, bit 2: Data Set Ready–This bit is set to 1 if the 'data set ready' line from the modem is on, or if the diagnostic wrap forces 'data set ready' on; otherwise, it is set to 0.

Byte 0, bit 3: Receive Line Signal Detector–This bit is set to 1 if the 'receive line signal detected' line from the modem is on, or if the diagnostic wrap state forces 'receive line signal detected' on; otherwise, it is set to 0.

Byte 0, bit 4: Receive Data Bit Buffer–This bit is set to 1 if the line interface receive data buffer contains a mark (1). If the buffer contains a space (0), this bit is set to 0.

Byte 0, bit 5: Diagnostic Wrap Mode–This bit is set to 1 if the line interface is in diagnostic wrap state; otherwise, it is set to 0.

Byte 0, bit 6: Bit Service Request–This bit is set to 1 if the line interface 'bit service request' is on; otherwise, it is set to 0. Normally, bit service must be on before the Type 3 Scanner can access the line associated with the interface address or initiate transmit or receive operations.

Byte 0, bit 7: ICW Test Mode–This bit is set to 1 if the diagnostic mode latch is set by an Output X'43' instruction or by an 'ICW and array reset.'

Byte 1, bits 0-7: These bits are 0.

Autocall Interface Bits for Input X'46'

Byte 0, bit 0: Abandon Call and Retry–This bit is set to 1 if the autocall unit 'abandon call and retry' (ACR) is active; otherwise it is set to 0.

Byte 0, bit 1: Present Next Digit–This bit is set to 1 if the autocall unit 'present next digit' (PND) is active; otherwise, it is set to 0.

Byte 0, bit 2: Data Line Occupied–This bit is set to 1 if the autocall unit 'data line occupied' (DLO) is active; otherwise, it is set to 0.

Byte 0, bit 3: Power Indicator–This bit is set to 1 if the autocall unit 'power indicator' (PWI) is active; otherwise, it is set to 0.

Byte 0, bit 4: This bit is 0.

Byte 0, bit 5: Call Originating Status—This bit is set to 1 if the autocall unit 'call originating status' (COS) is active; otherwise, it is set to 0.

Byte 0, bit 6: Bit Service Request—This bit is the same as for line interface.

Byte 0, bit 7: ICW Test Mode—This bit is the same as for a line interface.

Byte 1, bits 0-7: These bits are 0.

Input X'47' (ICW Bytes 4 and 5)
This instruction is used to determine the state of the bits of ICW bytes 4 and 5: SDF bits 8 and 9, interval timer/ones counter, timeout control/last line state, display request, level 2 interrupt pending, priority select 1 and 2, transparent text/NRZI control, diagnostic 1 and 2, and external modem check bits. The interface address in the ABAR selects the proper scanner and the associated ICW. This instruction places the contents of the ICW input register, bytes 4 and 5, in the register specified by the R field. See *I/O Programming Considerations* in Chapter 8 for conditions that cause the ICW input register to be set. For an interpretation of these bits, see *Interface Control Word Format* in Chapter 8.

Input X'48' (ICW Bytes 6 and 7)
This instruction is used to determine (1) the contents of the cycle steal byte count and cycle steal extended address bits X.4, X.5, X.6 and X.7, (2) the setting of the cycle steal control bits, and (3) whether ETB, ETX, or ENQ characters are present in data. This instruction places the contents of ICW input register bytes 6 and 7 in the register specified by the R field.

Input X'49' (ICW Bytes 8 and 9)
This instruction is used to determine the contents of the cycle steal address register (CSAR). The instruction places the contents of ICW input register bytes 8 and 9 in the register specified by the R field.

Input X'4A' (ICW Bytes 10 and 11)
This instruction is used to determine the contents of the old block check characters (BCC). The instruction places the contents of ICW input register bytes 10 and 11, containing the 16-bit accumulation for SDLC or BSC data, in the register specified by the R field.

Input X'4B' (ICW Byte 16)
This instruction is used to determine the state of the extended PCF and the new sync, data terminal ready, and OLT diagnostic bits. The instruction places the contents of ICW input register byte 16 in the register specified by the R field.

Input X'4C' (PDF Array Bits 0-10)
This instruction is used to determine the contents of bits 0-10 of the PDF currently selected by the PDF array pointer (ICW bits 12.4-12.7). The instruction places the contents of the PDF input register (previously loaded from the PDF) in the register specified by the R field. Refer to *PDF Array Format* in Chapter 8 for the meanings of the PDF array bits.

Input X'4E' (ICW Bytes 12 and 13)
This instruction is used to determine the PDF array address pointed to by the cycle steal PDF array pointer and the PDF array pointer, and to determine the state of the sequence 0, 1, and 2, RTS turnaround control, and cycle steal message counter bits. The interface address in the ABAR selects the proper scanner and the associated ICW. The instruction places the contents of the ICW input register bytes 12 and 13 in the register specified by the R field. For ICW controls extended (ICW bits 17.0 and 17.1), used for Type 3HS Scanner operations, refer to *Input X'41' (High Speed Select)* earlier in Appendix C.

Byte 0, bits 0-3: Cycle Steal PDF Array Pointer—These bits contain the address of the current PDF from which or to which data is being transferred via cycle steal operation.

Byte 0, bits 4-7: PDF Array Pointer—These bits contain the address of the current PDF from which or to which data is being transferred by the control program.

Byte 1, bits 0-1: Sequence 0 and 1—These bits are used by the scanner in determining the appropriate action to perform upon receiving or transmitting BSC and SDLC control sequences within message data.

Byte 1, bit 2: Request-to-Send Turnaround Control—This bit is set or reset by the control program to determine whether the RTS lead in the modem interface is to remain active or be deactivated when a line turnaround from transmit state to receive state occurs.

Byte 1, bit 3: Sequence 2—This bit is used by the scanner (1) in determining the action to take upon receiving an SDLC flag character under certain conditions, or (2) to indicate that character phase has been entered, for a BSC line.

Byte 1, bits 4-5: These bits are 0.

Byte 1, bits 6-7: Message Counter—These bits are used by the Type 3 Scanner in keeping track of multiple SDLC messages that may be queued in the PDF array during a receive operation.

Input X'4F' (ICW Bytes 14 and 15)

This instruction is used to determine the state of the status exception and BSC/SDLC control status fields of the ICW. Refer to *Interface Control Word Format* in Chapter 8 for the meanings of the bits of these fields. The instruction places the contents of the ICW input register bytes 14 and 15 in the register specified by the R field.

Type 3 and Type 3HS Scanner Output Instructions

Output X'40' (Interface Address)

This instruction is used to set an interface address in the attachment buffer address register (ABAR) of the Type 2 Attachment Base. When this instruction is executed, byte 0, bit 6 through byte 1, bit 6 in the register specified by the R operand are placed in the ABAR.

The interface address, placed in ABAR, selects the Type 3 Scanner and the ICW associated with that address. When accessed, the ICW is placed in the ICW work register by the scanner hardware. If Output X'40' is executed in program levels 3 or 4, the contents of the ICW work register are placed in the ICW input register where they are available for access by Inputs X'44', X'45', and X'47'.

Output X'41' (Scan Substitution Control)

This instruction must be used to set the substitution control register in the Type 2 Attachment Base. See *Address Substitution* in Chapter 8 for a description and coding of the substitution control bits.

Execution of Output X'41' causes byte 1, bits 2-5 from the register specified by R to be placed into the substitution control register.

Programming Notes:

1. If the Type 3HS Communication Scanner is used, Output X'41' must be executed with byte 1, bits 2-5 off in the register specified by R. Byte 0, bits 0 - 7 and byte 1, bits 0, 1, 6, and 7 of the Output X'4E' register are ignored.
2. If address substitution is not used for a Type 3 Communication Scanner, Output X'41' must be executed with byte 1, bits 2-5 off in the register specified by R.

Output X'42' (DBAR/Scan Limit Control)

This instruction must be used to set the diagnostic buffer address register (DBAR) and the scan limit in the selected Type 3 Scanner. At least one Output X'42' must be executed for each Type 3 Scanner available. The scanner selected is determined by the interface address in the attachment buffer address register (ABAR) of the Attachment Base at the time of execution.

When this instruction is executed, byte 0, bits 1-5 of the register specified by the R field are placed in the DBAR, and byte 1, bits 6 and 7 of that register are placed in the scan limit latches of the scanner. (See Not under Byte 1, bits 6-7).

Byte 0, bits 0-7: These bits are 0.

Byte 1, bits 0-5: DBAR bits—These bits (0-5) are placed in bit positions 5-0, respectively, of the DBAR.

Byte 1, bits 6-7: Scan Limit Select Bits 0 and 1—These bits are set as follows to indicate the desired scan limit for each Type 3 Scanner (see note).

Bit 6	7	*Scan Limit*
0	1	8
1	1	16
1	0	48
0	0	96

Note: Scan limit control is not used by the Type 3HS Communication Scanner. Byte 1, bits 6 and 7 have no effect on Type 3HS scanner operations and should be set off when Output X'42' is executed.

Output X'43' (Control)

This instruction may be executed to set or reset various control functions in a Type 3 Scanner. The Type 3 Scanner is selected by the interface address in the attachment buffer address register (ABAR) of the Attachment Base. When this instruction is executed, the bit configuration in the register specified by the R field determines which control functions are set or reset.

Byte 0, bit 0: Set Function—A 1 in this position causes the functions of byte 0, bits 2-7 and byte 1, bits 0-7 of this output to be set when the corresponding bit is 1. This bit should not be 1 if byte 0, bit 1 is 1.

Byte 0, bit 1: Reset Function—A 1 in this position causes the functions of byte 0, bits 2-7 and byte 1, bits 0-7 of this output to be reset when the corresponding bit is 1. This bit should not be 1 if byte 0, bit 0 is 1.

Byte 0, bit 2: Display Request—A 1 in this position causes the display request (ICW bit 4.6) to be set or reset according to byte 0, bits 0 and 1.

Byte 0, bits 3-5: These bits are unused.

Byte 0, bit 6: Diagnostic Test Mode—A 1 in this position sets the diagnostic latch of the scanner.

Byte 0, bit 7: Disable/Enable LIB Position—A 1 in this position causes LIB position 1 of the addressed scanner to be disabled or enabled. When this bit is on and byte 0, bit 0 (set function) is on, the LIB position is disabled. When this bit is on and byte 0, bit 1 (reset function) is on, the LIB position is enabled.

Byte 1, bit 0: Disable/Enable LIB Position 2—This bit is associated with LIB position 2 and functions the same as byte 0, bit 7.

Byte 1, bit 1: Disable/Enable LIB Position 3—This bit is associated with LIB position 3 and functions the same as byte 0, bit 7.

Byte 1, bit 2: Disable/Enable LIB Position 4—This bit is associtated with LIB position 4 and functions the same as byte 0, bit 7. This bit should be set for a Type 3 Scanner in scanner position 1.

Byte 1, bits 3 and 4: These bits are unused.

Byte 1, bit 5: Type 3 Scanner Level 1 Request—This bit is for diagnostic purposes. A 1 in this position along with the set function (byte 0, bit 0) causes a level 1 interrupt request and sets all latches in the control register.

A 1 in this position along with the reset function (byte 0, bit 1) resets the level 1 interrupt request and resets all latches in the control register.

Byte 1, bit 6: Disable Interrupt Requests—This bit is for diagnostic purposes. A 1 in this position along with the set function (byte 0, bit 0) sets the 'power-on-reset' latch and resets the scanners and LIBs. A 1 in this position along with the reset function (byte 0, bit 1) resets the 'power-on-reset' latch, thereby ending the reset state.

Programming Note
During any 'power-on' sequence, the POR latch is set in each Type 3 Scanner. The program *must* reset this latch with an Output X'43' instruction for each Type 3 Scanner before the scanner can be initialized. Also, a minimum of one scan period (153.6 microseconds) is required between setting and resetting this bit to ensure completion of the reset function.

Byte 1, Bit 7: This bit is unused.

Output X'44' (ICW Bytes 0 and 1)
This instruction (1) resets secondary control field (SCF) bits 0-3 and 5 (5 is for SDLC use only), (2) sets or resets SCF bits 6-7, (3) sets SCF bit 4, and (4) places data in the parallel data field (PDF) of the selected scanner. The PDF field is used as a character buffer. The interface address in the ABAR selects the Type 3 Scanner and the ICW associated with this address.

When this instruction is executed, the bit configuration in the register specified by the R field determine which bits are to be set, reset, or left unchanged in ICW bytes 0 and 1. Refer to the *Secondary Control Field* of the ICW in Chapter 8 for a description of the SCF bits and *Interface Control Word Format* in that chapter for a description of the PDF as it relates to various LCD states.

Byte 0, bit 0: When this bit is a 1, ICW bit 0.0 (SDLC abort) is reset to 0; otherwise, it is unchanged.

Byte 0, bit 1: When this bit is a 1, ICW bit 0.1 (normal service request interrupt) is reset to 0; otherwise, it is unchanged.

Byte 0, bit 2: If this bit is a 1, ICW bit 0.2 (character overrun/underrun) is reset to 0; otherwise, it is unchanged.

Byte 0, bit 3: If this bit is a 1, ICW bit 0.3 (modem check) is reset to 0; otherwise, it is unchanged.

Byte 0, bit 4: If this bit is a 1, ICW bit 0.4 (not level 2 bit) is set to 1; otherwise, it is unchanged.

Byte 0, bit 5: If this bit is a 1, ICW bit 0.5 (end of message) is reset to 0; otherwise, it is unchanged.

Byte 0, bit 6: If this bit is a 1, ICW bit 0.6 (program flag) is set to 1; otherwise, it is reset to 0.

Byte 0, bit 7: If this bit is a 1, ICW bit 0.7 (line trace active) is set to 1; otherwise, it is reset to 0.

Byte 1, bits 0-7: The settings of these bits are placed into the ICW positions 1.0-1.7 (PDF bits 0-7).

Output X'45' (ICW Bytes 2 and 16)
This instruction is used to set the bits of the line control definer (LCD), primary control field (PCF), and extended PCF of the ICW, and the new sync, data terminal ready, and OLT diagnostic bits of ICW byte 16. When this instruction is executed, byte 1, bits 0-7 of the register specified by the R field are placed in the LCD and PCF fields, byte 0, bits 0-3 of the register are placed in ICW bits 16.0-16.3, and byte 0, bits 4-7 of the register are placed in the extended PCF (ICW bits 16.4-16.7). The interface address in the ABAR selects the proper scanner and the associated ICW. For a detailed description of these bits, see *Interface Control Word Format* in Chapter 8.

Byte 0, bits 0-3: The settings of these bits are placed in ICW bit positions 16.0-16.3.

Byte 0, bits 4-7: The settings of these bits are placed in ICW bit positions 16.4-16.7 (extended PCF).

Byte 1, bits 0-3: The settings of these bits are placed in ICW bit positions 2.0-2.3 (LCD).

Byte 1, bits 4-7: The settings of these bits are placed in ICW bit positions 2.4-2.7 (PCF).

Output X'46' (ICW Bits 3.0-4.1)
This instruction is used to set the bits of the serial data field (SDF) of the ICW and indirectly to set or reset bits 5.4-5.7 of the ICW via a set mode operation subsequently executed by the scanner. When this instruction is executed, byte 0, bits 6-7 and byte 1, bits 0-7 of the register specified by the R field are placed in the SDF. Byte 0, bits 0-3 of the register are placed in ICW bit positions 3.0, 3.1, 3.2, and 3.6, respectively. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a detailed description of these bits, see *Interface Control Word Format* in Chapter 8.

Byte 0, bits 0-3: The settings of these bits are placed in ICW bit positions 3.0, 3.1, 3.2, and 3.6, respectively.

Byte 0, bits 4-5: These bits are unused.

Byte 0, bits 6-7: The settings of these bits are placed in ICW bit positions 3.0-3.1, respectively (SDF bits 0 and 1).

Byte 1, bits 0-7: The settings of these bits are placed into ICW bit positions 3.2-4.1, respectively (SDF bits 2-9).

Output X'47' (ICW Bits 4.2-4.5, 4.7-5.3)
This instruction sets the state of ICW bits 4.2-4.5 and 4.7-5.3. Execution of this instruction places bits from the register specified by the R field into the corresponding ICW bit positions. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a description of these bits, see *Interface Control Word Format* in Chapter 8.

Byte 0, bits 0-5: These bits are unused.

Byte 0, bits 6-7, byte 1, bit 0: Ones Counter/Interval Timer Bits 0, 1, and 2—The settings of these bits are placed in ICW bit positions 4.2, 4.3, and 4.4, respectively.

Byte 1, bit 1: Last Line State/Timeout Control—This bit is set by the scanner hardware, but it can be set and reset by this instruction.

Byte 1, bit 2: This bit is unused.

Byte 1, bits 3-4: Ones Counter/Interval Timer Bits 3 and 4—The settings of these bits are placed in ICW bit positions 4.7 and 5.0, respectively.

Byte 1, bit 5: Level 2 Interrupt Pending—A 1 in this bit position sets ICW bit 5.1, which forces an interrupt for a particular interface without requiring the interface to have a service request set. A 0 in this bit position leaves the ICW bit unchanged.

Byte 1, bits 6-7: Priority Select Bits 1 and 2—The settings of these bits are placed into ICW bit positions 5.2-5.3, respectively.

Output X'48' (ICW Bytes 6 and 7)
This instruction sets the bits of the cycle steal address, cycle steal control and cycle steal byte count fields. When this instruction is executed, bytes 0 and 1 of the register specified by the R field are placed in bytes 6 and 7, respectively, of the ICW. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW.

Byte 0, bit 0: Cycle Steal Address bit X.4.

Byte 0, bit 1: Cycle Steal Address bit X.5.

Byte 0, bit 2: Cycle Steal Address bit X.6.

Byte 0, bit 3: Cycle Steal Address bit X.7.

Byte 0, bit 4: This bit is 0.

Byte 0, bit 5: Cycle Steal Valid—This bit is set to 1 to allow a cycle steal operation.

Byte 0, bit 6: Data Chain Flag—This bit is set to 1 to indicate data chaining.

Byte 0, bit 7: Message Chain Flag—This bit is set to 1 to indicate message chaining.

Byte 1, bits 0-7: Cycle Steal Byte Count—These bits contain the byte count for the cycle steal operation.

Output X'49' (ICW Bytes 8 and 9)
This instruction places into the CSAR (ICW bytes 8 and 9) the storage address of the first data byte to be stored or accessed by a cycle steal operation. The storage address is obtained by combining the extended addressing bits (ICW bits 6.0-6.3) and the bits of the CSAR.

Output X'4A' (ICW Bytes 10 and 11)
This instruction sets the contents of the block check characters (BCC) in ICW bytes 10 and 11. This is not a normal action used by the control program, because the scanner hardware accumulates the BCC as it accesses or stores data. The interface address in the ABAR at execution selects the proper scanner and the associated ICW.

Output X'4C' (ICW Byte 1)
This instruction loads the PDF array with the 11-bit data from the register specified by the R field. The PDF pointer is not changed by this instruction. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW. For a description of the PDF bits, see *PDF Array Format* in Chapter 8.

Output X'4D' (ICW Byte 1)
This instruction loads the cycle steal PDFs with two data bytes from the register specified by the R field. The line address in the ABAR selects the proper scanner and the associated ICW and PDF array for the line interface. The cycle steal pointer selects one of the eight PDFs in the PDF array. Execution of this instruction causes the cycle steal PDF array pointer (ICW bits 12.0-12.3) to be incremented by two.

Output X'4E' (ICW Bytes 12, 13, and 17)
This instruction sets the contents of the ICW control bytes (12, 13, and 17) from the register specified by the R field. The interface address in the ABAR at execution time selects the proper scanner and the associated ICW, (See Note under "Byte 1, bits 4-5"). For a detailed description of these bits, see *Interface Control Word Format* in Chapter 8.

Byte 0, bits 0-3: Cycle Steal PDF Array Pointer—These bits contain the address of the current PDF from which or to which data is being transferred via cycle steal operation.

Byte 0, bits 4-7: PDF Array Pointer—These bits contain the address of the current PDF from which or to which data is being transferred by the control program.

Byte 1, bits 0-1: Sequence 0 and 1—These bits are used by the scanner in determining the appropriate action to perform upon receiving or transmitting BSC and SDLC control sequences within message data.

Byte 1, bit 2: Request-to-Send Turnaround Control—This bit is set or reset by the control program to determine whether the RTS lead in the modem interface is to remain active or be deactivated when a line turnaround from transmit state to receive state occurs.

Byte 1, bit 3: Sequence 2—This bit is used by the scanner (1) in determining the action to take upon receiving an SDLC flag character under certain conditions, or (2) to indicate that character phase has been entered, for a BSC line.

Byte 1, bits 4-5: These bits are 0 when executing an Output X'4E' instruction on a Type 3 Scanner (see Note).

Note: The following statements apply only to a Type 3HS Communication Scanner.

1. ICW bits 13.4 and 17.0 are both set to "1" when byte 1, bit 4 of the Output X'4E' register is on.
2. ICW bits 13.5 and 17.1 are both set to "1" when byte 1, bit 5 of the Output X'4E' register is on.

Byte 1, bits 6-7: Message Counter—These bits are used by the Type 3 Scanner in keeping track of multiple SDLC messages that may be queued in the PDF array during a receive operation.

Output X'4F' (ICW Bytes 14 and 15)
This instruction (1) resets ICW bits 14.0, 14.1, 14.3, 14.4, 14.6, and 14.7 from the corresponding bits of the register specified by the R field, and (2) sets or resets ICW bits 14.2, 14.5, and 15.0-15.7 from the corresponding bits of the register. For a detailed description of these bits, see *Interface Control Word Format* in Chapter 8.

Type 1 and Type 4 CA Input Instructions

Input X'60' (Initial Selection Control)
This instruction loads the register specified by R with the contents of the initial selection control register. The bits of this register are normally set at the completion of initial selection and identify the cause of a Type 1 or 4 CA initial L3 interrupt request.

Programming Note
The control program should not execute an Input X'60' while the channel adapter is enabled unless a Type 1 or 4 CA Initial Selection L3 Interrupt is present. If this input instruction is executed prior to an initial selection interrupt, an I/O parity check may occur because the data can be changing while the register is being accessed.

Byte 0, bit 0: Initial Selection Interrupt—This bit is set by hardware and causes a Type 1 CA initial L3 interrupt request when a Start I/O command is accepted by the adapter and clear initial status is presented to the host channel. This bit is also set when a Test I/O command is received for an emulation subchannel address and a status of X'70' is returned. If this bit is zero, the interrupt request was caused by an unusual condition and can be further defined by the remaining bits of this input. An Output X'62', byte 0, bit 5 or an Output X'60' resets this bit.

Byte 0, bit 1: Interface Disconnect—This bit is set by hardware when an interface disconnect condition (Halt I/O command) is detected during an initial selection sequence. An Output X'62', byte 0, bit 5 or an Output X'60' resets this bit.

Byte 0, bit 2: Selective Reset—This bit is set by hardware when a selective reset condition is detected during an initial selection sequence. An Output X'62', byte 0, bit 5 or an Output X'60' resets this bit.

Byte 0, bit 3: Channel Bus Out Check–This bit is set by hardware when incorrect parity is detected in the channel command byte during initial selection. This causes the CA to automatically respond with Unit Check (UC) initial status. An Output X'62', byte 0, bit 5 or an Output X'60 resets this bit.

Byte 0, bit 4: This bit is 0.

Byte 0, bit 5: Stacked Initial Status—This bit is set by hardware when a stacked status condition is detected during initial selection. An Output X'62', byte 0, bit 5 or an Output X'60' resets this bit.

Byte 0, bit 6: NSC Status Byte Cleared–This bit is set to indicate that a status byte for the native mode subchannel (NSC) has been transferred as the initial status byte in an initial selection. Therefore, the NSC status byte has been cleared, and this resulted in the setting of the CA initial level 3 interrupt request. An Output X'62', byte 0, bit 5 or an Output X'60' resets this bit.

Byte 0, bit 7: System Reset—This bit is set by hardware and causes a level 3 initial selection interrupt when a system reset is detected on the channel interface. An Output X'67', byte 1, bit 3 resets this bit.

Byte 1, bits 0-7: These bits are 0.

Input X'61' (Initial Selection Address and Command)
Programming Note
The control program should not execute an Input X'61' while the channel adapter is enabled unless a CA Initial Selection L3 Interrupt is present. If this input instruction is executed prior to an initial selection interrupt, an I/O parity check may occur because the data can be changing while the register is being accessed.

Byte 0, bits 0-7: Initial Selection Address—These bits are set during an initial selection sequence and contain the address of the line selected.

Byte 1, bits 0-7: Initial Selection Command—These bits are set during an initial selection sequence and contain the command as presented to the channel adapter from the channel interface.

Input X'62' (Data/Status Control)
This input loads the register specified by R with the contents of the data/status control register. The bits of this register identify the cause of a CA data/status L3 interrupt request.

Byte 0, bit 0: Outbound Data Transfer Sequence—This bit indicates that the channel adapter hardware is transferring data to the host processor channel. The control program can set or reset this bit with an Output X'62' instruction.

Byte 0, bit 1: Inbound Data Transfer Sequence—This bit indicates that the channel adapter hardware is transferring data from the host processor channel. The control program can set or reset this bit with an Output X'62' instruction.

Byte 0, bit 2: ESC Final Status Transfer Sequence—This bit indicates that the channel adapter is transferring a 2701/2702/2703 type status byte to the host processor channel. The control program can set or reset this bit with an Output X'62' instruction.

Byte 0, bit 3: NSC Channel End Status Transfer Sequence—This bit indicates that the channel adapter is transferring NSC Channel End status to the host processor channel. The control program can set or reset this bit with an Output X'62' instruction.

Programming Note
If the host channel accepts the NSC Channel End status byte, the channel adapter automatically generates a Busy initial status. This occurs in all subsequent initial selection sequences on the native mode subchannel until the control program initiates an NSC final status transfer by executing Output X'62'.

Byte 0, bit 4: NSC Final Status Transfer Sequence—This bit indicates that the channel adapter is tranferring final status to the host processor channel. The control program can set or reset this bit with an Output X'62' instruction.

Byte 0, bit 5: Channel Stop or Interface Disconnect—This bit indicates that a channel stop or interface disconnect was detected when the channel adapter was in a data transfer sequence. This bit is set by hardware and reset by an Output X'62', byte 0, bit 6.

Byte 0, bit 6: Suppress Out Monitor Interrupt—This bit is set by hardware and causes a CA data/status L3 interrupt request when the 'suppress out monitor' latch (see Output X'67') is on and the 'suppress out' tag line drops. This bit is reset by executing an Output X'62' instruction.

Byte 0, bit 7: Program-Requested Interrupt—This bit indicates that the program has requested a CA data/status L3 interrupt by executing an Output X'67' instruction. Execution of an Output X'62' instruction with any bit combination resets this bit.

Byte 1, bit 0: Channel Bus Out Check—This bit is set by hardware to indicate incorrect parity on the channel interface during a Write command. This bit is reset by an Output X'62', byte 0, bit 6.

When this check occurs, the byte with incorrect parity is placed in the data buffer, and data transfer is terminated. The transfer byte count (byte 1, bits 5-7) reflects the byte that caused the check.

Byte 1, bit 1: Selective Reset—This bit is set by the CA hardware to indicate the detection of a selective reset when the CA was in a service transfer sequence. This bit is reset by an Output X'62', byte 0, bit 6.

Byte 1, bit 2: Suppress Out—This bit is set to indicate that the 'suppress out' tag line on the channel interface is active.

Byte 1, bit 3: Stacked Ending Status—This bit is set to indicate that the ending status has been stacked by the host processor channel during a status transfer sequence. This bit is reset by an Output X'62', byte 0, bit 6.

Byte 1, bit 4: I/O Command Chaining—This bit indicates command chaining when the CA is in a status transfer sequence. This bit is reset by an Output X'62', byte 0, bit 6.

Byte 1, bits 5-7: Transferred Byte Count Bits 0-2 (Non-EB/Non-Cycle Steal mode)—These bits are set by the CA hardware and reflect the number of bytes transferred across the channel in the current data transfer operation or the last-completed data transfer operation (if none is in progress). Up to four bytes can be transferred in one data transfer sequence.

Bit 5	6	7	*Number of Bytes Transferred*
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4

Input X'63' (CA Address and ESC Status Bytes)
This instruction loads a general register with the CA line address and the status bits for the line that were set by the last Output X'63' instruction.

Byte 0, bits 0-7: Address Byte—These bits contain the address of the last communication line to be ser-

viced by the channel adapter for data or status transfer.

Byte 1, bit 0: ESC Attention.

Byte 1, bit 1: ESC Status Modifier.

Byte 1, bit 2: ESC Control Unit End.

Byte 1, bit 3: ESC Busy.

Byte 1, bit 4: ESC Channel End.

Byte 1, bit 5: ESC Device End.

Byte 1, bit 6: ESC Unit Check.

Byte 1, bit 7: ESC Unit Exception.

Input X'64' (Data Buffer Bytes 1 and 2)
This instruction loads a general register with the contents of the data buffer bytes 1 and 2 as received from the channel interface. It can also be used to verify the contents of the data buffers following an Output X'63' instruction.

Byte 0, bits 0-7: Data Buffer Byte 1—These bits represent the first byte of data received from the channel during a channel Write command.

Byte 1, bits 0-7: Data Buffer Byte 2—These bits represent the second byte of data received from the channel during a channel Write command.

Input X'65' (Data Buffer Bytes 3 and 4)
This instruction loads a general register with the contents of the data buffer bytes 3 and 4 as received from the channel interface. It can also be used to verify the contents of the data buffers following an Output X'64' instruction.

Byte 0, bits 0-7: Data Buffer Byte 3—These bits represent the third byte of data received from the channel during a channel Write command.

Byte 1, bits 0-7: Data Buffer Byte 4—These bits represent the fourth byte of data received from the channel during a channel Write command.

Input X'66' (NSC Status Byte)
This instruction loads a general register with the contents of the NSC status register. These bits reflect the status bits loaded into the status register by the last Output X'66' instruction. This instruction should be used only as a diagnostic aid.

Byte 0, bit 0: Attention

Byte 0, bit 1: Status Modifier

Byte 0, bits 2-3: These bits are 0.

Byte 0, bit 4: Channel End.

Byte 0, bit 5: Device End.

Byte 0, bit 6: Unit Check.

Byte 0, bit 7: Unit Exception.

Byte 1, bits 0-7: These bits are 0.

Input X'67' (CA Controls)
This instruction loads a general register with various kinds of CA control information. Byte 1, bits 0-3 (check indications) are reset by an Output X'67', byte 1, bit 2.

Byte 0, bits 0-7: These bits are set to the NSC address for the enabled A or B interface.

Byte 1, bit 0: Channel Bus In Check—This bit indicates that incorrect parity was detected on the channel bus in. When this is detected, the hardware generates good parity and causes a level 1 interrupt.

Byte 1, bit 1: In/Out Instruction Accept Check—This bit indicates that the control program executed an Input or Output X'60', X'61', X'62', X'63, X'64', X'65', or X'66' instruction when the CA was in the process of handling a data/status transfer. Detection of this condition also causes a level 1 interrupt request.

Byte 1, bit 2: CCU Outbus Check—This bit indicates that the CA hardware detected incorrect parity on the CCU outbus. When this is detected, the hardware causes a level 1 interrupt request and prohibits reselection on the channel interface until this bit is reset.

Byte 1, bit 3: Local Store Check—This bit indicates that the CA hardware detected incorrect parity on data bytes gated out of local store. The control program should place good parity in local store by executing an Output X'63', X'64', or X'65' instruction.

Byte 1, bit 4: Channel Interface Enabled—This bit indicates that either interface A or interface B is enabled. When no interface is enabled, the bit is 0.

Byte 1, bit 5: NSC Address Active—This bit indicates that the native subchannel has been selected and is active. The bit is reset when the host channel accepts the final status from the CA.

Byte 1, bits 6-7: (Type 1 CA) These bits are unused.

Byte 1, bits 6-7: Type 4 CA Selected—These bits indicate which of up to four Type 4 CAs is currently selected: 00-Type 4 CA-1, 01-Type 4 CA-2, 10-Type 4 CA-3, 11-Type 4 CA-4.

Input X'6C' (EB Mode/Cycle Steal Mode Control Register) (Type 4 CA)
This instruction loads the contents of the channel adapter's control character recognition latches, the EB mode/cycle steal mode control bits, and the EB mode/cycle steal mode byte count into the register specified by the R field.

Byte 0, bit 0: EB Mode—This bit indicates whether the CA is in extended buffer mode (bit=1) or in non-extended buffer mode (bit=0).

Byte 0, bits 1-4: (Type 1 CA) These bits are 0.

Byte 0, bit 1: (Type 4 CA) Cycle Steal Mode—This bit indicates whether the Type 4 CA is in cycle steal mode (bit=1) or in non-cycle steal mode (bit=0).

Byte 0, bits 2-3: (Type 4 CA) These bits are 0.

Byte 0, bit 4: (Type 4 CA) SYN Monitor Control Latch—A 1 indicates that the SYN monitor control latch is set, a 0 indicates that the latch is reset.

Byte 0, bit 5: DLE Remember Latch—A 1 indicates that the DLE remember latch is set, a 0 indicates that the latch is reset.

Byte 0, bit 6: ASCII Monitor Latch—A 1 indicates that the ASCII monitor latch is set, a 0 indicates that the latch is reset.

Byte 0, bit 7: EBCDIC Monitor Latch—A 1 indicates that the EBCDIC monitor latch is set, a 0 indicates that the latch is reset.

Byte 1, bits 0-7: Register Byte Count (EB Mode/Cycle Steal Mode)—These bits contain the byte count of data transferred by the Type 4 CA in extended buffer mode or cycle steal mode.

Input X'6D' (EB Mode/Cycle Steal Mode Data Buffer) (Type 4 CA)
This instruction loads the contents of the two-byte EB mode/cycle steal mode buffer into the register specified by the R field. The first (even) data byte is placed in byte 0 of the register; the second (odd) byte is placed in byte 1 of the register.

Input X'6E' (Cycle Steal Mode Error Register and CSAR Byte X) (Type 4 CA)
This instruction loads the contents of the cycle steal error register and byte X of the CSAR into the register specified by the R field. Byte 0, bits 0-3 are reset by an Output X'67' instruction in which bit 1.2 is set to 1.

Byte 0, bit 0: Cycle Steal Outbus Error.

Byte 0, bit 1: Cycle Steal Inbus Error.

Byte 0, bit 2: Cycle Steal Address Bus Error.

Byte 0, bit 3: Cycle Steal Address Exception Error.

Byte 0, bits 4-7: These bits are 0.

Byte 1, bits 0-3: These bits are 0.

Byte 1, bit 4: CSAR byte X bit 4.

Byte 1, bit 5: CSAR byte X bit 5.

Byte 1, bit 6: CSAR byte X bit 6.

Byte 1, bit 7: CSAR byte X bit 7.

Input X'6F' (Cycle Steal Mode CSAR Bytes 0 and 1) (Type 4 CA)
This instruction loads the contents of the CSAR bytes 0 and 1 into the register specified by the R field.

Byte 0, bits 0-7: CSAR byte 0, bits 0-7.

Byte 1, bits 0-7: CSAR byte 1, bits 0-7.

Type 1 and Type 4 Output Instructions

Output X'60' (Reset Initial Selection)
This instruction resets the CA initial selection latches and the level 3 interrupt request resulting from an initial selection. Since this instruction performs a function, the bit settings of the register specified by the R operand are ignored.

Output X'62' (Data/Status Control)
This instruction unconditionally resets the CA program-requested interrupt and the 'suppress out monitor' latch. It also is used to set the following bits in the data/status control register.

Programming Note
If the suppress out monitor interrupt (Input X'62', byte 0, bit 6) is active, this instruction should be executed when initiating the next transfer sequence.

If the suppress out monitor and the program requested interrupt requests are both set, resetting one of them also resets the other. Therefore, if one of the interrupts is still desired, it must be requested again by an Output X'67' with the appropriate bit set.

Byte 0, bit 0: Outbound Data Transfer Sequence—This bit is set by the control program to initiate an outbound data transfer sequence. For example, a channel Read or Sense command should initiate an outboard data transfer sequence that sends data to the host processor.

Byte 0, bit 1: Inbound Data Transfer Sequence—This bit is set by the control program to initiate an inbound data transfer sequence. For example, a channel Write command should initiate an inbound data transfer sequence that receives data from the host processor.

Byte 0, bit 2: ESC Final Status Transfer Sequence—This bit is set by the control program and signals the hardware to initiate an ESC status transfer using the address and status information previously loaded into the address and status register by an Output X'63'.

Byte 0, bit 3: NSC Channel End Status Transfer—This bit is set by the control program and signals the CA hardware to present Channel End only for the associated NSC address.

Byte 0, bit 4: NSC Final Status Transfer—This bit is set by the control program and signals the CA hardware to initiate an NSC final status transfer sequence.

Byte 0, bit 5: Reset Initial Selection–This bit is set by the control program to reset byte 0, bits 0-6 of the initial selection control register (Input X'60'). This reset allows the CA to accept an initial selection. The bit position is reset to 0 at the completion of the Output X'62' instruction.

Note: *This bit resets the CA initial L3 interrupt request unless the interrupt was caused by a system reset.*

Byte 0, bit 6: Reset Data/Status Interrupt–This bit is set by the control program to reset the CA data/status L3 interrupt request and the following data/status service register bits.

- Interface disconnect
- Selective reset
- Bus out check
- Monitor for circle B and 2848 ETX
- Channel stop
- Stacked status

When this bit is on along with one of the transfer sequence bits (byte 0, bits 0-4), the CA hardware raises the 'request in' tag line on the channel interface, except when ESC Test I/O Status is available (Output X'62', byte 1, bit 4).

This bit position is reset to 0 at the completion of the Output X'62' instruction.

Byte 0, bit 7: Type 4 CA–Reset Extended Buffer Mode or Cycle Steal Mode. Type 1 CA–This bit is unused.

Byte 1, bit 0: Set Monitor for an IBM Type I or II Circle B—When this bit is set to 1, the channel adapter hardware circuits monitor the inbound data characters for a circle B (X'3D' or X'BD'). When the circle B is detected, the CA causes a channel stop condition and sets byte 0, bit 5 of Input X'62' to 1 (Channel Stop/Interface Disconnect). This monitor bit is reset by Output X'62', byte 0, bit 6 (Reset data/status interrupt).

Byte 1, bit 1: This bit is unused.

Byte 1, bit 2: Set Monitor for IBM 2848 or 2845 ETX—When this bit is set to 1, the channel adapter hardware circuits monitor the inbound data characters for a 2848 or 2845 ETX (X'03'). When the ETX is detected, the CA causes a channel stop condition and

sets byte 0, bit 5 of Input X'62' to 1 (Channel Stop/Interface Disconnect). This monitor bit is reset by Output X'62', byte 0, bit 6 (Reset data/status interrupt).

Byte 1, bit 3: Set Suppressible Status—This bit should be set when the control program is presenting suppressible status to the host channel when ESC mode is enabled. Status is suppressible if 'stacked status' is received for a particular line or when the line has been issued an interface disconnect. Refer to *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers Information* (GA22-6974) for further information on suppressible status.

Byte 1, bit 4: Set ESC Test I/O Status Available—When this bit is set to 1, the controller hardware responds to a Test I/O command given to a 2701/2702/2703 address. The control program must have previously loaded the correct address and status byte into the CA address and emulator status byte register (Output X'63') before setting this bit. This bit is reset by the emulator hardware when it presents this status to the channel.

When this bit is set to 1, byte 0, bit 2 of this instruction must also be set to 1.

Byte 1, bit 5: Type 4 CA–Set Priority Outbound Data Transfer Sequence. Type 1 CA–This bit is unused.

Byte 1, bits 6-7: Request Byte Count 1 and 2–These bits are set according to the number of bytes to be transferred during inbound or outbound data transfer. (Type 4 CA: These bits apply to data transfer in non-EB or non-CS mode.)

In EB or CS mode, bits 6 and 7 are set as indicated to monitor the number of consecutive SYN characters (maximum of 4). The 'syn monitor control' latch must be set with an Output X'6C' instruction (byte 0, bit 4 = 1) before issuing the Output X'62' instruction.

Bit 6	7	*Number of Bytes Transferred**
0	1	1
1	0	2
1	1	3
0	0	4

*In extended buffer mode or cycle steal mode, the *number of bytes transferred* represents the number of consecutive SYNS to be monitored.

Output X'63' (CA Address and Emulator Status Bytes)
The control program can set this output to indicate the line address (NSC or ESC) and the status of the line to be serviced next by the CA in emulation mode.

Byte 0, bits 0-7: Address Byte–These bits are set by the control program to indicate the I/O device address to be serviced. The bits are used only when Output X'62' bit 0.2 is set to '1'.

Byte 1, bit 0: Set ESC Attention status.

Byte 1, bit 1: Set ESC Status Modifier.

Byte 1, bit 2: Set ESC Control Unit End status.

Byte 1, bit 3: Set ESC Busy status.

Byte 1, bit 4: Set ESC Channel End status.

Byte 1, bit 5: Set ESC Device End status.

Byte 1, bit 6: Set ESC Unit Check status.

Byte 1, bit 7: Set ESC Unit Exception status.

Output X'64' (Data Buffer Bytes 1 and 2)
This instruction is used only for outbound data transfer. (Type 4 CA: This instruction applies only to data transfer in non-EB mode/non-cycle steal mode.)

Byte 0, bits 0-7: Data Buffer Byte 1—These bits represent the first data byte to be sent across the channel during a channel Read command. This buffer must be loaded by the control program.

Byte 1, bits 0-7: Data Buffer Byte 2—These bits represent the second data byte to be sent across the channel during a channel Read command. This buffer must be loaded by the control program.

Output X'65' (Data Buffer Bytes 3 and 4)
This output instruction is used only for outbound data transfer.

Byte 0, bits 0-7: Data Buffer Byte 3—These bits represent the third data byte to be sent across the channel during a channel Read command. This buffer must be loaded by the control program.

Byte 1, bits 0-7: Data Buffer Byte 4—These bits represent the fourth data byte to be sent across the channel during a channel Read command. This buffer must be loaded by the control program.

Output X'66' (CA NSC Status Byte)
This instruction loads the native mode status byte with the bits that are set in the register specified by R. The control program sets these bits to indicate the status to be presented across the channel interface when the CA is in the NSC status transfer sequence. Hardware resets these bits when the status byte is accepted by the channel.

Byte 0, bits 0-3, 5-7: Type 4 CA—These bits are unused.

Byte 0, bit 4: Type 4 CA: Set NSC Long Busy.

Byte 0, bits 0-7: Type 1 CA—These bits are unused.

Byte 1, bit 0: Set Attention status.

Byte 1, bit 1: Set Status Modifier.

Byte 1, bits 2-3: These bits are unused.

Byte 1, bit 4: Set Channel End.

Byte 1, bit 5: Set Device End.

Byte 1, bit 6: Set Unit Check.

Byte 1, bit 7: Set Unit Exception.

Output X'67' (CA Controls)
This instruction causes various control latches to be set or reset in the channel adapter according to the states of the bits in the register specified by R.

Byte 0 (Type 1 CA)

Byte 0, bits 0-3: (Type 1 CA) These bits are unused.

Byte 0, bit 4: (Type 1 CA) Diagnostic Reset—This bit resets the channel adapter when the 'channel interface disable' latch is set. This bit should be set only by a diagnostic program and not by inline code.

Byte 0, bits 5-7: (Type 1 CA) These bits are unused.

Byte 0 (Type 4 CA)
The control program must execute an Output X'67' instruction to enable the channel adapter before the CA can transfer data to or from the channel. This instruction first selects the Type 4 CA specified by CCU Outbus bits 0.5-0.7 and resets the 'selected' latch on the Type 4 CAs not specified; thus only one Type 4 CA at a time can be selected. The instruction then sets the control latches in the selected CA.

Programming Notes: (1) Outbus bit 0.5 must not be a 1 for subsequent Output X'67' instructions unless a currently non-selected CA is to be selected. (2) The control program can execute this instruction for a non-selected CA by setting Outbus bit 0.3 to 1. The status of the 'selected' latch in each Type 4 CA is not altered, but the Output X'67' instruction is executed for the non-selected CA. Bits 0.3 and 0.5 must never both be set to 1 during the same Output X'67' instruction.

Byte 0, bit 0: (Type 4 CA) Diagnostic Force Initial Selection Interrupt.

Byte 0, bit 1: (Type 4 CA) Diagnostic Force Byte Transfer in Cycle Steal Mode.

Byte 0, bit 2: (Type 4 CA) This bit is unused.

Byte 0, bit 3: (Type 4 CA) Perform Output X'67' on Type 4 CA specified by bits 0.6-0.7.

Byte 0, bit 4: (Type 4 CA) Diagnostic Reset—This bit resets the channel adapter when the 'channel interface disable' latch is set. This bit should be set only by a diagnostic program and not by inline code.

Byte 0, bit 5: Type 4 CA Selection Indicator—This bit, when set to 1, causes the control program to select the Type 4 CA specified by bits 0.6 and 0.7. The instruction is then executed for the selected CA. This bit, when set to 0, causes the control program to execute the instruction for the currently selected Type 4 CA.

Byte 0, bits 6 and 7: Selected Type 4 CA—These bits specify in which of up to four Type 4 CAs the output X'67' instruction is to be executed:

00 – Type 4 CA #1
01 – Type 4 CA #2
10 – Type 4 CA #3
11 – Type 4 CA #4

Byte 1, bit 0: Suppress Out Monitor Interrupt—A 1 in this position causes the CA to monitor the 'suppress out' tag line for the inactive state. When this is detected, the CA data/status L3 interrupt request is set. After servicing the request, the control program should execute an Output X'62' instruction to reset the request.

Programming Note
Following a stacked status condition, the control program can use this bit to cause the channel adapter to signal when the suppress status indication is removed.

Byte 1, bit 1: Set Program-Requested Interrupt—A 1 in this position indicates that a CA data/status L3 interrupt is requested. If a data/status transfer or initial selection is in progress, the interrupt request is held until the sequence is complete.

Byte 1, bit 2: Reset Level 1 Checks—A 1 in this position resets the CA level 1 check latches and interrupt requests.

Byte 1, bit 3: Reset System Reset and NSC Address Active—A 1 in this position resets the level 3 interrupt request caused by a system reset. It also resets the NSC address active indication and the NSC status register.

Byte 1, bit 4: Allow Channel Interface Enable—A 1 in this position causes the 'channel interface enable' latch to be set. This enables thc CA to communicate with the host processor. The bit must be 0 if byte 1, bit 7 of this output is 1.

Programming Note
The channel interface cannot be enabled following a power-off to power-on-reset until an Output X'67 is executed with this bit on. The IPL Bootstrap program performs this operation in IPL Phase 3.

Byte 1, bit 5: ESC Operational—A 1 in this position sets the emulator subchannel (ESC) addresses to an operational mode. The channel interface must be enabled before the emulator subchannels can become operational.

Byte 1, bit 6: ESC Command Free—A 1 in this position resets the 'ESC command active' latch. The 'ESC command active' latch is set by initial selection.

Programming Note
The CA cannot be disabled until it is free of commands; therefore, the control program must ensure that the 'ESC command active' latch is reset before a disable attempt is made.

Byte 1, bit 7: Allow Channel interface Disable—A 1 in this position sets the 'channel interface disable' latch. This latch overrides the I/O Channel 1 Enable/Disable switch on the control panel and allows the channel to become disabled if (1) the channel adapter is free of commands, (2) commands are not chained, and (3) the adapter is not in initial selection.

The 'channel interface disable' latch is reset by Output X'67', byte 1, bit 4.

Output X'6C' (EB Mode Control Register) (Type 4 CA)
This instruction sets the contents of the channel adapter's control character recognition latches, the EB mode control bit, and the EB mode byte count from the corresponding bits of the register specified by the R field.

Byte 0, bit 0: Set/Reset EB Mode—A 1 specifies that the CA is to operate in extended buffer mode; a 0 specifies that the CA is to operate in non-extended buffer mode.

Byte 0, bits 1-4: These bits are 0. (Bit 1 is reserved for future use.)

Byte 0, bit 5: DLE Remember Latch—A 1 sets this latch; a 0 resets it.

Byte 0, bit 6: ASCII Monitor Latch—A 1 sets this latch; a 0 resets it.

Byte 0, bit 7: EBCDIC Monitor Latch—A 1 sets this latch; a 0 resets it.

Byte 1, bits 0-7: Register Byte Count (EB Mode)—These bits contain the byte count of data to be transferred by the Type 4 CA in extended buffer mode.

Output X'6D' (EB Mode/Cycle Steal Data Buffer) (Type 4 CA)
This instruction loads two data bytes from the register specified by the R field into the EB mode/cycle steal data buffer of the Type 4 CA. The first data byte (0) of the register is placed in the first (even) byte of the buffer; the second data byte (1) of the register is placed in the second (odd) byte of the buffer.

Note: This instruction has no effect unless the Type 4 CA is in EB mode or cycle steal mode.

Output X'6E' (CSAR Byte X) (Type 4 CA)
This instruction sets the extended address bits of CSAR byte X from the register specified by the R field.

Programming Note
Before this instruction is executed, an Output X'6F' instruction must be executed to set CSAR bytes 0 and 1 and reset CSAR byte X.

Byte 0, bits 0-7: These bits are unused.

Byte 1, bits 0-3: These bits are unused.

Byte 1, bits 4-7: CSAR byte X bits 4-7.

Output X'6F' (Cycle Steal Mode CSAR Bytes 0 and 1) (Type 4 CA)
This instruction sets into CSAR bytes 0 and 1 (16 low-order bits only) the storage address of the first data buffer byte involved in a cycle steal data transfer. When the cycle steal data transfer ends, the address is updated to the next sequential storage halfword address. This instruction also resets CSAR byte X to 0.

Byte 0, bits 0-7: CSAR byte 0, bits 0-7.

Byte 1, bits 0-7: CSAR byte 1, bits 0-7.

Type 2 and Type 3 CA Input Instructions

Input X'50' (Inbound Data Control Word Address Register INCWAR)
This instruction loads a general register with the contents of the INCWAR. The INCWAR contains the storage address of the first control word to be used when the channel adapter receives a Write, Write Break, or Write IPL command. The CA recognizes this instruction only after setting a CA interrupt request.

Byte 0, bits 0-7: INCWAR bits 0-7.

Byte 1, bits 0-7: INCWAR bits 8-15.

Input X'51' (Outbound Data Control Word Address Register–OUTCWAR)
This instruction loads a general register with the contents of the OUTCWAR. The OUTCWAR contains the storage address of the next control word to be used when the channel adapter receives a Read command. The instruction is recognized by the CA only following the setting of a CA interrupt request.

Byte 0, bits 0-7: OUTCWAR bits 0-7.

Byte 1, bits 0-7: OUTCWAR bits 8-15.

Input X'52' (Control Word Byte Count Register–CWCNT)
This instruction loads a general register with the number of bytes remaining to be transferred under the last control word that was fetched. See *Control Word Byte Count Register* in Chapter 10. The CA recognizes this instruction only after setting a CA interrupt request.

Byte 0, bits 0-5: These bits are 0.

Byte 0, bits 6-7: CWCNT bits 0-1. (For 3705-II Models J–L, bits 6 and 7 of byte 0 are used as CWCNT bits in IPL mode only.)

Byte 1, bits 0-7: CWCNT bits 2-9. (When 3705-II Models J–L are in non-IPL mode, the CWCNT field is reduced to 8 bits. Byte 1, bits 0-7 represent bits 0-7 of the CWCNT field.)

Input X'53' (Channel Adapter Sense Register–CASNSR)
This instruction loads a general register with the contents of the channel adapter sense register and byte X of the CSAR.

The sense register is accessible for input only when the CA is active, selected, and has a level 1 or level 3 interrupt request set, or the CA is in the diagnostic wrap state. If these conditions are not met, an Input X'53' causes a CCU Inbus parity check. If an interrupt request is set and the CA is not active, an Input X'53' causes the general register to be loaded with zeros. If restrictions that apply to the Input X'53' instruction are met, CSAR information is accessible from the CASNSR register with the selected channel adapter active or inactive.

Byte 0, bit 0: Command Reject—This bit is set when the host processor channel command presented to the CA during initial selection is not a valid command for the controller.

Byte 0, bit 1: Intervention Required—This bit indicates programming errors detected by the CCU or CA hardware, or the control program. It is set under hardware control for any one of the following conditions:

1. The CCU 'hard stop' latch is set while the CA is transferring data under a Read, Write, or Write Break command.
2. An addressing exception or a protection check was caused by the address used by the CA for a cycle-steal operation.
3. A TIC command or command chaining to a control word address above 64K has been detected during a CW fetch cycle steal.
4. An OUT or OUT STOP control word was decoded when executing a channel Write, Write Break, or Write IPL command during a CW fetch cycle steal.
5. An IN control word was decoded when executing a channel Read command during a CW fetch cycle steal.
6. An IN, OUT, or OUT STOP control word was decoded with a byte count of zero during a CW fetch cycle steal.

Programming Note
Condition 3 above also sets byte 0, bit 0 (invalid CWAR address) of the channel adapter check register. Conditions 4, 5, and 6 above also set byte 0, bit 1

(invalid control word format) of the channel adapter check register.

Byte 0, bit 2: Bus Out Check—This bit is set when a parity error is detected on the channel bus out during the initial selection command transfer or during host processor-to-controller data transfer. The control program cannot set this bit.

Byte 0, bit 3: Equipment Check—This bit is set any time the CA detects an internal hardware error or a parity error on the Inbus or Outbus between the Central Control Unit and the CA.

Byte 0, bit 4: Data Check—This bit can be set on by the control program only during a level 3 interrupt.

Byte 0, bit 5: This bit is 0.

Byte 0, bit 6: Not Initialized—This bit is on when the controller has not been initialized. The channel adapter hardware sets the not-initialized condition when the CA goes offline. This condition is reset by the ROS program via an Output X'77' with byte 0, bit 0 on.

Byte 0, bit 7: Abort—This bit indicates that the channel adapter has halted its channel operation abnormally.

Byte 1, bits 0-3: These bits are 0.

Byte 1, bit 4: CSAR byte X bit 4.

Byte 1, bit 5: CSAR byte X bit 5.

Byte 1, bit 6: CSAR byte X bit 6.

Byte 1, bit 7: CSAR byte X bit 7.

Input X'54' (Channel Adapter Status Register–CASTR)
This instruction loads a general register with the contents of the channel adapter status register. The bits of the status register can be set by the control program and/or the CA hardware. See Output X'54' in this appendix for the method of setting each bit.

Byte 0, bit 0: Attention—This bit indicates that Attention has been set.

Byte 0, bit 1: Status Modifier—This bit indicates that the Status Modifier has been set.

Byte 0, bit 2: This bit is 0.

Byte 0, bit 3: Busy—This bit indicates that Busy status has been set.

Byte 0, bit 4: Channel End—This bit indicates that Channel End status has been set.

Byte 0, bit 5: Device End—This bit indicates that Device End status has been set.

Byte 0, bit 6: Unit Check—This bit indicates that a Unit Check has occurred.

Byte 0, bit 7: Unit Exception—This bit indicates that Unit Exception status has been set.

Byte 1, bits 0-7: These bits are 0.

Input X'55' (Channel Adapter Control Register–CACR)
This instruction loads a general register with the status of various control latches in the CA. This instruction is recognized by the CA only following the setting of a CA select and a CA interrupt request. The CA need not be in the CA active state.

Byte 0, bit 0: Diagnostic Wrap Mode—This bit indicates that the controller is offline and in the diagnostic wrap state.

Byte 0, bit 1: Zero Count Override—This bit indicates the condition of the zero count override flag in the control word just executed. It is reset either when a control word is fetched with zero count override off, or when Channel End is generated for the current command.

Byte 0, bit 2: INCWAR Valid—This bit indicates that the control word address register for inbound data transfer (channel Write command) points to the storage location containing the control word to be used for controlling this type of data transfer.

The control program sets this bit during a CA-requested level 3 interrupt via an Output X'55' instruction. However, once data transfer across the channel begins, this bit is controlled as follows.

After an IN-CW fetch operation, the bit reflects the status of the chain flag of the IN-CW fetched for the CA. During the CW fetch operation, the address in

the INCWAR register is incremented by 4 (fullword address). The chain flag in the fetched CW indicates whether or not the updated INCWAR points to a valid CW. If the chain bit is off in the fetched CW, the 'INCWAR valid' latch is reset.

Byte 0, bit 3: OUTCWAR Valid—This bit indicates that the control word address register for outbound data transfer (that is, a channel Read command) points to the storage location containing the control word to be used for controlling this type of data transfer. The control program sets this bit during a CA-requested level 3 interrupt by an Output X'55' instruction. However, once data transfer across the channel has started, this bit is controlled as follows.

After an OUT-CW fetch operation, this bit reflects the status of the chain flag in the OUT or OUT STOP control word fetched for the CA. During the CW fetch operation, the address in the OUTCWAR is incremented by 4 (fullword address). The chain flag in the fetched CW indicates whether or not the updated OUTCWAR points to a valid CW. If the chain bit is off in the fetched CW, the 'OUTCWAR valid' latch is reset.

Byte 0, bit 4: Program Requested Level 3 Interrupt—This bit indicates that the CA L3 interrupt was initiated because the control program set the CA mode register byte 1, bit 0 (set CA L3 request).

Byte 0, bit 5: Program Requested Abort/Level 3 Interrupt—This bit indicates that the current level 3 interrupt was caused by executing an Output X'57' with byte 1, bit 1 on. This bit is reset when Output X'57' is executed with byte 1, bit 3 on (reset L3 request).

Byte 0, bit 6: Program Requested Attention—This bit indicates that the program has requested Attention by executing an Output X'55' instruction with byte 0, bit 6 on. It is reset when the host channel accepts the status byte containing Attention.

Byte 0, bit 7: Channel Adapter Active—This bit indicates that the CA is currently executing a channel command. It is set by completion of the initial selection for the command and is reset when the host channel accepts Device End status for that command.

Byte 1, bit 0: Command Chaining—This bit is set by the Type 2 CA hardware when the 'suppress out' tag line is up at the time the channel accepts ending status from the CA. It is reset at the end of the first level 3 interrupt to occur after the latch has been set each time a valid command is decoded during initial selection, or when suppress out fails and the CA is not active.

Byte 1, bit 1: Write Break Command Remember–This bit is set by the channel adapter when a Write Break command (X'09') is received. It is reset when the host channel accepts Device End status for that command.

Byte 1, bit 2: Channel Stop/Interface Disconnect—This bit is set by the channel adapter when a Channel Stop or an Interface Disconnect is detected on the channel interface. This bit is reset by an Output X'57', byte 1, bit 6.

Byte 1, bit 3: Selective/System Reset—This bit is set by the CA hardware when a system reset or a selective reset is detected on the interface. It is reset by Output X'57', byte 1, bit 5.

Byte 1, bit 4: This bit is 0.

Byte 1, bit 5: Channel Read Command Remember–This bit is set when a Read command is accepted by the CA during initial selection. It is reset when the CPU accepts the Device End status for this command.

Byte 1, bit 6: CA-2 Selected—This bit indicates that the second channel adapter (CA-2) has been selected for operation by an Output X'57'. This bit is always 0 if only one channel adapter is installed.

Byte 1, bit 7: CA-1 Selected—This bit indicates that the first channel adapter (CA-1) has been selected for operation by an Output X'57'.

Input X'56' (Channel Adapter Check Register–CACHKR) This instruction loads a general register with the contents of the CA check register. All the bits of the check register set a level 1 interrupt request. By executing this input, the level 1 interrupt check routine can determine the exact cause of the CA level 1 check. Except for the bus out checks, all the latches in this register are automatically reset

when an Output X'57' is executed to reset the adapter's L1 interrupt request. This input instruction is recognized only after a CA interrupt request is set.

Byte 0, bit 0: Invalid CWAR Address—This bit is set when the CWAR associated with the current channel operation points to a storage address above 64K bytes.

Byte 0, bit 1: Invalid Control Word Format—This bit is set when (1) an OUT STOP control word is fetched when executing a channel Write command, (2) an IN control word is fetched when executing a channel Read command, or (3) an IN, OUT, or OUT STOP control word containing a data count of zero is fetched.

Note: A programming error in the 3705 that causes this hardware error may result in an Interface Control check on the system channel and "hang" the CPU. Whether this will occur depends on the CPU and channel type.

Byte 0, bit 2: Cycle Steal Address Check—This bit is set when the CCU signals the channel adapter that an address error has occurred during a cycle steal operation. It indicates that the cycle steal address (1) is beyond the storage capacity of the machine, (2) is of incorrect parity, or (3) points to a protected area of storage.

Byte 0, bit 3: CWAR/Data Buffer Check—This bit indicates that either the INCWAR, OUTCWAR, data 1, or data 2 register contained incorrect parity when access was attempted for either an input instruction or data transfer to the channel during a Read command.

Byte 0, bit 4: CCU Outbus Check—This bit is set (1) when data from an output instruction to the CA has incorrect parity on the CCU Outbus, or (2) when, during a cycle steal, the data from storage contained incorrect parity.

Byte 0, bit 5: CCU Inbus Check—This bit indicates that incorrect parity was present on the Inbus during a CA cycle steal operation or input instruction.

Byte 0, bit 6: Channel Bus Out Check—This bit indicates that a parity check was detected on the channel bus out lines during initial selection or data transfer.

Byte 0, bit 7: This bit is 0.

Byte 1, bits 0-3: These bits are 0.

Byte 1, bit 4: Channel Bus In Check (Interface A)—This bit indicates that the sense, status, data, or address byte presented to interface A did not have correct parity.

Byte 1, bit 5: Channel Bus In Check (Interface B)—This bit indicates that the sense, status, data, or address byte presented to interface B did not have the correct parity.

Byte 1, bits 6-7: These bits are 0.

Input X'58' (Channel Bus Out Diagnostic Register–CBODR)
This instruction loads a general register with the current state of the host processor 'bus out' lines. However, byte 0 and byte 1, bit 0 are accessible only in the diagnostic wrap mode, and byte 1, bits 1-7 are accessible when the adapter is selected and in a level 1 or level 3 interrupt state.

Byte 0, bits 0-7: Channel Bus Out bits 0-7.

Byte 1, bit 0: Channel Bus Out Parity Bit—This bit may be used in diagnostic mode to check the CA error-detection circuits.

Byte 1, bit 1: This bit is 0.

Byte 1, bit 2: Transfer Byte 1—This bit indicates that the CA is currently transferring an odd numbered byte across the channel interface.

Byte 1, bit 3: Transfer Byte 2—This bit indicates that the Type 2 CA is currently transferring an even numbered byte across the channel interface.

Byte 1, bit 4: Interface A Enabled—This bit is 1 when channel interface A of the Channel Adapter is currently enabled.

Byte 1, bit 5: Interface B Enabled—This bit is 1 when channel interface B of the channel adapter is currently enabled.

Byte 1, bit 6: CSAR Byte X, Bit 6—This bit is 1 when byte X, bit 6 of the cycle-steal address register (with Extended Addressing on 3705 Models A–H only) is 1.

Byte 1, bit 7: CSAR Byte X, Bit 7—This bit is 1 when byte X, bit 7 of the cycle-steal address register (with Extended Addressing on 3705 Models A–H only) is 1.

Input X'59' (Cycle-Steal Address Register–CSAR)
This instruction loads a general register with the current storage data address from the cycle-steal address register while data transfer is in progress.

Byte 0, bits 0-7: CSAR byte 0, bits 0-7.

Byte 1, bits 0-7: CSAR byte 1, bits 0-7.

Input X'5A' (CA Data Buffer–CADB)
This instruction loads a general register with incoming data from the channel adapter data buffer.

Byte 0, bits 0-7: Data buffer byte 0, bits 0-7. Any nonstandard channel command is available in this byte for level 3 program interrogation.

Byte 1, bits 0-7: Data buffer byte 1, bits 0-7.

Input X'5B' (Channel Adapter Tag Diagnostic Register)
This instruction loads a general register with a combination of bits to indicate the state of the channel tag lines for diagnostic purposes. This input can be used only when the adapter is in diagnostic mode.

Byte 0, bit 0: Select Out/Hold Out—This bit indicates the state of the diagnostic 'select out/hold out' tag line.

Byte 0, bit 1: Address Out—This bit indicates the state of the diagnostic 'address out' tag line.

Byte 0, bit 2: Command Out—This bit indicates the state of the diagnostic 'command out' tag line.

Byte 0, bit 3: Service Out—This bit indicates the state of the diagnostic 'service out' tag line.

Byte 0, bit 4: Operational Out—This bit indicates the state of the diagnostic 'operational out' tag line.

Byte 0, bit 5: Suppress Out—This bit indicates the state of the diagnostic 'suppress out' tag line.

Byte 0, bits 6-7: These bits are 0.

Byte 1, bit 0: Select Out—This bit indicates the state of the diagnostic 'select out' tag line.

Byte 1, bit 1: Request In—This bit indicates the state of the diagnostic 'request in' tag line.

Byte 1, bit 2: Operational In—This bit indicates the state of the diagnostic 'operational in' tag line.

Byte 1, bit 3: Address In—This bit indicates the state of the diagnostic 'address in' tag line.

Byte 1, bit 4: Status In—This bit indicates the state of the diagnostic 'status in' tag line.

Byte 1, bit 5: Service In—This bit indicates the state of the diagnostic 'service in' tag line.

Byte 1, bit 6: This bit is 0.

Byte 1, bit 7: Generate Busy—This bit indicates that the channel adapter is busy.

Input X'5C' (CA Command Register—CMDR)
This instruction loads a general register with the current channel command being executed. Byte 1 indicates the current or last control word type executed.

Byte 0, bit 0: Test I/O—This bit is 1 when the command received from the host processor was a Test I/O (X'00').

Byte 0, bit 1: Write—This bit is 1 when the command received from the host processor was a channel Write (X'01') command.

Byte 0, bit 2: Read—This bit is 1 when the command received from the host processor was a channel Read (X'02') command.

Byte 0, bit 3: No-Op—This bit is 1 when the command received from the host processor was a No-Op (X'03').

Byte 0, bit 4: Sense—This bit is 1 when the command received from the host processor was a Sense (X'04') command.

Byte 0, bit 5: This bit is 0.

Byte 0, bit 6: Write Break—This bit is 1 when the command received from the host processor was a Write Break (X'09') command.

Byte 0, bit 7: This bit is 0.

Byte 1, bit 0: OUT Control Word—This bit is 1 when the current or last control word in use was an OUT control word.

Byte 1, bit 1: OUT STOP Control Word—This bit is 1 when the current or last control word in use was an OUT STOP control word.

Byte 1, bit 2: IN Control Word—This bit is 1 when the current or last control word in use was an IN control word.

Byte 1, bit 3: TIC Control Word—This bit is 1 when the current or last control word in use was a TIC control word.

Byte 1, bit 4: Nonstandard Command—A 1 in this position indicates that a nonstandard command was issued. The command byte is available for examination by the 3705 control program, in byte 0 of register X'5A'.

Byte 1, bit 5: Interface A—A 1 in this position indicates that the Type 3 CA currently is switched to interface A.

Byte 1, bit 6: Interface B—A 1 in this position indicates that the Type 3 CA currently is switched to interface B.

Byte 1, bit 7: Write IPL—This bit is 1 when the command received from the host processor was a Write IPL (X'05') command.

Type 2 and Type 3 CA Output Instructions

Output X'50' (Inbound Data Control Word Address Register–INCWAR)
This instruction loads the INCWAR with the storage address of the control word (CW) to be fetched by the CA cycle-steal hardware when a channel Write, Write Break, or Write IPL command is decoded. The CA recognizes this instruction only after setting a CA interrupt request.

Programming Note
All CWs must begin on a halfword boundary and reside in the lower 64K bytes of storage. CW chaining or a TIC (transfer in channel) to an address above 64K causes a CW error condition resulting in a CA level 1 interrupt.

Byte 0, bits 0-7: INCWAR bits 0-7.

Byte 1, bits 0-7: INCWAR bits 8-15.

Output X'51' (Outbound Data Control Word Address Register–OUTCWAR)
This instruction loads the OUTCWAR with the storage address of the control word (CW) to be fetched by the CA cycle-steal hardware when a channel Read command is decoded. The instruction is recognized by the CA only following the setting of a CA interrupt request.

Programming Note
All CWs must begin on a halfword boundary and reside in the lower 64K bytes of storage. CW chaining or TIC (transfer in channel) to an address above 64K causes a CW error condition resulting in a CA level 1 interrupt.

Byte 0, bits 0-7: OUTCWAR bits 0-7.

Byte 1, bits 0-7: OUTCWAR bits 8-15.

Output X'53' (Channel Adapter Sense Register—CASNSR)
This output instruction is used to set the abort indication in the CA sense register. The CA recognizes this instruction only after setting a CA interrupt request while the CA is in the CA active state. If Output X'53' is issued while in a CA interrupt state and the CA is neither active nor in the diagnostic wrap state, the output is ignored, and no indication of this is returned to the control program. The control program should always determine the active/inactive state of the CA before issuing this output instruction.

Programming Note
The setting of any CASNSR bit causes the Unit Check bit to be set in the CA status register and also causes the termination of any data transfer that may have been in progress. CASNSR is reset during initial selection whenever the CA accepts a command other than Sense, Test I/O, or No-Op.

Byte 0, bit 0: Command Reject—This output allows a level 3 interrupt program to set the Command Reject sense bit. Execution of this output also causes Unit Check to be set in the status register.

Byte 0, bit 1: Intervention Required—This bit should never be set by the control program during normal operation.

Byte 0, bits 2-3: These bits are unused.

Byte 0, bit 4: Set Data Check—This bit is set to 1 by the control program during a level 3 interrupt. The CA must be in the active state or in diagnostic mode.

Byte 0, bits 5-6: These bits are unused.

Byte 0, bit 7: Abort—This bit can be set by the control program during a CA interrupt if the CA active state exists. Abort indicates to the host processor that the control program has halted its channel operation abnormally.

Byte 1, bits 0-7: These bits are unused.

Output X'54' (Channel Adapter Status Register—CASTR)
This instruction sets the channel adapter status register bits. The instruction is recognized by the CA only following the setting of a CA level 1 or level 3 interrupt request while the CA is in the CA active state or in the diagnostic wrap state.

Byte 0, bit 0: Attention—When the CA is both active and has either its level 1 or level 3 interrupt request latch set, a 1 bit in this position is used to include Attention along with other ending status such as Device End.

Byte 0, bit 1: Status Modifier—This bit may have special applications in controlling channel data transfers. Status Modifier should convey to the host processor a unique indication for the particular command being executed.

Byte 0, bit 2: This bit is unused.

Byte 0, bit 3: Busy—This bit is presented as initial status to all host processor channel commands if (1) initial selection is attempted before Device End status has been signaled to the host processor for the command currently being executed, or (2) the channel adapter has its level 1 or level 3 interrupt request latch set.

If status is available at this time, it is presented along with Busy status. If status has been stacked, that status is also presented along with Busy.

Byte 0, bit 4: Channel End—This bit is set to indicate that the controller has completed the data transfer portion of the channel command in progress. Channel End is set by the CA hardware for each host processor channel command. It may also be set when the CA is in an active state with a level 1 or level 3 request pending and Channel End has not already been presented to the channel for the command being executed.

Byte 0, bit 5: Device End—This bit is set to indicate that the controller has finished with the current host processor channel command and is ready to accept another command from the channel. CE and DE are not always presented together. The conditions under which they are presented separately are discussed under *Status Servicing* in Chapter 10. When CE and DE are presented separately, the CA requests a level 3 interrupt after the channel accepts CE. When the interrupt request is reset (Output X'57'—channel adapter mode register), the CA sends DE and any other status (Attention, Status Modifier, Unit Exception) that may have been set during execution of the interrupt handling routine.

Byte 0, bit 6: This bit is unused.

Byte 0, bit 7: Unit Exception—This bit is set during initial status to notify the channel that the control routine has not set up a CA control word to handle this particular host processor channel command. UE is presented with DE to more efficiently notify the channel that a CW is invalid. Unit Exception can be used in this manner to break host processor channel command chaining without going through another selection sequence when the controller no longer needs service.

When two channel adapters are installed in the controller, and an IPL command is in progress to one of the CAs, Unit Exception is presented as initial status to all commands, except Write IPL, issued to the other CA.

Byte 1, bits 0-7: These bits are unused.

Output X'55' (Channel Adapter Control Register–CACR)
This instruction sets the CA control register bits. The instruction is recognized by the CA only following the setting of a CA select and a CA interrupt request. The CA need not be in the CA active state.

Byte 0, bits 0-1: These bits are unused.

Byte 0, bit 2: INCWAR Valid—This bit is set by the control program when the control word address register for inbound data transfer (channel Write command) points to the storage location containing the control word to be used for controlling this type of data transfer.

To initialize the CA, the control program sets this bit during a CA-requested level 3 interrupt.

Byte 0, bit 3: OUTCWAR Valid—The control program sets this bit when the control word address register for outbound data transfer (that is, a channel Read command) points to the storage location containing the control word to be used for controlling this type of data transfer. To initialize the CA, the control program sets this bit during a CA-requested level 3 interrupt.

Byte 0, bits 4-5: These bits are unused.

Byte 0, bit 6: Program Requested Attention—When this bit has been set, the Attention status is presented to the channel as soon as the CA's level 3 interrupt request latch has been reset provided the 3705 is not executing a selection sequence or has not come to a hard stop. The bit is reset when the channel accepts the status byte containing the attention bit. The Type 3 CA presents the Attention status to both channels.

Byte 0, bit 7: This bit is unused.

Byte 1, bits 0-7: These bits are unused.

Output X'56' (Reset Control Register–CACR)
This instruction is executed to reset the 'INCWAR valid' and the 'OUTCWAR valid' latches.

Byte 0, bits 0-1: These bits are unused.

Byte 0, bit 2: Reset INCWAR Valid—A 1 in this position causes the 'INCWAR valid' latch to be reset.

Byte 0, bit 3: Reset OUTCWAR Valid—A 1 in this position causes the 'OUTCWAR valid' latch to be reset.

Byte 0, bits 4-7: These bits are unused.

Byte 1, bits 0-5: These bits are unused.

Byte 1, bit 6: This bit being on disables the CA from accepting nonstandard channel commands.

Byte 1, bit 7: This bit being on enables the CA to accept nonstandard channel commands by responding to the channel with a Channel End initial status, and requesting a level 3 interrupt.

Output X'57' (Channel Adapter Mode Register–CAMR)
This instruction loads the channel adapter mode register with the bits set in the general register. Byte 1 of this register can be loaded at any time to initialize or halt the CA.

Byte 0, Bit 0: Set IPL Attention (Models A–H without IBM Engineering Change 318882 installed–check with your IBM Service Representative)—A 1 in this position causes the channel adapter 'attention' latch to be set (see Note). This is done as soon as the adapter hardware determines that the channel is not examining the status register. The Type 3 CA offers Attention to both channels. Acceptance of the status byte by either channel causes the bit to be reset.

Note: This bit is ignored unless the channel adapter is in diagnostic mode, or the 3705 is in IPL Phase 3 (not initialized).

Byte 0, bit 0: Set Sense Unit Exception Latch (Models A–H with IBM Engineering Change 318882 installed or Models J–L–check with your IBM Service Representative)–With this bit set to 1, a Sense Command ends with CE, DE, and UE final status (*after* the sense byte transfer). The 'Sense Unit Exception' latch cannot be set unless the 3705 is in the initialized state (IPL Phase 3 reset). The latch resets automatically if the 3705 enters the not initialized state. The IPL Unit Exception' latch, if set by Output X'57', bit 0.6, overrides the 'Sense Unit Exception' latch.

Byte 0, bit 1: Set IPL Channel End—A 1 in this position causes the channel adapter 'channel end status' latch to be set once the adapter hardware determines that the 'channel end remembrance' latch is not on. (See Note.)

Byte 0, bit 2: This bit is reserved.

Byte 0, bit 3: Set Asynchronous Device End—A 1 in this position causes the channel adapter 'device end status' latch to be set. The Type 3 CA offers Device End to both channels. Acceptance of the status byte by either channel causes the bit to be reset.

Byte 0, bit 4: Set IPL Unit Check—A 1 in this position causes the channel adapter 'unit check status' latch to be set (see Note). This indication should not be set without setting byte 0, bit 7 (IPL not initialized).

Byte 0, bit 5: Reset Sense Unit Exception—In diagnostic mode only, setting this bit to "1" resets the 'Sense Unit Exception' latch.

Byte 0, bit 6: Set IPL Unit Exception—A 1 in this position causes the selected CA to present Unit Exception initial status to all Sense commands (see Note). This bit is set by the ROS program to prevent two host processors from simultaneously trying to IPL the controller when two channel adapters are installed. A 0 in this position causes a reset of the channel adapter 'IPL Unit Exception' latch. However, it is the responsibility of the loader program to turn this bit off.

Byte 0, bit 7: Set IPL Not-Initialized—A 1 in this position causes the channel adapter not-initialized sense bit to be set when the channel is not executing a Sense command (see Note). The not-initialized sense bit is reset when the ROS program executes an Output X'77' instruction with byte 0, bit 0 set to 1.

Note: This bit is ignored unless the channel adapter is in diagnostic mode, or the 3705 is in IPL Phase 3 (not initialized).

Byte 1, bit 0: Set CA Level 3 Interrupt Request—A 1 in this position causes the CA to request a level 3 interrupt once the CA is in the inactive state, with no outstanding status and no channel chaining indicated. The latch is reset at the end of the first level 3 interrupt to occur after it has been set.

Byte 1, bit 1: Set Program Abort—When an Output X'57' is executed with a 1 bit in this position while a channel operation of 'Write', 'Write Break', 'Write IPL', or 'Read' is in progress, the operation is terminated with an ending status of CE, DE, UC, and the abort sense bit is set. Once the status is accepted by the channel, a level 3 interrupt is requested. If other than one of the mentioned channel operations is in progress, the level 3 interrupt is requested at the completion of the operation. If no channel operation is in progress, the level 3 interrupt is requested immediately. Program abort is reset when the level 3 interrupt is reset.

Programming Note

The interrupt program should invalidate the CWARs, if necessary, by resetting the CWAR-valid flags with an Output X'56' instruction. If the program does reset the CWAR-valid flags, they must be restored by an Output X'55' before another channel data transfer can be initiated.

Byte 1, bit 2: Reset CA Level 1 Interrupt Request—A 1 in this position resets the CA 'level 1 interrupt request' latch. This should be the last action the control program takes before leaving a CA-initiated level 1 interrupt. All check latches, except 'bus out check', contained in Input X'55' are reset when this output occurs.

Byte 1, bit 3: Reset CA Level 3 Interrupt Request—A I in this position resets the CA 'level 3 interrupt request' latch. However, it does not necessarily reset the cause of the interrupt request.

Byte 1, bit 4: Select CA—A 1 in this position selects CA-1. A 0 in this position selects CA-2. The control program must ensure that the state of this bit is correct any time an Output X'57' is issued.

Byte 1, bit 5: Reset Selective/System Reset—A I in this position resets the selective system reset condition. However, byte 1, bit 3 of this output must also be 1 to reset the resulting level 3 interrupt request.

Byte 1, bit 6: Reset Channel Stop/Interface Disconnect—A 1 in this position resets the Channel

Stop or Halt I/O indication set when either of these sequences is received from the channel interface. However, byte 1, bit 3 of this output must also be 1 to reset the resulting level 3 interrupt request.

Byte 1, bit 7: Diagnostic Wrap Mode—A 1 in this position forces the channel adapter to go offline and places it in the diagnostic wrap state. A 0 places the CA back online.

Output X'58' (Channel Bus Out Diagnostic Register—CBODR)
The channel bus out diagnostic register (CBODR) is used to simulate I/O 'bus out' when the CA is in diagnostic wrap state. Byte 0, bits 0-7 and byte 1, bit 0 of this output are available only when the adapter is in the diagnostic wrap mode.

Byte 0, bits 0-7: Channel Bus Out bits 0-7.

Byte 1, bit 0: Channel Bus Out Parity bit. This bit may be used in diagnostic state to check the CA error-detection circuits.

Byte 1, bits 1-6: These bits are unused.

Byte 1, bit 7: Reset CA—A 1 in this position causes the CA currently selected to be reset. Its intended use is for diagnostic programs, and it is not necessary for normal channel adapter operation.

Output X'59' (Type 3 Channel Adapter Diagnostic Busy)
This instruction makes either or both Type 3 Channel Adapter interfaces Busy for diagnostic purposes.

Byte 0, bit 0: Set Interface A Busy—This bit is set on to cause Interface A to respond with an initial status of Busy to all channel initiated selection sequences.

Byte 0, bit 1: Set Interface B Busy—A 1 in this position causes Interface B to respond with a Busy status to all channel-initiated sequences.

Byte 0, bits 2-3: These bits are unused.

Byte 0, bit 4: Reset Interface A Busy—A 1 in this position resets Interface A Busy (if previously set by an Output X'59'). If the Interface A Busy condition is already reset, the output performs no operation and is ignored.

Byte 0, bit 5: Reset Interface B Busy—A 1 in this position resets Interface B Busy (if previously set by an Output X'59'). If Interface B Busy condition is already reset, the output performs no operation and is ignored.

Byte 0, bits 6-7: These bits are unused.

Byte 1, bits 0-7: These bits are unused.

Programming Note
Do not execute Output X'59' with both the set and reset bits on for either interface. An Output X'59' with either bits 0 and 3 or 1 and 4 on in byte 0 causes the respective hardware latch to reach an indeterminate state.

Output X'5A' (Channel Adapter Data Buffer—CADB)
This instruction loads the CA data buffer with the data to be sent to the host processor channel for either normal or diagnostic operations.

Byte 0, bits 0-7: Data Buffer byte 0, bits 0-7.

Byte 1, bits 0-7: Data Buffer byte 1, bits 0-7.

Output X'5B' (Channel Adapter Tag Diagnostic Register)
This instruction loads the CA tag diagnostic register with a combination of bits from a general register to raise channel tag lines for diagnostic purposes. The characteristic of this register is such that a 1 sets the corresponding bit, and a 0 resets it. Therefore, care should be taken when issuing this output to ensure the register's integrity.

This output is accessible only when the CA is in the diagnostic wrap mode.

Byte 0, bit 0: Select Out/Hold Out—A 1 in this position raises the inbound 'select out/hold out' tag line.

Byte 0, bit 1: Address Out—A 1 in this position raises the 'address out' tag line.

Byte 0, bit 2: Command Out—A 1 in this position raises the 'command out' tag line.

Byte 0, bit 3: Service Out—A 1 in this position raises the 'service out' tag line.

Byte 0, bit 4: Operational Out—A 1 in this position raises the 'operational out' tag line.

Byte 0, bit 5: Suppress Out—A 1 in this position raises the 'suppress out' tag line.

Byte 0, bits 6-7: These bits are unused.

Byte 1, bits 0-7: These bits are unused.

Remote Program Loader Input Instructions

Input X'68' (Level 1 Status)
This instruction allows the control program to examine the contents of the level 1 status register to determine the cause of a remote program loader interrupt.

Byte 0, bit 0: This bit is set 0.

Byte 0, bit 1: Outbus Parity Error—This bit is set to 1 when a parity error is detected on the Outbus from the CCU to the disk controller. This is an error condition that causes a program level 1 interrupt request.

Byte 0, bits 2-7: These bits are 0.

Byte 1, bits 0-2: These bits are 0.

Byte 1, bit 3: This bit is set to 1 when a Write command is issued to the disk and the write operation is not enabled. This is an error condition that causes a program level 1 interrupt request.

Byte 1, bits 4-7: These bits are 0.

Input X'69' (Level 3 Status)
This register can be accessed only after an interrupt request or when the disk controller is in the reset state.

Byte 0, bit 0: Index—This bit is set to 1 when the index is detected and the interrupt on index bit (Output X'68', byte 1, bit 7) is set.

Byte 0, bit 1: Read Sync—This bit is set on when the disk controller is in sync on a read operation (for diagnostic purposes).

Byte 0, bits 2-5: Head Access Counter—These bits form a counter that controls the head access stepping motor. The bits are named access 0 through access 3 respectively. They are used by the control program to determine if the head has moved after execution of an Output X'68' with byte l, bit l on.

Byte 0, bit 6: Head Engage—This bit is set on when the 'head engage' latch is set on.

Byte 0, bit 7: I/O Data Service Request—This bit is set on when a data service request is present for an input/output operation.

Byte 1, bit 0: Head Disengaged— This bit is set on when the disk head is disengaged and the current is dropped from the disk motor.

Byte 1, bits 1-3: These bits are 0.

Byte 1, bit 4: Overrun—This bit is set on when an I/O overrun is detected during a data transfer from the disk controller to the CCU.

Byte 1, bits 5-7: These bits are 0.

Input X'6A' (Parallel Data Register)
This instruction places the contents of the disk controller's parallel data register on the CCU Inbus. This instruction is used to read data into storage during an I/O data transfer and for diagnostic purposes.

Input X'6B' (Control Program Load Register)
This instruction is used to provide information required by the IPL and program load phases. The bits in this register are reset to 0 when the Reset push button is pressed or when a power-on reset occurs.

Byte 0, bit 0: Preserve Storage—A1 in this position indicates that the contents of storage are to be preserved until a storage dump is taken.

Byte 0, bit 1: Control Program IPL—This bit should be on when an IPL is initiated by the control program.

Byte 0, bit 2: This bit is set to 0.

Byte 0, bit 3: Host Initiated IPL—This bit should be on when an IPL is initiated by a host processor command.

The remaining bits of this register are not present in the controller.

Remote Program Loader Output Instructions

Output X'68' (Control)
This instruction prepares for subsequent read or write operations by controlling the access arm.

Byte 0, bit 0: Low Current—This bit sets the current level to the disk for a write operation. When writing on tracks 45 through 76, this bit must be set to 1 (low current). The bit must be 0 (high current) when writing on tracks 0 through 41. Tracks 42, 43, and 44 can use either high or low current.

Byte 0, bit 2: Reset Low Current—A 1 in this position causes the low current indication (byte 0, bit 0 of this output) to be reset.

Byte 0, bit 3: Reset Access Counter—A 1 in this position resets the head access counter (byte 0, bits 2-5 of Input X'69') to Access 0.

Byte 0, bits 4-7: These bits are unused.

Byte 1, bit 0: Reset L3 Interrupt Latch—A 1 in this position resets the 'interrupt on index' latch that is set as a result of byte 1, bit 7 of this output being on.

Byte 1, bit 1: Head Move Enable—A 1 in this position allows the head to be moved. A 0 inhibits all head movement.

Byte 1, bit 2: Head Direction—A 1 in this position indicates that the head is to be moved in a forward direction and a 0 indicates a reverse direction.

Byte 1, bit 3: Set Status Latches—A 1 in this position sets the diagnostic status latches in the disk controller.

Byte 1, bit 4: Head Engage—A 1 in this position sets the 'head engage' latch, which allows the disk head to become active for a read or write operation.

Byte 1, bit 5: Disk Controller Reset—A 1 in this position resets the disk controller. All registers, latches, and counters in the disk controller except the head access counter are reset.

Byte 1, bit 6: L1 and L3 Interrupt Reset—A 1 in this position resets the 'level 1 interrupt' and the 'level 3 interrupt' latches in the disk controller and all the controller status latches.

Byte 1, bit 7: Set L3 Interrupt on Index—A 1 in this position causes the disk controller to request a level 3 interrupt on index.

Output X'69' (Read/Write)

Byte 0, bit 0: This bit is unused.

Byte 0, bit 1: I/O Write—A 1 in this position initiates an input/output write operation to the disk.

Byte 0, bit 2: I/O Read—A 1 in this position initiates an input/output read operation to the disk.

Byte 0, bits 3-7: These bits are unused.

Byte 1, bits 0-7: These bits are unused.

Output X'6A' (Parallel Data Register)
This instruction loads the parallel data register in the disk controller with the information on the CCU Outbus. This instruction is used to write data on the disk during an I/O data transfer or for diagnostic purposes.

Output X'6B' (Control Program Load Register)
This register is used to pass information required by the IPL and program load phases. The bits of this register are reset to 0 when the Reset push button is pressed or when a power-on reset occurs.

Byte 0, bit 0: Preserve Storage—This bit must be set to 1 by the control program if the contents of storage are to be preserved so that the load program can dump the remote storage contents back to the host processor.

Note: *This bit does not initiate a dump operation. It only informs the load program to preserve storage until a dump is complete.*

Byte 0, bit 1: Control Program IPL—This bit must be set to 1 by the control program to inform the load programs that an IPL operation was initiated by the control program.

Byte 0, bit 2: This bit is unused.

Byte 0, bit 3: Host Initiated IPL—This bit must be set to 1 by the control program to inform the load programs that an IPL operation was initiated by a host processor command.

The remaining bits of this register are not present in the controller.

CCU Input Instructions

Input X'70' (Storage Size Installed)
This instruction causes the register specified by R to be loaded with a bit combination that indicates the amount of storage installed in the controller.

The register bits are set to one of the values shown below to indicate the amount of storage installed in the controller.

3705-II Bit Settings

Storage Size	Byte 0, bit 2 3 4 5 6	Hex value of byte 0
32K	0 0 0 0 1	X'02'
64K	0 0 0 1 0	X'04'
96K	0 0 0 1 1	X'06'
128K	0 0 1 0 0	X'08'
160K	0 0 1 0 1	X'0A'
192K	0 0 1 1 0	X'0C'
224K	0 0 1 1 1	X'0E'
256K	0 1 0 0 0	X'10'
320K	0 1 0 1 0	X'14'
384K	0 1 1 0 0	X'18'
448K	0 1 1 1 0	X'1C'
512K	1 0 0 0 0	X'20'

Over 256K sets bit 1-7 to 1.

3705-I Bit Settings

Storage Size	Byte 0, bit 0 1 2 3	Hex value of byte 0
16K	0 0 0 1	X'10'
48K	0 0 1 1	X'30'
80K	0 1 0 1	X'50'
112K	0 1 1 1	X'70'
144K	1 0 0 1	X'90'
176K	1 0 1 1	X'B0'
208K	1 1 0 1	X'D0'
240K	1 1 1 1	X'F0'

3704 Bit Settings

Storage Size	Byte 0, bit 0 1 2 3	Hex value of byte 0
16K	0 0 0 1	X'10'
32K	0 0 1 0	X'20'
48K	0 0 1 1	X'30'
64K	0 1 0 0	X'40'

All bit positions of byte 1 of this register are 0.

Input X'71' (Panel Address/Data Entry Digits)
This instruction causes the register specified by R to be loaded according to the setting of the Address/Data switches on the control panel.

The action taken for each register bit position is given below.

Byte X, bits 4-7: Address/Data A—On a 3705 with Extended Addressing, these bits are loaded with the information from switch A on the control panel.

Byte 0, bits 0-7: Address/Data B & C—These bits are loaded with the information from switches B and C on the control panel.

Byte 1, bits 0-7: Address/Data D & E—These bits are loaded with the information from switches D and E on the control panel.

Input X'72' (Panel Display/Function Select Switch Controls)
This instruction causes the register specified by R to be loaded with information indicating the position of the Display/Function Select switch on the control panel.

Byte 0, bits 0-2: These bits are 0.

Byte 0, bit 3: Storage Address—This bit indicates that the Display/Function Select switch is in the STORAGE ADDRESS position.

Byte 0, bit 4: Register Address—This bit indicates that the Display/Function Select switch is in the REGISTER ADDRESS position.

Byte 0, bits 5-7: These bits are 0.

Byte 1, bit 0: This bit is 0.

Byte 1, bit 1: Function Select 1—This bit indicates that the Display/Function Select switch is in the FUNCTION 1 position.

Byte 1, bit 2: Function Select 2—This bit indicates that the Display/Function Select switch is in the FUNCTION 2 position.

Byte 1, bit 3: Function Select 3—This bit indicates that the Display/Function Select switch is in the FUNCTION 3 position.

Byte 1, bit 4: Function Select 4—This bit indicates that the Display/Function Select switch is in the FUNCTION 4 position.

Byte 1, bit 5: Function Select 5—This bit indicates that the Display/Function Select switch is in the FUNCTION 5 position.

Byte 1, bit 6: Function Select 6—This bit indicates that the Display/Function Select switch is in the FUNCTION 6 position.

Byte 1, bit 7: This bit is 0.

Input X'73' (Insert Key)
This instruction is associated with storage protection. It causes the key addressed by the last Output X'73' to be inserted into byte 1, bits 5-7 of the register specified by R. All other bits of the register are set to 0. See *Storage Protect* in Chapter 5.

Input X'74' (Lagging Address Register)
This instruction causes the contents of the lagging address register to be transferred to the register specified by R.

If this instruction is executed at program levels 2, 3, or 4, the address from the LAR is that of the last instruction executed before the input instruction. If this instruction is executed in program level 1, the address from the LAR is that of the last instruction executed before entering level 1.

Input X'76' (Adapter Level 1 Interrupt Requests)
This instruction is associated with program level 1 interrupt requests. It loads the register specified by R with a combination of bits to indicate the origin of an adapter level 1 interrupt request.

Byte 0, bit 0: Type 4 CA-1, CA-2, CA-3, or CA-4 L1—This bit indicates that Type 4 CA-1, CA-2, CA-3, or CA-4 has requested a program level 1 interrupt.

Byte 0, bit 1: Type 2 or 3 Scanner-1 (or Type 1 Scanner) L1—This bit indicates that a Type 1 Scanner or a Type 2 or 3 Scanner-1 has requested a program level 1 interrupt.

Byte 0, bit 2: Type 2 or 3 Scanner-2 L1—This bit indicates that a Type 2 or 3 Scanner-2 has requested a program level 1 interrupt.

Byte 0, bit 3: Type 2 or 3 Scanner-3 L1—This bit indicates that a Type 2 or 3 Scanner-3 has requested a program level 1 interrupt.

Byte 0, bit 4: Type 2 or 3 Scanner-4 L1—This bit indicates that a Type 2 or 3 Scanner-4 has requested a program level 1 interrupt.

Byte 0, bit 5: Type 1, 2, or 3 CA-1 L1 or Selected Type 4 CA L1—This bit indicates that a Type 1 CA, a Type 2 or Type 3 CA-1, or a selected Type 4 CA has requested a program level 1 interrupt. An Input X'67' instruction determines which Type 4 CA is selected.

Byte 0, bit 6: Type 2 or 3 CA-2 L1—This bit indicates that a Type 2 or Type 3 CA-2 has requested a program level 1 interrupt.

Byte 0, bit 7: Remote Loader L1 Request—This bit indicates that the disk controller has requested a program level 1 interrupt.

Byte 1, bits 0-7: These bits are 0.

Input X'77' (Adapter Level 2 or 3 Interrupt Requests)
This instruction is associated with program level 2 and level 3 interrupt requests. It loads the register specified by R with a combination of bits to indicate the origin of an adapter level 2 or 3 interrupt request.

When priority selection is required with more than one Type 4 CAs, this instruction sets or rests the selected latch in each Type 4 CA according to the state of the "CA4 has priority" latch. It also resets the "prime priority select" latch.

Byte 0, bit 0: This bit is 0.

Byte 0, bit 1: Type 1, 2, or 3 Scanner L2—This bit indicates that a Type 1, Type 2, or Type 3 Scanner has requested a program level 2 interrupt.

Byte 0, bits 2-7: These bits are 0.

Byte 1, bit 0: Type 4 CA L3—This bit indicates that a Type 4 CA-1, CA-2, CA-3, or CA-4 has requested a program level 3 interrupt.

Byte 1, bit 1: Remote Loader L3 Request—This bit indicates that the disk controller has requested a program level 3 interrupt.

Byte 1, bit 2: Type 2 or 3 CA-2 L3—This bit indicates that a Type 2 or Type 3 CA-2 has requested a program level 3 interrupt.

Byte 1, bit 3: Type 1 or Selected Type 4 CA Data/Status L3—This bit indicates that a Type 1 or selected Type 4 CA has requested a program level 3 data service interrupt.

Byte 1, bit 4: Type 1, 2, or 3 CA-1 or selected Type 4 CA L3—This bit indicates that a Type 2 or Type 3 CA-1 has requested a program level 3 interrupt, or a Type 1 or selected Type 4 CA has requested a program level 3 initial selection interrupt.

Byte 1, bits 5 and 6: Type 4 CA Selected—These bits indicate the Type 4 CA that has been selected:

00 - CA #1	10 - CA #3
01 - CA #2	11 - CA #4

Byte 1, bit 7: This bit is 0.

Input X'79' (Utility)

This instruction causes the register specified by R to be loaded with information indicating (1) the state of the program level 5 C and Z condition latches, (2) the last program level to be active before a level 1 interrupt, and (3) the state of the IPL escape control.

Byte 0, bits 0-4: These bits are 0.

Byte 0, bit 5: 900 nanosecond cycle time.

Byte 0, bit 6: Program Level 5, C Condition—This bit indicates that the 'C condition' latch for program level 5 is on.

Byte 0, bit 7: Program Level 5, Z Condition—This bit indicates that the 'Z condition' latch for program level 5 is on.

Byte 1, bit 0: Program Level 2—This bit indicates that program level 2 was interrupted by level 1. (See note below.)

Byte 1, bit 1: Program Level 3—This bit indicates that program level 3 was interrupted by level 1. (See note below.)

Byte 1, bit 2: Program Level 4—This bit indicates that program level 4 was interrupted by level 1. (See note below.)

Byte 1, bit 3: Program Level 5—This bit indicates that program level 5 or the "wait" state was interrupted by level 1. (See note below.)

Byte 1, bit 4: 1 indicates that the 3705 has FET storage (3705-II); 0 indicates that the 3705 has bridge storage (3705-I).

Byte 1, bit 5: Remote 3704—0 indicates 3705; 1 indicates 3704. This bit is required for timing purposes in the test section of the ROS bootstrap program of a remote communications controller.

Byte 1, bit 6: Type 1 or 4 CA Installed—This bit indicates that a Type 1 or 4 CA is installed in the basic module of the controller. When the bit is off, a Type 2 or Type 3 CA is implied. However, this bit will be on only when the program being executed is running in level 1.

Byte 1, bit 7: IPL Escape Control—This bit is 0 as a result of a jumper wire installed by a Customer Engineer. By forcing a branch to storage location X'06FC', this jumper causes a bypass of the part of the bootstrap program that actually controls the initial program load. This is a diagnostic facility for read-only-storage maintenance.

Note to byte 1, bits 0-3: *One of these bits is 1 when an Input X'79' is executed in program level 1. The bit that is set indicates the program level that was operating when control was passed to program level 1. All other positions are set to 0. These bits are all 0 if Input X'79' is executed when not in program level 1.*

Input X'7A' (CUCR)

This instruction accesses the cycle utilization counter register (CUCR). The CUCR consists of a flag bit and 15 data bits. The flag bit, if set to 1, indicates that the CUCR is installed in the 3705. The 15 data bits comprise a 15-position binary counter that accumulates a count of the total number of utilized machine cycles. Utilized cycles are defined as cycles taken for instruction execution, cycle steal operations, and maintenance operations.

Notes:

1. The CUCR is a standard feature on 3705-II Models J–L only. The counter is available for 3705-II Models E–H, but only on an RPQ basis.
2. To determine if a 3705-II Model E–H contains the CUCR RPQ and clear the register of random data:
   a. Execute a Load Halfword instruction (storage = X'0000').

b. Execute an Output X'7A' instruction. The register specified must contain X'0000'.
c. Execute an Input X'7A' instruction to determine if bit 0.0 of the CUCR is set to 1. If bit 0.0 equals 1, the CUCR RPQ is installed. All other bit positions in the CUCR are zero.

3. Actual utilized cycle count is eight times the value in the CUCR because the counter advances by 1 each time eight cycles are utilized.

Byte 0, bit 0. (Flag): A 1 in this position indicates that the CUCR RPQ is installed (3705-II Model E–H only).

Byte 0, bit 1: A 1 in this position indicates a utilized cycle count of at least 16,384.

Byte 0, bit 2: A 1 in this position indicates a utilized cycle count of at least 8,192.

Byte 0, bit 3: A 1 in this poisiton indicates a utilized cycle count of at least 4,096.

Byte 0, bit 4: A 1 in this position indicates a utilized cycle count of at least 2,048.

Byte 0, bit 5: A 1 in this position indicates a utilized cycle count of at least 1,024.

Byte 0, bit 6: A 1 in this position indicates a utilized cycle count of at least 512.

Byte 0, bit 7: A 1 in this position indicates a utilized cycle count of at least 256.

Byte 1, bit 0: A 1 in this position indicates a utilized cycle count of at least 128.

Byte 1, bit 1: A 1 in this position indicates a utilized cycle count of at least 64.

Byte 1, bit 2: A 1 in this poisiton indicates a utilized cycle count of at least 32.

Byte 1, bit 3: A 1 in this position indicates a utilized cycle count of at least 16.

Byte 1, bit 4: A 1 in this position indicates a utilized cycle count of at least 8.

Byte 1, bit 5: A 1 in this position indicates a utilized cycle count of at least 4.

Byte 1, bit 6: A 1 in this position indicates a utilized cycle count of at least 2.

Byte 1, bit 7: A 1 in this position indicates a utilized cycle count of at least 1.

Input X'7B' (BSC CRC Register)

This instruction causes the old CRC character and the data character to be added to the CRC accumulation to be combined and loaded into the BSC CRC register. Then bytes 0 and 1 of the general register specified by R are loaded with the new BSC CRC accumulation character from the BSC CRC register. With Extended Addressing, byte X of the general register is set to 0. See *Cyclic Redundancy Check* in Chapter 5.

Input X'7C' (SDLC CRC Register)

This instruction combines the old CRC character with the data character to be added to the SDLC CRC and loads the new character into the CRC register. The new SDLC CRC is then stored in the specified general register.

Input X'7D' (CCU Check Register)

The bits of this instruction are set when the Central Control Unit detects an error condition. This instruction sets the bits in the general register specified by R to correspond to the CCU check register.

Byte 0, bit 0: Byte X Check—This bit indicates a byte X parity error (for Extended Addressing only).

Byte 0, bit 1: Byte 0 Check—This bit indicates a byte 0 parity error.

Byte 0, bit 2: Byte 1 Check—This bit indicates a byte 1 parity error.

Byte 0, bit 3: L1 Program Check—This bit indicates that a program check occurred while in level 1.

Byte 0, bit 4: SAR Check—This bit indicates a storage address register parity check. Byte 0, bit 0, 1, or 2 is also 1 to indicate which byte of the SAR caused the check.

Byte 0, bit 5: SDR Check—This bit indicates a storage data register parity check. Byte 0, bit 0, 1, or 2 is also 1 to indicate which byte of the SDR caused the check.

Byte 0, bit 6: Op Reg Check—This bit indicates an operation register parity check. Byte 0, bit 0, 1, or 2 is also 1 to indicate which byte of the Op Reg caused the check.

Byte 0, bit 7: Indata Bus Check—This bit indicates an indata bus check. Byte 0, bit 0, 1, or 2 is also 1 to indicate which byte of the indata bus caused the check.

Byte 1, bit 0: Cycle Counter Check—This bit indicates that the CCU cycle counter signaled an even number of time slots to the CCU. This check is one of three that set the Clock Check light on the control panel.

Byte 1, bits 1-4: These bits are 0.

Byte 1, bit 5: CCU Checks—This bit indicates the presence of a CCU check. The CCU check bit is a summary type bit that is set to 1 whenever any one or more of the CCU check bits of this input are on. When checking for a CCU check condition, this bit should be tested first.

Byte 1, bit 6: Type 2 Attachment Base Clock Check—This bit indicates a Type 2 Attachment Base clock check. This check indicates that the Type 2 Scanner clock has signaled an incorrect number of time slots. The check is one of three checks that set the Clock Check light on the control panel.

Byte 1, bit 7: CCU Clock Check—This bit indicates a Central Control Unit clock check. A CCU clock check indicates that the CCU clock has signaled an incorrect number of time slots. This check is one of three checks that set the Clock Check light on the control panel.

Input X'7E' (CCU Level 1 Interrupt Requests)
This instruction sets the bits in the register specified by R to indicate which level 1 interrupt request is set. Byte 1, bits 1-4 are set as the result of a program check in any level and cause an interrupt to level 1.

Byte 0, bits 0-7: These bits are 0.

Byte 1, bit 0: Address Compare Interrupt L1—This bit indicates a level 1 address compare interrupt.

Byte 1, bit 1: Address Exception L1—This bit indicates that an addressing exception has occurred.

Byte 1, bit 2: In/Out Check L1—This bit indicates that an input/output check has occurred.

Byte 1, bit 3: Protection Check L1—This bit indicates that a protection check has occurred.

Byte 1, bit 4: Invalid Op Check L1—This bit indicates that an invalid op-code check has occurred.

Byte 1, bit 5: This bit is 0.

Byte 1, bit 6: IPL L1—This bit indicates that program level 1 has requested an IPL.

Byte 1, bit 7: This bit is 0.

Input X'7F' (CCU Level 2, 3, or 4 Interrupt Requests)
This instruction is used to set bits in the register specified by R to indicate which level 2, 3, or 4 interrupt request is set.

Byte 0, bit 0: Diagnostic L2—This bit indicates a diagnostic level 2 interrupt request.

Byte 0, bits 1-5: These bits are 0.

Byte 0, bit 6: Panel Interrupt Request L3—This bit indicates an interrupt request from the Interrupt push button on the control panel.

Byte 0, bit 7: PCI L4—This bit indicates a level 4 program-controlled interrupt (PCI L4) request.

Byte 1, bits 0-4: These bits are 0.

Byte 1, bit 5: Interval Timer L3—This bit indicates a level 3 interval timer interrupt request.

Byte 1, bit 6: PCI L3—This bit indicates a level 3 program-controlled interrupt (PCI L3) request.

Byte 1, bit 7: SVC L4—This bit indicates a level 4 supervisor call interrupt (SVC L4) request.

CCU Output Instructions

Output X'70' (Hardstop)
This instruction causes the 'hardstop' latch to be set. This causes the controller to come to a complete stop and requires an IPL to continue processing. Since this instruction performs a function, the bit settings of the register are ignored.

Output X'71' (Display Register 1)
This instruction transfers the contents of the register specified by R to display register 1. The Program Display light on the control panel is also turned on.

Output X'72' (Display Register 2)
This instruction transfers the contents of the register specified by R to display register 2. The Program Display light on the control panel is also turned on.

Output X'73' (Set Key)
This instruction is associated with the storage protect mechanism. Refer to *Storage Protect* in Chapter 5. It is normally used to set either a storage key or protect key with the contents of byte 1, bits 5-7 of the register specified by R.

Byte 1, bit 3 (key select) controls the selection of either a storage key or protect key. If byte 1, bit 4 (set key) of the register is on, the addressed key is set according to byte 1, bits 5-7. If byte 1, bit 4 is off, the addressed key is not set. In either case, the key addressed with the last Output X'73' executed can be accessed with a subsequent Input X'73'.

For the 3704 and Models A–H of the 3705:

Byte 0, bits 0-3: Key Address—If byte 1, bit 3 of this output is 1, these bits, along with byte 0, bits 4-6 are set to the storage block number to be referenced when setting a storage key. If byte 1, bit 3 is 0, these bits are ignored.

Byte 0, bits 4-6: Key Address—If byte 1, bit 3 of this output is 1, these bits along with byte 0, bits 0-3 form a storage block number. If byte 1, bit 3 is a 0, these bits are set to the protect key address of the desired user.

Byte 0, bit 7: This bit is unused.

Byte 1, bits 0-2: These bits are unused.

For 3705 Models J–L:

Byte 0, bits 0-2: Reserved

Byte 0, bits 3-7: Key Address—If byte 1, bit 3 of this output is 1, these bits, along with byte 1, bits 0-2 are set to the storage block number to be referenced when setting a storage key. If byte 1, bit 3 is 0, byte 0, bits 4-6 are set to the protect key address of the desired user; byte 0, bits 3 and 7, and byte 1, bits 0-2 are ignored.

Byte 1, bits 0-2: Key Address—If byte 1, bit 3 of this output is 1, these bits along with byte 0, bits 3-7 form a storage block number. If byte 1, bit 3 is a 0, these bits along with byte 0, bits 3 and 7 are ignored.

Byte 1, bit 3: Key Address Select—This bit is used to indicate which key this instruction will be used for. If this bit is 1, a storage key is set, and the storage block number should be in byte 0, bits 0-6 (byte 0, bits 3-7 and byte 1, bits 0-2 for 3705 Models J–L). If this bit is 0, a protect key is set, and the address of the user should be in byte 0, bits 4-6.

Byte 1, bit 4: Set Key—If this bit is set to 1, the key set in bits 5-7 is inserted for the addressed key. If this bit is 0, no keys are changed.

Byte 1, bits 5-7: Key—These bits contain the storage key or protect key as indicated by byte 1, bit 3 to be assigned to the storage block or user addressed by byte 0, bits 0-6 (byte 0, bits 3-7 and byte 1, bits 0-2 for 3705 Models J–L). If byte 1, bit 4 is zero, theses bits are ignored.

Output X'77' (Miscellaneous Control)
This instruction contains miscellaneous controls used to set or to reset various interrupt requests.

Byte 0, bit 0: Reset IPL L1—This bit is set to 1 to reset the level 1 IPL request and the CA not-initialized state (Output X'57', byte 0, bit 7).

Byte 0, bit 1: Reset CCU Checks—This bit is set to 1 to reset all CCU checks.

Byte 0, bit 2: Reset Panel Interrupt Request L3—This bit is set to 1 to reset the external interrupt request at program level 3.

Byte 0, bits 3-4: These bits are reserved for diagnostic use. A 0 is the inactive state of these bits. The active state is allowed only in the test mode.

Byte 0 bit 5: This bit is unused.

Byte 0, bit 6: Set Diagnostic L2—If this bit is set to 1 and the CCU is in test mode, the diagnostic interrupt request at program level 2 is set. This bit should not be 1 if the CCU is not in test mode because the level 2 interrupt may be taken and there will be no indication that it is a diagnostic level 2 interrupt request (byte 0, bit 0 of Input X'7F').

Byte 0, bit 7: Reset Diagnostic L2—This bit is set to 1 to reset the level 2 diagnostic interrupt request. It is ignored if the CCU is not in the test mode.

Byte 1, bit 0: This bit is unused.

Byte 1, bit 1: Reset Interval Timer L3—This bit is set to 1 to reset the program level 3 interval timer interrupt request.

Byte 1, bit 2: Reset PCI L3—This bit is set to 1 to reset the level 3 program-controlled interrupt request (PCI L3) set by Output X'7C'.

Byte 1, bit 3: This bit is unused.

Byte 1, bit 4: Reset Address Compare L1—This bit is set to 1 to reset the program level 1 address compare interrupt request.

Byte 1, bit 5: Reset Program Checks L1—This bit is set to 1 to reset all program check interrupt requests to program level 1.

Byte 1, bit 6: Reset PCI L4—This bit is set to 1 to reset the level 4 program-controlled interrupt request (PCI L4) set by Output X'7D'.

Byte 1, bit 7: Reset SVC L4–This bit is set to 1 to reset the level 4 supervisor call (SVC L4) request.

Output X'78' (Force CCU Checks–3705)
This instruction provides a means for testing the CCU check circuits under diagnostic control by forcing checks in the CCU data flow. This output instruction is ignored if the CCU is not in the test mode.

Programming Note
Although the action specified by this instruction is taken only once, the result may be 'permanent' until corrective action is taken to store data with the correct parity into the affected register or storage location.

Byte 0, bits 0-7: Complement Bits 0-7—A 1 in any of these positions causes the corresponding bit positions of each byte (byte X, 0, and 1) of the input to the ALU check detection circuits to be complemented.

Byte 1, bit 0: Complement Storage Parity—A 1 in this position causes incorrect parity in both byte 0 and byte 1 of the halfword accessed in storage on the next instruction cycle.

Byte 1, bit 1: Complement Z Bus Parity—A 1 in this position causes incorrect parity to be stored into a general register. A load or store instruction should then follow this output to place the data from the general register on the Z bus to exercise parity checking circuits.

Byte 1, bit 2: A-Register Check—A 1 in this position causes incorrect parity in the A-register.

Byte 1, bit 3: Indata Bus Check—A 1 in this position causes the Indata parity bits to be complemented. This results in a B-register parity check when an Input X'70', X'73'-X'75', or X'78'-X'7F' instruction is executed. Input instructions X'71' and X'72' do not give checks.

Byte 1, bits 4-7: These bits are unused.

Output '78' (Force CCU Checks–3704)
This instruction provides a means of testing the CCU check circuits under diagnostic control by forcing checks in the CCU. This output is ignored if the CCU is not in test mode.

Programming Note
Although the action specified by this instruction is taken only once, the result may be 'permanent' until corrective action is taken to store data with the correct parity into the affected register or storage location.

Byte 0, bits 0-4: These bits are unused.

Byte 0, bits 5-7: Instruction Cycle Select—A binary decode of these three bits determines the cycle in which the selected error will occur, as follows:

001 = Select next I1 cycle
010 = Select next I2 cycle
011 = Select next I3 cycle
100 = Select next I4 cycle
101 = Select next I5 cycle

Byte 1, bit 0: Complement Storage Parity—This bit causes improper parity to be stored in both main storage bytes addressed during the next selected cycle (selected by byte 0, bits 5-7 of this instruction). This can be used to exercise either SDR or Op Reg parity checks at a later time. For the expected results, the selected cycle must coincide with an actual storage write operation.

Byte 1, bit 1: Complement Z Bus Parity—This bit is used to store even parity into a local store register or an external register.

Byte 1, bit 2: A-Reg Check—This bit causes the A-reg parity bits to be complemented during the next selected cycle.

Byte 1, bit 3: B-Reg Parity Error—This bit causes the B-reg parity bits to be complemented during the next selected cycle.

Byte 1, bit 4: SAR Parity Error—This bit causes the SAR parity bits to be complemented during the next selected cycle.

Byte 1, bit 5: Op Reg Parity Error—This bit causes the Op reg parity bits to be complemented during the next selected cycle. The selected cycle must be I1.

Byte 1, bits 6-7: These bits are unused.

Output X'79' (Utility)
This instruction is used to set or reset various CCU latches.

Byte 0, bits 0-1: These bits are unused.

Byte 0, bit 2: Set IPL—This bit is set to 1 to initiate an IPL operation.

Byte 0, bit 3: Set FET Storage Diagnostic Mode—This bit sets the 'allow set memory diagnostic register' latch.

Byte 0, bit 4: Remote Power Off—Using this bit allows the remote communications controller (if equipped with the Remote Power Off feature) to be powered off by the control program. Power must be restored manually.

Byte 0, bit 5: Inhibit Prog Level 5, C & Z Replacement—If this bit is set to 0, the program level 5 C and Z condition latches are set according to byte 0, bits 6-7. If this bit is 1, no action is taken.

Byte 0, bit 6: Program Level 5, C Condition—If byte 0, bit 5 of this output is 1, the 'C condition' latch for program level 5 is set according to the state of this bit.

Byte 0, bit 7: Program Level 5, Z Condition—If byte 0, bit 5 of this output is 1, the 'Z condition' latch for program level 5 is set according to the state of this bit.

Byte 1, bit 0: Reset CCU Check Hard Stop Mode—This bit is set to 1 to reset a CCU check hard stop.

The 'check stop mode' latch is set during IPL phase 1. As long as the Diagnostic Control switch on the control panel is in the PROCESS or CLOCK STEP position, the controller operates as if the switch is in the CCU CHECK HARD STOP position. This state can be overridden by the bypass CCU check stop state.

Byte 1, bit 1: Reset Load Indicator—This bit is set to 1 to reset the Load light on the control panel and to reset the 'load' latch to indicate the completion of IPL. The 'load' latch is set and the Load light is turned on during IPL.

Byte 1, bit 2: Set Test Mode—This bit is set to 1 to set the CCU in the *test mode.* This bit turns on the Test light on the control panel and enables the following diagnostic functions to be performed:

(1) Force CCU checks—Output X'78'.
(2) Set/reset Diagnostic Level 2.
(3) Set/reset Bypass CCU Check Stop.
(4) Set/reset adapter level 1 interrupt request mask.

See the *CCU Diagnostic Facilities* section in Chapter 5. This bit should not be 1 if byte 1, bit 3 of this output is 1.

Byte 1, bit 3: Reset Test Mode—This bit is set to 1 to reset the test mode. The Test light on the control panel is turned off if the Mode Select and the Diagnostic Control switches are both in the PROCESS position. Any of the test functions allowed by the test mode are also reset. This bit should not be 1 if byte 1, bit 2 of this output is 1.

Byte 1, bit 4: Set Bypass CCU Check Stop Mode—This bit is set to 1 to bypass the CCU check stop. When this bit is set, the operation is the same as if the Diagnostic Control switch on the control panel were in the BYPASS CCU CHECK STOP position. This bit should not be 1 if byte 1, bit 5 of this output is 1. It is ignored if the CCU is not in the test mode.

Byte 1, bit 5: Reset Bypass CCU Check Stop Mode—This bit is set to 1 to reset the bypass CCU check stop. This bit should not be 1 if byte 1, bit 4 of this output is 1. It is ignored if the CCU is not in the test mode.

Byte 1, bit 6: Scope Sync Pulse 1—This bit is set to 1 to generate the scope sync pulse 1. This is an oscilloscope synchronization pulse of 100 ns for maintenance purposes.

Byte 1, bit 7: Scope Sync Pulse 2—This bit is set to 1 to generate the scope sync pulse 1. This is an oscilloscope synchronization pulse of 100 ns for maintenance purposes.

Output X'7A' (Reset the CUCR)
This instruction resets the bits of the cycle utilization counter register. When the Output X'7A' instruction is issued, all of the bits in the CUCR are set to 0. Since this instruction performs a function, the bit settings of the register are ignored.

Output X'7C' (Set PCI L3)
This instruction sets the program-controlled interrupt request for level 3. Since this instruction performs a function, the bit settings of the register are ignored.

Output X'7D' (Set PCI L4)
This instruction sets the program-controlled interrupt request for level 4. Since this instruction performs a function, the bit settings of the register are ignored.

Output X'7E' (Set Mask bits)
This instruction sets mask bits that prevent interrupts to a certain program level during processing. See *Masking Program Level Priorities* in Chapter 5.

Byte 0, bits 0-7: These bits are unused.

Byte 1, bit 0: This bit is unused.

Byte 1, bit 1: Adapter Requests L1—A 1 in this position sets a mask to prevent CA and Scanner interrupts to program level 1 (for diagnostic test mode only).

Byte 1, bit 2: Program Level 2—A 1 in this position sets a mask to prevent interrupts to program level 2.

Byte 1, bit 3: Program Level 3—A 1 in this position sets a mask to prevent interrupts to program level 3.

Byte 1, bit 4: Program Level 4—A 1 in this position sets a mask to prevent interrupts to program level 4.

Byte 1, bit 5: Program Level 5—A 1 in this position sets a mask to prevent instruction execution in program level 5.

Byte 1, bits 6-7: These bits are unused.

Output X'7F' (Reset Mask bits)
This instruction resets the mask bits for program level interrupts. See *Masking Program Level Priorities* in Chapter 5.

Byte 0, bits 0-7: These bits are unused.

Byte 1, bit 0: This bit is unused.

Byte 1, bit 1: Adapter Requests L1—A 1 in this position unmasks CA and scanner interrupts to level 1 (for diagnostic test modes only).

Byte 1, bit 2: Program Level 2—A 1 in this position unmasks interrupts to program level 2.

Byte 1, bit 3: Program Level 3—A 1 in this position unmasks interrupts to program level 3.

Byte 1, bit 4: Program Level 4—A 1 in this position unmasks interrupts to program level 4.

Byte 1, bit 5: Program Level 5—A 1 in this position unmasks program level 5 to allow instruction execution at that level.

Byte 1, bits 6-7: These bits are unused.

Appendix C. Input/Output Instruction Summary Charts

GENERAL REGISTERS
X'00'–X'1F'

INPUT X'00' thru X'1F' GENERAL REGISTERS			OUTPUT X'00' thru X'1F' GENERAL REGISTERS (Note)		
Gen Reg (R)	Reg/Function (E)		Gen Reg (R)	Reg/Function (E)	
BYTE X, BIT 4	BYTE X, BIT 4	with 20-bit EA only	BYTE X, BIT 4	BYTE X, BIT 4	with 20-bit EA only
BIT 5	BIT 5		BIT 5	BIT 5	
BIT 6	BIT 6	with 1B or 20-bit EA	BIT 6	BIT 6	with 1B or 20-bit EA
BIT 7	BIT 7		BIT 7	BIT 7	
BYTE 0, BIT 0	BYTE 0, BIT 0		BYTE 0, BIT 0	BYTE 0, BIT 0	
BIT 1	BIT 1		BIT 1	BIT 1	
BIT 2	BIT 2		BIT 2	BIT 2	
BIT 3	BIT 3		BIT 3	BIT 3	
BIT 4	BIT 4		BIT 4	BIT 4	
BIT 5	BIT 5		BIT 5	BIT 5	
BIT 6	BIT 6		BIT 6	BIT 6	
BIT 7	BIT 7		BIT 7	BIT 7	
BYTE 1, BIT 0	BYTE 1, BIT 0		BYTE 1, BIT 0	BYTE 1, BIT 0	
BIT 1	BIT 1		BIT 1	BIT 1	
BIT 2	BIT 2		BIT 2	BIT 2	
BIT 3	BIT 3		BIT 3	BIT 3	
BIT 4	BIT 4		BIT 4	BIT 4	
BIT 5	BIT 5		BIT 5	BIT 5	
BIT 6	BIT 6		BIT 6	BIT 6	
BIT 7	BIT 7		BIT 7	BIT 7	
EA = Extended Addressing			Note: If R field=0, data in addressed reg is not changed but parity is regenerated.		

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.

TYPE 1 SCANNER
X'40'-X'47'

	OUTPUT X'40' TYPE 1 SCANNER - SET MODE BIT OVERRIDE and OVERRIDE REMEMBER Gen Reg (R) / Reg/Functian (E) BYTE 0, BIT 0 * BIT 1 * BIT 2 * BIT 3 * BIT 4 * BIT 5 * BIT 6 * BIT 7 * BYTE 1, BIT 0 * BIT 1 * BIT 2 * BIT 3 * BIT 4 * BIT 5 * BIT 6 * BIT 7 *
INPUT X'41' TYPE 1 SCANNER-INTERFACE ADDRESS (Note) Gen Reg (R) / Reg/Function (E) BYTE 0, BIT 0 0 BIT 1 0 BIT 2 0 BIT 3 0 BIT 4 1 BIT 5 0 BIT 6 Interface Address BIT 3 BIT 7 BIT 4 BYTE 1, BIT 0 BIT 5 BIT 1 BIT 6 BIT 2 BIT 7 BIT 3 BIT 8 BIT 4 0 BIT 5 0 BIT 6 0 BIT 7 0 Note: Bytes 0 & 1, I=X'06F0' For Chor Serv	OUTPUT X'41' TYPE 1 SCANNER-START SCANNER and RESET L2 BIT SERVICE REQUEST Gen Reg (R) / Reg/Function (E) BYTE 0, BIT 0 * BIT 1 * BIT 2 * BIT 3 * BIT 4 * BIT 5 * BIT 6 * BIT 7 * BYTE 1, BIT 0 * BIT 1 * BIT 2 * BIT 3 * BIT 4 * BIT 5 * BIT 6 * BIT 7 *
INPUT X'42' TYPE 1 SCANNER-CNTRL A--LINE INTERFACE (Autocall Interface shown below) Gen Reg (R) / Reg/Function (E) BYTE 0, BIT 0 0 BIT 1 0 BIT 2 0 BIT 3 0 BIT 4 0 BIT 5 0 BIT 6 Mode Bit 1 BIT 7 Mode Bit 2 BYTE 1, BIT 0 1=LO;0=HI Bit Svc Priority BIT 1 Diagnostic Mode BIT 2 Data Terminal Ready (DTR) BIT 3 Synchronous Bit Clock BIT 4 External Clock BIT 5 Data Rate Selector BIT 6 OSC Select Bit 1 BIT 7 OSC Select Bit 2	OUTPUT X'42' TYPE 1 SCANNER-CNTRL A--LINE INTERFACE (Autocall Interface shown below) Gen Reg (R) / Reg/Function (E) BYTE 0, BIT 0 * BIT 1 * BIT 2 * BIT 3 * BIT 4 * BIT 5 * BIT 6 1=Set; 0=Rst Mode Bit 1 BIT 7 1=Set; 0=Rst Mode Bit 2 BYTE 1, BIT 0 1=LO;0=HI Bit Svc Priority BIT 1 1=Set; 0=Rst Diagnostic Mode BIT 2 1=Set; 0=Rst Data Terminal Ready (DTR) BIT 3 1=Set; 0=Rst Synchronous Bit Clock BIT 4 1=Set; 0=Rst External Clock BIT 5 1=Set; 0=Rst Data Rate Selector BIT 6 1=Set; 0=Rst OSC Select Bit 1 BIT 7 1=Set; 0=Rst OSC Select Bit 2
INPUT X'42' TYPE 1 SCANNER-CNTRL A--AUTOCALL INTERFACE (Line Interface shown above) Gen Reg (R) / Reg/Function (E) BYTE 0, BIT 0 0 BIT 1 0 BIT 2 0 BIT 3 0 BIT 4 0 BIT 5 0 BIT 6 Mode Bit 1 BIT 7 Mode Bit 2 BYTE 1, BIT 0 1=LO;0=HI Bit Svc Priority BIT 1 0 BIT 2 0 BIT 3 0 BIT 4 0 BIT 5 0 BIT 6 0 BIT 7 0	OUTPUT X'42' TYPE 1 SCANNER-CNTRL A--AUTOCALL INTERFACE (Line Interface shown above) Gen Reg (R) / Reg/Function (E) BYTE 0, BIT 0 * BIT 1 * BIT 2 * BIT 3 * BIT 4 * BIT 5 * BIT 6 1=Set; 0=Rst Mode Bit 1 BIT 7 1=Set; 0=Rst Mode Bit 2 BYTE 1, BIT 0 1=LO;0=HI Bit Svc Priority BIT 1 * BIT 2 * BIT 3 * BIT 4 * BIT 5 * BIT 6 * BIT 7 *

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 1 SCANNER
X'40'-X'47'

INPUT X'43'	TYPE 1 SCANNER-CNTRL B/C-LINE INTERFACE (Autacall Interface shown belaw)
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	Receive Data Bit Buffer
BIT 1	Feedback Check
BIT 2	Interface Check Summary (note)
BIT 3	Received Data Lead (1=SPACE)
BIT 4	Transmit Mode
BIT 5	New Sync
BIT 6	Request to Send (RTS)
BIT 7	Send Data Bit Buffer
BYTE 1, BIT 0	Not Cleor ta Send (CTS)
BIT 1	Ring Indicatar (RI)
BIT 2	Not Data Set Ready (DSR)
BIT 3	Received Line Signal Detectar
BIT 4	Telegraph Interface Echa Check
BIT 5	Diagnostic Mode
BIT 6	Bit Service
BIT 7	Bit Overrun/Underrun

Note: OR of Byte 0 Bit 1, Byte 1 Bits 2 & 7

OUTPUT X'43'	TYPE 1 SCANNER-CNTRL B-LINE INTERFACE (Autacall Interface shawn belaw)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	1=Transmit Mode; 0=Receive Mode
BIT 5	New Sync
BIT 6	Request ta Send (RTS)
BIT 7	Send Data (1=mark)

INPUT X'43'	TYPE 1 SCANNER-CNTRL B/C-AUTOCALL INTERFACE (Line Interface shawn above)
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	0
BIT 1	Feedback Check
BIT 2	Interface Check Summary (nate)
BIT 3	Digit Present (DPR)
BIT 4	Digit NBR 8
BIT 5	Digit NBR 4
BIT 6	Digit NBR 2
BIT 7	Digit NBR 1
BYTE 1, BIT 0	Not Abandon Call & Retry (ACR)
BIT 1	Present Next Digit (PND)
BIT 2	Nat Data Line Occupied (DLO)
BIT 3	Power Indicatar (PWI)
BIT 4	Call Request (CRQ)
BIT 5	Call Originating Status (COS)
BIT 6	Bit Service
BIT 7	Bit Overrun/Underrun

Note: OR of Byte 0 Bit 1, Byte 1 Bits 2 & 7

OUTPUT X'43'	TYPE 1 SCANNER-CNTRL B-AUTOCALL INTERFACE (Line Interface shown above)
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	Call Request (CRQ)
BIT 3	Digit Present (DPR)
BIT 4	Digit NBR 8
BIT 5	Digit NBR 4
BIT 6	Digit NBR 2
BIT 7	Digit NBR 1

INPUT X'44'	TYPE 1 SCANNER-STATUS
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	Mode Bit Override
BIT 1	0
BIT 2	Override Remember
BIT 3	Sconner Enabled
BIT 4	Char Svc Pending
BIT 5	0
BIT 6	0
BIT 7	0
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	LIB Pas1 Bit Clock Check
BIT 3	LIB Pos2 Bit Clock Check
BIT 4	LIB Pas3 Bit Clock Check
BIT 5	LIB Pos4 Bit Clock Check
BIT 6	LIB Select Check
BIT 7	CCU OUTBUS Check

OUTPUT X'44'	TYPE 1 SCANNER-GENERAL CONTROL
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	1=Set; 0=Rst Diagnostic Bit Svc
BIT 1	*
BIT 2	Reset Mode Bit Override
BIT 3	Reset Override Remember
BIT 4	Reset Chorocter Service Pending
BIT 5	Reset Type 1 Scan LI Checks
BIT 6	Reset Feedback Check
BIT 7	Reset Bit Overrun/Underrun

OUTPUT X'45'	TYPE 1 SCANNER-SCANNER CONTROL
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	*
BIT 1	Set Scanner Enabled
BIT 2	Reset Sconner Enabled
BIT 3	*
BIT 4	1=Set; 0=Rst Disable LIB Pos 1
BIT 5	1=Set; 0=Rst Disable LIB Pos 2
BIT 6	1=Set; 0=Rst Disable LIB Pos 3
BIT 7	1=Set; 0=Rst Disable LIB Pos 4
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 1 SCANNER
X'40'-X'47'

OUTPUT X'46' — TYPE 1 SCANNER SET CHAR SVC PENDING, START SCANNER, RST L2 BIT REQUEST

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

OUTPUT X'47' — TYPE 1 SCANNER-FORCE BIT SERVICE L2 REQUEST

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	Interface Address BIT 3
BIT 7	BIT 4
BYTE 1, BIT 0	BIT 5
BIT 1	BIT 6
BIT 2	BIT 7
BIT 3	BIT B
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

TYPE 2 SCANNER
X'40'-X'47'

INPUT X'40' — TYPE 2 SCANNER - INTERFACE ADDRESS

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	1
BIT 5	0
BIT 6	Interface Address BIT 0
BIT 7	BIT 1
BYTE 1, BIT 0	BIT 2
BIT 1	BIT 3
BIT 2	BIT 4
BIT 3	BIT 5
BIT 4	BIT 6
BIT 5	BIT 7
BIT 6	BIT B
BIT 7	0

OUTPUT X'40' — TYPE 2 SCANNER - INTERFACE ADDRESS

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	Interface Address BIT 0
BIT 7	BIT 1
BYTE 1, BIT 0	BIT 2
BIT 1	BIT 3
BIT 2	BIT 4
BIT 3	BIT 5
BIT 4	BIT 6
BIT 5	BIT 7
BIT 6	BIT B
BIT 7	*

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 2 SCANNER
X'40'-X'47'

OUTPUT X'41' TYPE 2 SCANNER - ADDRESS SUBSTITUTION CONTROL

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	SUB CTRL REG BIT 1
BIT 3	SUB CTRL REG BIT 2
BIT 4	SUB CTRL REG BIT 3
BIT 5	SUB CTRL REG BIT 4
BIT 6	*
BIT 7	*

OUTPUT X'42' TYPE 2 SCANNER - UPPER SCAN LIMIT CONTROL

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	Scan Limit Select BIT 0 (note)
BIT 7	Scan Limit Select BIT 1 (note)

Note: 00=96; 01=8; 10=48; 11=16

INPUT X'43' TYPE 2 SCANNER - CHECK REGISTER

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	LIB Pos 1 Bit Clock Check
BIT 1	LIB Pos 2 Bit Clock Check
BIT 2	LIB Pos 3 Bit Clock Check
BIT 3	LIB Pos 4 Bit Clock Check
BIT 4	LIB Pos 5 Bit Clock Check (Note)
BIT 5	LIB Pos 6 Bit Clock Check (Note)
BIT 6	LIB Select Check
BIT 7	ICW IN Reg Check
BYTE 1, BIT 0	ICW Work Reg Check
BIT 1	Priority Reg Avail Check
BIT 2	CCU OUTBUS Check
BIT 3	LINEADBUS Check
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0

Note: Not applicable for Type 2 Scanner-1

OUTPUT X'43' TYPE 2 SCANNER - CONTROL

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Set Function
BIT 1	Reset Function
BIT 2	ICW Bit 3B (Display Request)
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	Disable LIB Pos 1
BYTE 1, BIT 0	Disable LIB Pos 2
BIT 1	Disable LIB Pos 3
BIT 2	Disable LIB Pos 4
BIT 3	Disable LIB Pos 5 (Note)
BIT 4	Disable LIB Pos 6 (Note)
BIT 5	Type 2 Scan L1 Request
BIT 6	Disable Interrupt Requests
BIT 7	*

Note: Not applicable for Type 2 Scanner-1

INPUT X'44' TYPE 2 SCANNER-ICW Input Reg Bits 0-15 (Note)

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	ICW BIT 0	Stop Bit Check/Receive Break
BIT 1	BIT 1	Service Request
BIT 2	BIT 2	Char Over/Underrun
BIT 3	BIT 3	Modem Check
BIT 4	BIT 4	Rcvd Line Sig Det (PWI)
BIT 5	BIT 5	*
BIT 6	BIT 6	Program Flag
BIT 7	BIT 7	Pod Flag
BYTE 1, BIT 0	BIT 8	PDF BIT 0
BIT 1	BIT 9	BIT 1
BIT 2	BIT 10	BIT 2
BIT 3	BIT 11	BIT 3
BIT 4	BIT 12	BIT 4
BIT 5	BIT 13	BIT 5
BIT 6	BIT 14	BIT 6
BIT 7	BIT 15	BIT 7

Note: Autocall Interface Lines are shown in parenthesis.

OUTPUT X'44' TYPE 2 SCANNER-ICW Bits 0-15

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	RST ICW BIT 0	Stop Bit Check/Receive Break
BIT 1	RST ICW BIT 1	Service Request
BIT 2	RST ICW BIT 2	Char Over/Underrun
BIT 3	RST ICW BIT 3	Modem Check
BIT 4	*	
BIT 5	ICW BIT 5	(must be 0)
BIT 6	BIT 6	Program Flag
BIT 7	BIT 7	Pod Flag
BYTE 1, BIT 0	BIT 8	PDF BIT 0
BIT 1	BIT 9	BIT 1
BIT 2	BIT 10	BIT 2
BIT 3	BIT 11	BIT 3
BIT 4	BIT 12	BIT 4
BIT 5	BIT 13	BIT 5
BIT 6	BIT 14	BIT 6
BIT 7	BIT 15	BIT 7

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 2 SCANNER
X'40'-'47'

INPUT X'44' — TYPE 2 SCANNER - ICW Input Reg Bits 0-15
SYNCHRONOUS DATA LINK CONTROL (SDLC)

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	ICW BIT 0	Abort
BIT 1	BIT 1	Service Request Interlock
BIT 2	BIT 2	Chorocter Overrun/Underrun - Flag Not on Boundory
BIT 3	BIT 3	Modem Check
BIT 4	BIT 4	Receive Line Signal Det.
BIT 5	BIT 5	Flag Detection/Disable Zero Insert Remembronce
BIT 6	BIT 6	Program Flag
BIT 7	BIT 7	Disable-Zero Insert Control
BYTE 1, BIT 0	BIT 8	PDF BIT 0
BIT 1	BIT 9	BIT 1
BIT 2	BIT 10	BIT 2
BIT 3	BIT 11	BIT 3
BIT 4	BIT 12	BIT 4
BIT 5	BIT 13	BIT 5
BIT 6	BIT 14	BIT 6
BIT 7	BIT 15	BIT 7

OUTPUT X'44' — TYPE 2 SCANNER - ICW Bits 0-15
SYNCHRONOUS DATA LINK CONTROL (SDLC)

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	RST ICW BIT 0	Abort
BIT 1	RST ICW BIT 1	Service Request Inerlock
BIT 2	RST ICW BIT 2	Chorocter Overrun/Underrun - Flag Not on Boundory
BIT 3	RST ICW BIT 3	Modem Check
BIT 4	*	
BIT 5	RST ICW BIT 5	Flag Detection/Disable Zero-Insert Remembronce
BIT 6	ICW BIT 6	Program Flag
BIT 7	BIT 7	Disable Zero-Insert Control
BYTE 1, BIT 0	BIT 8	PDF BIT 0
BIT 1	BIT 9	BIT 1
BIT 2	BIT 10	BIT 2
BIT 3	BIT 11	BIT 3
BIT 4	BIT 12	BIT 4
BIT 5	BIT 13	BIT 5
BIT 6	BIT 14	BIT 6
BIT 7	BIT 15	BIT 7

INPUT X'45' — TYPE 2 SCANNER-ICW Input Reg Bits 16-31

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	ICW BIT 16	LCD BIT 0
BIT 1	BIT 17	BIT 1
BIT 2	BIT 18	BIT 2
BIT 3	BIT 19	BIT 3
BIT 4	BIT 20	PCF BIT 0
BIT 5	BIT 21	BIT 1
BIT 6	BIT 22	BIT 2
BIT 7	BIT 23	BIT 3
BYTE 1, BIT 0	BIT 24	SDF BIT 0
BIT 1	BIT 25	BIT 1
BIT 2	BIT 26	BIT 2
BIT 3	BIT 27	BIT 3
BIT 4	BIT 28	BIT 4
BIT 5	BIT 29	BIT 5
BIT 6	BIT 30	BIT 6
BIT 7	BIT 31	BIT 7

OUTPUT X'45' — TYPE 2 SCANNER-ICW Bits 16-23

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	*	
BIT 1	*	
BIT 2	*	
BIT 3	*	
BIT 4	*	
BIT 5	*	
BIT 6	*	
BIT 7	*	
BYTE 1, BIT 0	ICW BIT 16	LCD BIT 0
BIT 1	BIT 17	BIT 1
BIT 2	BIT 18	BIT 2
BIT 3	BIT 19	BIT 3
BIT 4	BIT 20	PCF BIT 0
BIT 5	BIT 21	BIT 1
BIT 6	BIT 22	BIT 2
BIT 7	BIT 23	BIT 3

INPUT X'46' — TYPE 2 SCANNER DISPLAY REG
(Note)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Clear to Send (ACR)
BIT 1	Ring Indicator (PND)
BIT 2	Data Set Ready (DLO)
BIT 3	Rcv Line Sig Det (PWI)
BIT 4	Receive Data Bit Buffer
BIT 5	Diagnostic Wrap Mode (COS)
BIT 6	Bit Service Request
BIT 7	0
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0

Note: Autocall Interface Lines are shown in parenthesis.

OUTPUT X'46' — TYPE 2 SCANNER-ICW Bits 24-33 & 44

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	ICW BIT 44-NRZI Control (SDLC)	
BIT 1	*	
BIT 2	*	
BIT 3	*	
BIT 4	*	
BIT 5	*	
BIT 6	ICW BIT 24	SDF BIT 0
BIT 7	BIT 25	BIT 1
BYTE 1, BIT 0	BIT 26	BIT 2
BIT 1	BIT 27	BIT 3
BIT 2	BIT 28	BIT 4
BIT 3	BIT 29	BIT 5
BIT 4	BIT 30	BIT 6
BIT 5	BIT 31	BIT 7
BIT 6	BIT 32	BIT 8
BIT 7	BIT 33	BIT 9

INPUT X'47' — TYPE 2 SCANNER-ICW Input Reg Bits 32-45

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	ICW BIT 32	SDF BIT 8
BIT 1	BIT 33	SDF BIT 9
BIT 2	BIT 34	Ones Counter 0
BIT 3	BIT 35	Ones Counter 1 (SDLC)
BIT 4	BIT 36	Ones Counter 2
BIT 5	BIT 37	0-Unused
BIT 6	ICW BIT 38	Display Request
BIT 7	BIT 39	0-Unused
BYTE 1, BIT 0	BIT 40	0-Unused
BIT 1	BIT 41	L2 Interrupt Pending
BIT 2	BIT 42	Priority Bit 1
BIT 3	BIT 43	Priority Bit 2
BIT 4	BIT 44	NRZI Mode (SDLC)
BIT 5	BIT 45	0-Unused
BIT 6	0	
BIT 7	0	

OUTPUT X'47' — TYPE 2 SCANNER-ICW Bits 34-43

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	*	
BIT 1	*	
BIT 2	*	
BIT 3	*	
BIT 4	*	
BIT 5	*	
BIT 6	ICW BIT 34	
BIT 7	BIT 35	
BYTE 1, BIT 0	BIT 36	
BIT 1	BIT 37	
BIT 2	*	
BIT 3	ICW BIT 39	
BIT 4	BIT 40	
BIT 5	BIT 41	Set L2 Interrupt Pending
BIT 6	BIT 42	Priority Bit 1
BIT 7	BIT 43	Priority Bit 2

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 3/3HS SCANNER
X'40'-X'4F'

INPUT X'40' TYPE 3/TYPE 3HS SCANNER - INTERFACE ADDRESS

Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	1
BIT 5	0
BIT 6	Interfoce Address BIT 0
BIT 7	BIT 1
BYTE 1, BIT 0	BIT 2
BIT 1	BIT 3
BIT 2	BIT 4
BIT 3	BIT 5
BIT 4	BIT 6
BIT 5	BIT 7
BIT 6	BIT 8
BIT 7	0

OUTPUT X"40' TYPE 3/TYPE 3HS SCANNER - INTERFACE ADDRESS

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	Interfoce Address BIT 0
BIT 7	BIT 1
BYTE 1, BIT 0	BIT 2
BIT 1	BIT 3
BIT 2	BIT 4
BIT 3	BIT 5
BIT 4	BIT 6
BIT 5	BIT 7
BIT 6	BIT 8
BIT 7	*

INPUT X'41' TYPE 3/TYPE 3HS SCANNER - HIGH SPEED SELECT

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	High Speed Select Reg 0	Not applicable to the Type 3HS Scanner
1	1	
2	2	
3	3	
4	4	
5	5	
6	6	
7	7	
BYTE 1, BIT 0	Cy Stl PDF Array Ptr Bit 16 (ICW 17.0)	Type 3HS Scanner Only
1	PDF Array Ptr Bit 16 (ICW 17.1)	
2	0	
3	0	
4	0	
5	0	
6	0	
7	0	

OUTPUT X'41' TYPE 3/TYPE 3HS SCANNER - SCAN SUBSTITUTION CONTROL

Gen Reg (R)	Reg/Functian (E)	
BYTE 0, BIT 0	High Speed Select Reg 0	Not applicable to the Type 3HS Scanner
BIT 1	1	
BIT 2	2	
BIT 3	3	
BIT 4	4	
BIT 5	5	
BIT 6	6	
BIT 7	7	
BYTE 1, BIT 0	*	
BIT 1	*	
BIT 2	SUB CTRL REG BIT 1	These bits must be set to zero when using a Type 3HS Communication Scanner
BIT 3	SUB CTRL REG BIT 2	
BIT 4	SUB CTRL REG BIT 3	
BIT 5	SUB CTRL REG BIT 4	
BIT 6	*	
BIT 7	*	

INPUT X'42' TYPE 3/TYPE 3HS SCANNER - DBAR/CHECK REGISTER 0

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	Work Reg Ck 2 Por. Err KW Byte	3/13
1	3	4/12
2	4	5/11
3	5	6/8
4	6	7/9
5	7	15/16
6	PDF Array Pority Error	
7	0	
BYTE 1, BIT 0	DBAR 2^5	
1	2^4	
2	2^3	
3	2^2	
4	2^1	
5	2^0	
6	Scon Limit Select BIT 0 (note)	
7	1 (note)	

Note: 00=96; 01=8; 10=48; 11=16
(Bits 1.6 and 1.7 are not applicable to a Type 3HS Scanner.)

OUTPUT X"42' TYPE 3/TYPE 3HS SCANNER - DBAR/SCAN LIMIT CONTROL

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0
BYTE 1, BIT 0	DBAR 2^5
BIT 1	2^4
BIT 2	2^3
BIT 3	2^2
BIT 4	2^1
BIT 5	2^0
BIT 6	Scon Limit Select BIT 0 (note)
BIT 7	Scon Limit Select BIT 1 (note)

Note: 00=96; 01=8; 10=48; 11=16
(Bits 1.6 and 1.7 are not applicable to e Type 3HS Scanner.)

INPUT X'43' TYPE 3/TYPE 3HS SCANNER - CHECK REGISTER 1

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	LIB Pos 1 Bit Clock Check
BIT 1	LIB Pos 2 Bit Clock Check
BIT 2	LIB Pos 3 Bit Clock Check
BIT 3	LIB Pos 4 Bit Clock Check
BIT 4	0
BIT 5	0
BIT 6	LIB Select Check
BIT 7	ICW IN Bus Check
BYTE 1, BIT 0	ICW Work Reg Check 1 Par. Err ICW Byte 2/10
BIT 1	Priority Reg Avail Check
BIT 2	CCU OUTBUS Check
BIT 3	LINEADBUS Check
BIT 4	Bad Cycle Steal Data Inbound
BIT 5	CSAR Check
BIT 6	Address Exception
BIT 7	ICW Work Reg Check 0 Por. Err ICW Byte 0/14

OUTPUT X'43' TYPE 3/TYPE 3HS SCANNER - CONTROL

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Set Function
BIT 1	Reset Function
BIT 2	ICW Bit 4.6 (Display Request)
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	ICW Diognostic Mode
BIT 7	Disable/Enoble LIB Pos 1
BYTE 1, BIT 0	Disoble/Enoble LIB Pos 2
BIT 1	Disable/Enoble LIB Pos 3
BIT 2	Disoble/Enoble LIB Pos 4
BIT 3	*
BIT 4	*
BIT 5	Type 3 Scan L1 Request
BIT 6	Disable Interrupt Requests
BIT 7	*

With Extended Addressing, Byte X is set to zero for input instructians, ignared for output instructions.
* = Bit positions unused – moy be 1 or 0.

TYPE 3/TYPE 3HS SCANNER
X'40'-X'4F'

INPUT X'44' — TYPE 3/TYPE 3HS SCANNER-ICW Reg Bytes 0 and 1

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 0.0 Abart Detect (SDLC)
BIT 1	BIT 0.1 Service Request
BIT 2	BIT 0.2 Character Overrun/Underrun
BIT 3	BIT 0.3 Modem Check
BIT 4	BIT 0.4 Not Level 2 Bid
BIT 5	BIT 0.5 End of Messoge
BIT 6	BIT 0.6 Program Flog
BIT 7	BIT 0.7 Line Trace Cantral
BYTE 1, BIT 0	BIT 1.0 PDF BIT 0
BIT 1	BIT 1.1 BIT 1
BIT 2	BIT 1.2 BIT 2
BIT 3	BIT 1.3 BIT 3
BIT 4	BIT 1.4 BIT 4
BIT 5	BIT 1.5 BIT 5
BIT 6	BIT 1.6 BIT 6
BIT 7	BIT 1.7 BIT 7

OUTPUT X'44' — TYPE 3/TYPE 3HS SCANNER-ICW Reg Bytes 0 and 1

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 0.0 Reset Abart Detect (SDLC)
BIT 1	BIT 0.1 Reset Norm Service Request Int.
BIT 2	BIT 0.2 Reset Char Overrun/Underrun
BIT 3	BIT 0.3 Reset Modem Check
BIT 4	BIT 0.4 Set Not L2 Bid
BIT 5	BIT 0.5 Reset End of Messoge
BIT 6	BIT 0.6 Set/reset Program Flag
BIT 7	BIT 0.7 Set/reset Line Trace Control
BYTE 1, BIT 0	BIT 1.0 PDF BIT 0
BIT 1	BIT 1.1 BIT 1
BIT 2	BIT 1.2 BIT 2
BIT 3	BIT 1.3 BIT 3
BIT 4	BIT 1.4 BIT 4
BIT 5	BIT 1.5 BIT 5
BIT 6	BIT 1.6 BIT 6
BIT 7	BIT 1.7 BIT 7

INPUT X'45' — TYPE 3/TYPE 3HS SCANNER-ICW Reg Bytes 2 and 3

Gen Reg (R)	
BYTE 0, BIT 0	ICW BIT 2.0 LCD BIT 0
BIT 1	BIT 2.1 BIT 1
BIT 2	BIT 2.2 BIT 2
BIT 3	BIT 2.3 BIT 3
BIT 4	BIT 2.4 PCF BIT 0
BIT 5	BIT 2.5 BIT 1
BIT 6	BIT 2.6 BIT 2
BIT 7	BIT 2.7 BIT 3
BYTE 1, BIT 0	BIT 3.0 SDF BIT 0
BIT 1	BIT 3.1 BIT 1
BIT 2	BIT 3.2 BIT 2
BIT 3	BIT 3.3 BIT 3
BIT 4	BIT 3.4 BIT 4
BIT 5	BIT 3.5 BIT 5
BIT 6	BIT 3.6 BIT 6
BIT 7	BIT 3.7 BIT 7

OUTPUT X'45' — TYPE 3/TYPE 3HS SCANNER-ICW Reg Bytes 2 and 16

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	1-Set/0-Do not set byte 16
BIT 1	ICW BIT 16.1 Dota Terminal Reody
BIT 2	BIT 16.2 OLTT Diognastic
BIT 3	BIT 16.3 (reserved)
BIT 4	BIT 16.4 EPCF BIT 0
BIT 5	BIT 16.5 BIT 1
BIT 6	BIT 16.6 BIT 2
BIT 7	BIT 16.7 BIT 3
BYTE 1, BIT 0	ICW BIT 2.0 LCD BIT 0
BIT 1	BIT 2.1 BIT 1
BIT 2	BIT 2.2 BIT 2
BIT 3	BIT 2.3 BIT 3
BIT 4	BIT 2.4 PCF BIT 0
BIT 5	BIT 2.5 BIT 1
BIT 6	BIT 2.6 BIT 2
BIT 7	BIT 2.7 BIT 3

INPUT X'46' — TYPE 3/TYPE 3HS SCANNER-DISPLAY REG (Note)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Clear to Send (ACR)/DO-1/DI-1
BIT 1	Ring Indicotor (PND)/DO-2/DI-2
BIT 2	Dato Set Ready (DLO)/DO-3/DI-3
BIT 3	Receive Line Signol Detect (PWI)/DO-4/DI-4
BIT 4	Receive Data Bit Buffer/DO-5/DI-5
BIT 5	Diagnastic Wrap Mode (COS)/DO-6/DI-6
BIT 6	Bit Service Request/DO-7/DI-7
BIT 7	ICW Diag Mode
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0

Autocoll Interface Lines are shawn in parentheses; DO-x refers to Scanner Data Out line to LIB; this bit meoning effective when ICW bit 5.5 is on; DI-x refers ta Sconner Data In line to LIB; this bit meaning effective when LCD state is X'7' ar X'F'

OUTPUT X'46' — TYPE 3/TYPE 3HS SCANNER-ICW Byte 3 and Bits 4.0, 4.1

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 3.0 (Set Mode)
BIT 1	BIT 3.1 (Set Mode)
BIT 2	BIT 3.2 (Set Mode)
BIT 3	BIT 3.6 (Set Mode)
BIT 4	*
BIT 5	*
BIT 6	ICW BIT 3.0 SDF BIT 0
BIT 7	BIT 3.1 BIT 1
BYTE 1, BIT 0	BIT 3.2 BIT 2
BIT 1	BIT 3.3 BIT 3
BIT 2	BIT 3.4 BIT 4
BIT 3	BIT 3.5 BIT 5
BIT 4	BIT 3.6 BIT 6
BIT 5	BIT 3.7 BIT 7
BIT 6	BIT 3.8 BIT 8
BIT 7	BIT 3.9 BIT 9

INPUT X'47' — TYPE 3/TYPE 3HS SCANNER-ICW Bytes 4 and 5

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 4.0 SDF BIT 8
BIT 1	BIT 4.1 BIT 9
BIT 2	BIT 4.2 Ones Counter Bit 4
BIT 3	BIT 4.3 Ones Counter Bit 2
BIT 4	BIT 4.4 Ones Counter Bit 1
BIT 5	BIT 4.5 Lost Line Stote/Timeout CH
BIT 6	BIT 4.6 Display Request
BIT 7	BIT 4.7 Ones Counter Bit 16
BYTE 1, BIT 0	BIT 5.0 Ones Counter Bit 8
BIT 1	BIT 5.1 L2 Interrupt Pending
BIT 2	BIT 5.2 Priority Bit 1
BIT 3	BIT 5.3 Priority Bit 2
BIT 4	BIT 5.4 NRZI Mode/Transp. Text
BIT 5	BIT 5.5 Diagnostic Bit 0
BIT 6	BIT 5.6 Diognostic Bit 1
BIT 7	BIT 5.7 External Clock

OUTPUT X'47' — TYPE 3/TYPE 3HS SCANNER-ICW Bytes 4 and 5

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	ICW BIT 4.2 Ones Counter/Int. Timer Bit 4
BIT 7	BIT 4.3 Ones Counter/Int. Timer Bit 2
BYTE 1, BIT 0	BIT 4.4 Ones Counter/Int. Timer Bit 1
BIT 1	BIT 4.5 Last Line State/Timeout Ctl
BIT 2	*
BIT 3	ICW BIT 4.7 Ones Counter/Int. Timer Bit 16
BIT 4	BIT 5.0 Ones Counter/Int. Timer Bit 8
BIT 5	BIT 5.1 L2 Int. Pending
BIT 6	ICW BIT 5.2 Priority Sel Bit 1
BIT 7	BIT 5.3 Priority Sel Bit 2

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 3/TYPE 3HS SCANNER
X'40'-X'4F'

INPUT X'48' — TYPE 3/TYPE 3HS SCANNER-ICW Bytes 6 and 7

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 6.0 Cycle Steal Addr Bit X.4
BIT 1	BIT 6.1 Cycle Steal Addr Bit X.5
BIT 2	ICW BIT 6.2 Cycle Steal Addr Bit X.6
BIT 3	BIT 6.3 Cycle Steal Addr Bit X.7
BIT 4	BIT 6.4 ETB/ETX/ENQ in data
BIT 5	BIT 6.5 Cycle Steal Valid
BIT 6	BIT 6.6 Data Chain Flag
BIT 7	BIT 6.7 Message Chain Flag
BYTE 1, BIT 0	BIT 7.0 Cy Stl Byte Ct Bit 12B
BIT 1	BIT 7.1 Bit 64
BIT 2	BIT 7.2 Bit 32
BIT 3	BIT 7.3 Bit 16
BIT 4	BIT 7.4 Bit B
BIT 5	BIT 7.5 Bit 4
BIT 6	BIT 7.6 Bit 2
BIT 7	BIT 7.7 Bit 1

OUTPUT X'48' — TYPE 3/TYPE 3HS SCANNER-ICW Bytes 6 and 7

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 6.0 Cycle Steal Addr Bit X.4
BIT 1	BIT 6.1 Cycle Steal Addr Bit X.5
BIT 2	ICW BIT 6.2 Cycle Steal Addr Bit X.6
BIT 3	BIT 6.3 Cycle Steal Addr Bit X.7
BIT 4	(reserved)
BIT 5	ICW BIT 6.5 Cycle Steal Valid
BIT 6	BIT 6.6 Data Chain Flag
BIT 7	BIT 6.7 Message Chain Flag
BYTE 1, BIT 0	BIT 7.0 Cy Stl Byte Ct Bit 12B
BIT 1	BIT 7.1 Bit 64
BIT 2	BIT 7.2 Bit 32
BIT 3	BIT 7.3 Bit 16
BIT 4	BIT 7.4 Bit B
BIT 5	BIT 7.5 Bit 4
BIT 6	BIT 7.6 Bit 2
BIT 7	BIT 7.7 Bit 1

INPUT X'49' — TYPE 3/TYPE 3HS SCANNER-ICW Bytes 8 and 9

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 8.0 Cycle Steal Address Byte 0
BIT 1	BIT 8.1
BIT 2	BIT 8.2
BIT 3	BIT 8.3
BIT 4	BIT 8.4
BIT 5	BIT 8.5
BIT 6	BIT 8.6
BIT 7	BIT 8.7
BYTE 1, BIT 0	BIT 9.0 Cycle Steal Address Byte 1
BIT 1	BIT 9.1
BIT 2	BIT 9.2
BIT 3	BIT 9.3
BIT 4	BIT 9.4
BIT 5	BIT 9.5
BIT 6	BIT 9.6
BIT 7	BIT 9.7

OUTPUT X'49' — TYPE 3/TYPE 3HS SCANNER-ICW Bytes 8 and 9

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 8.0 Cycle Steal Address Byte 0
BIT 1	BIT 8.1
BIT 2	BIT 8.2
BIT 3	BIT 8.3
BIT 4	BIT 8.4
BIT 5	BIT 8.5
BIT 6	BIT 8.6
BIT 7	BIT 8.7
BYTE 1, BIT 0	BIT 9.0 Cycle Steal Address Byte 1
BIT 1	BIT 9.1
BIT 2	BIT 9.2
BIT 3	BIT 9.3
BIT 4	BIT 9.4
BIT 5	BIT 9.5
BIT 6	BIT 9.6
BIT 7	BIT 9.7

INPUT X'4A' — TYPE 3/TYPE 3HS SCANNER-ICW Bytes 10 and 11

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 10.0 BCC BIT 0 BCC-1
BIT 1	BIT 10.1 BIT 1
BIT 2	BIT 10.2 BIT 2
BIT 3	BIT 10.3 BIT 3
BIT 4	BIT 10.4 BIT 4
BIT 5	BIT 10.5 BIT 5
BIT 6	BIT 10.6 BIT 6
BIT 7	BIT 10.7 BIT 7
BYTE 1, BIT 0	BIT 11.0 BIT B BCC-2
BIT 1	BIT 11.1 BIT 9
BIT 2	BIT 11.2 BIT 10
BIT 3	BIT 11.3 BIT 11
BIT 4	BIT 11.4 BIT 12
BIT 5	BIT 11.5 BIT 13
BIT 6	BIT 11.6 BIT 14
BIT 7	BIT 11.7 BIT 15

OUTPUT X'4A' — TYPE 3/TYPE 3HS SCANNER-ICW Bytes 10 and 11

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 10.0 BCC BIT 0 BCC-1
BIT 1	BIT 10.1 BIT 1
BIT 2	BIT 10.2 BIT 2
BIT 3	BIT 10.3 BIT 3
BIT 4	BIT 10.4 BIT 4
BIT 5	BIT 10.5 BIT 5
BIT 6	BIT 10.6 BIT 6
BIT 7	BIT 10.7 BIT 7
BYTE 1, BIT 0	BIT 11.0 BIT B BCC-2
BIT 1	BIT 11.1 BIT 9
BIT 2	BIT 11.2 BIT 10
BIT 3	BIT 11.3 BIT 11
BIT 4	BIT 11.4 BIT 12
BIT 5	BIT 11.5 BIT 13
BIT 6	BIT 11.6 BIT 14
BIT 7	BIT 11.7 BIT 15

INPUT X'4B' — TYPE 3/TYPE 3HS SCANNER-ICW Bytes 16

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	ICW BIT 16.0 New Sync
BIT 1	BIT 16.1 Data Terminal Ready
BIT 2	BIT 16.2 OLTT Diagnostic
BIT 3	BIT 16.3 (reserved)
BIT 4	BIT 16.4 Extended PCF Bit 0
BIT 5	BIT 16.5 Bit 1
BIT 6	BIT 16.6 Bit 2
BIT 7	BIT 16.7 Bit 3

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

INPUT X'4C' **TYPE 3/TYPE 3HS SCANNER-PDF Array Address**

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	PDF Array Bit 0.5
BIT 6	Bit 0.6
BIT 7	Bit 0.7
BYTE 1, BIT 0	Bit 1.0
BIT 1	Bit 1.1
BIT 2	Bit 1.2
BIT 3	Bit 1.3
BIT 4	Bit 1.4
BIT 5	Bit 1.5
BIT 6	Bit 1.6
BIT 7	Bit 1.7

OUTPUT X'4C' **TYPE 3/TYPE 3HS SCANNER-PDF Array Address**

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	PDF Array Bit 0.5
BIT 6	Bit 0.6
BIT 7	Bit 0.7
BYTE 1, BIT 0	Bit 1.0
BIT 1	Bit 1.1
BIT 2	Bit 1.2
BIT 3	Bit 1.3
BIT 4	Bit 1.4
BIT 5	Bit 1.5
BIT 6	Bit 1.6
BIT 7	Bit 1.7

OUTPUT X'4D' **TYPE 3/TYPE 3HS SCANNER-ICW Cycle Steal PDF**

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Cycle Steal PDF Bit 0.0
BIT 1	Bit 0.1
BIT 2	Bit 0.2
BIT 3	Bit 0.3
BIT 4	Bit 0.4
BIT 5	Bit 0.5
BIT 6	Bit 0.6
BIT 7	Bit 0.7
BYTE 1, BIT 0	Bit 1.0
BIT 1	Bit 1.1
BIT 2	Bit 1.2
BIT 3	Bit 1.3
BIT 4	Bit 1.4
BIT 5	Bit 1.5
BIT 6	Bit 1.6
BIT 7	Bit 1.7

INPUT X'4E' **TYPE 3/TYPE 3HS SCANNER-ICW Bytes 12 and 13 (Note)**

Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	ICW BIT 12.0 Cy Stl PDF Array Ptr Bit 8
BIT 1	BIT 12.1 Bit 4
BIT 2	BIT 12.2 Bit 2
BIT 3	BIT 12.3 Bit 1
BIT 4	BIT 12.4 PDF Array Ptr Bit 8
BIT 5	BIT 12.5 Bit 4
BIT 6	BIT 12.6 Bit 2
BIT 7	BIT 12.7 Bit 1
BYTE 1, BIT 0	BIT 13.0 Sequence 0
BIT 1	BIT 13.1 Sequence 1
BIT 2	BIT 13.2 RTS Turnaround Control
BIT 3	BIT 13.3 Sequence 2
BIT 4	BIT 13.4 (reserved)
BIT 5	BIT 13.5 (reserved)
BIT 6	BIT 13.6 Cycle Steal Message Ctr 0
BIT 7	BIT 13.7 Cycle Steal Message Ctr 1

Note: See Input X'41' in this section of Appendix C for (1) ICW BIT 17.0 Cy Stl PDF Array Ptr Bit 16, and (2) ICW BIT 17.1 PDF Array Ptr Bit 16. These bits are used only with Type 3HS Scanner operations

OUTPUT X'4E' **TYPE 3/TYPE 3HS SCANNER-ICW Bytes 12, 13, and 17**

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 12.0 Cy Stl PDF Array Ptr Bit 8
BIT 1	BIT 12.1 Bit 4
BIT 2	BIT 12.2 Bit 2
BIT 3	BIT 12.3 Bit 1
BIT 4	BIT 12.4 PDF Array Ptr Bit 8
BIT 5	BIT 12.5 Bit 4
BIT 6	BIT 12.6 Bit 2
BIT 7	BIT 12.7 Bit 1
BYTE 1, BIT 0	BIT 13.0 Sequence 0
BIT 1	BIT 13.1 Sequence 1
BIT 2	BIT 13.2 RTS Turnaround Control
BIT 3	BIT 13.3 Sequence 2
BIT 4	BIT 13.4 *
BIT 5	BIT 13.5 *
BIT 6	BIT 13.6 Cycle Steal Message Ctr 0
BIT 7	BIT 13.7 Cycle Steal Message Ctr 1

Note: If a Type 3HS Scanner is installed, these bits represent:
ICW BIT 17.0 Cy Stl PDF Array Ptr Bit 16
ICW BIT 17.1 PDF Array Ptr Bit 16
Otherwise, the bit positians are unused and may be 0 or 1.

INPUT X'4F' **TYPE 3/TYPE 3HS SCANNER-ICW Bytes 14 and 15**

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	ICW BIT 14.0 Receive Line Signal Detect
BIT 1	BIT 14.1 Format Excep/Idle Detect
BIT 2	BIT 14.3 Flush (BSC)
BIT 3	BIT 14.4 Data Check
BIT 4	BIT 14.4 Bad Pad/Flag Off Bdry
BIT 5	BIT 14.5 0=ACK-0/1=ACK-1 Expected
BIT 6	BIT 14.6 DLE Seq. Error (BSC)
BIT 7	BIT 14.7 Length Check
BYTE 1, BIT 0	BIT 15.0 Int. Stat 0 Control Exception
BIT 1	BIT 15.1 1 (reserved)
BIT 2	BIT 15.2 2 (reserved)
BIT 3	BIT 15.3 Final Stat 3 Pgm Req Int on line idle detect or flag
BIT 4	BIT 15.4 4 (reserved)
BIT 5	BIT 15.5 5 Transmit flag or idle
BIT 6	BIT 15.6 6 Transmit pad before turn
BIT 7	BIT 15.7 Ldg graph. Line turn after transmission

OUTPUT X'4F' **TYPE 3/TYPE 3HS SCANNER-ICW Bytes 14 and 15**

Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	ICW BIT 14.0 Reset Receive Line Signal Detect
BIT 1	BIT 14.1 Reset Format Excep/Idle Detect
BIT 2	BIT 14.2 Flush (BSC)
BIT 3	BIT 14.3 Reset Data Check
BIT 4	BIT 14.4 Reset Bad Pad/Flag Off Bdry
BIT 5	BIT 14.5 0=ACK-0/1=ACK-1 Expected
BIT 6	BIT 14.6 Reset DLE Seq. Errar (BSC)
BIT 7	BIT 14.7 Reset Length Che k
BYTE 1, BIT 0	BIT 15.0 Init. Stat 0 Contral Exception
BIT 1	BIT 15.1 1 (reserved)
BIT 2	BIT 15.2 2 (reserved)
BIT 3	BIT 15.3 Final Stat 3 Pgm req int on line idle detect
BIT 4	BIT 15.4 4 (reserved)
BIT 5	BIT 15.5 5 Transmit flag or idle
BIT 6	BIT 15.6 6 Transmit pad before turnaround
BIT 7	BIT 15.7 Ldg Graph. Line turn after transmission

With Extended Addressing, Byte X is set ta zera far input instructians, ignared far autput instructians.
* = Bit positians unused - may be 1 or 0.

INPUT X'50'	TYPE 2/TYPE 3 CA-INCWAR (For Chonnel Write, Write Breok, & Write IPL)	OUTPUT X'50'	TYPE 2/TYPE 3 CA-INCWAR (For Channel Write, Write Break, & Write IPL)
Gen Reg (R)	Reg/Function (E)	Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	INCWAR BIT 0	BYTE 0, BIT 0	INCWAR BIT 0
BIT 1	BIT 1	BIT 1	BIT 1
BIT 2	BIT 2	BIT 2	BIT 2
BIT 3	BIT 3	BIT 3	BIT 3
BIT 4	BIT 4	BIT 4	BIT 4
BIT 5	BIT 5	BIT 5	BIT 5
BIT 6	BIT 6	BIT 6	BIT 6
BIT 7	BIT 7	BIT 7	BIT 7
BYTE 1, BIT 0	BIT B	BYTE 1, BIT 0	BIT B
BIT 1	BIT 9	BIT 1	BIT 9
BIT 2	BIT 10	BIT 2	BIT 10
BIT 3	BIT 11	BIT 3	BIT 11
BIT 4	BIT 12	BIT 4	BIT 12
BIT 5	BIT 13	BIT 5	BIT 13
BIT 6	BIT 14	BIT 6	BIT 14
BIT 7	BIT 15	BIT 7	BIT 15

INPUT X'51'	TYPE 2/TYPE 3 CA-OUTCWAR (For Channel Read)	OUTPUT X'51'	TYPE 2/TYPE 3 CA-OUTCWAR (For Channel Read)
Gen Reg (R)	Reg/Function (E)	Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	OUTCWAR BIT 0	BYTE 0, BIT 0	OUTCWAR BIT 0
BIT 1	BIT 1	BIT 1	BIT 1
BIT 2	BIT 2	BIT 2	BIT 2
BIT 3	BIT 3	BIT 3	BIT 3
BIT 4	BIT 4	BIT 4	BIT 4
BIT 5	BIT 5	BIT 5	BIT 5
BIT 6	BIT 6	BIT 6	BIT 6
BIT 7	BIT 7	BIT 7	BIT 7
BYTE 1, BIT 0	BIT B	BYTE 1, BIT 0	BIT B
BIT 1	BIT 9	BIT 1	BIT 9
BIT 2	BIT 10	BIT 2	BIT 10
BIT 3	BIT 11	BIT 3	BIT 11
BIT 4	BIT 12	BIT 4	BIT 12
BIT 5	BIT 13	BIT 5	BIT 13
BIT 6	BIT 14	BIT 6	BIT 14
BIT 7	BIT 15	BIT 7	BIT 15

INPUT X'52' (See Note)	TYPE 2/TYPE 3 CA-CONTROL WORD BYTE COUNT (CWCNT)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	CWCNT BIT 0
BIT 7	BIT 1
BYTE 1, BIT 0	BIT 2
BIT 1	BIT 3
BIT 2	BIT 4
BIT 3	BIT 5
BIT 4	BIT 6
BIT 5	BIT 7
BIT 6	BIT B
BIT 7	BIT 9

Note: For 3705 Models J, K, and L, this bit configuration is applicable during IPL mode only. Bits 6 and 7 of BYTE 0 are set to 1 each time the field is loaded.

INPUT X'52' (See Note)	TYPE 2/3 CA-CONTROL WORD BYTE COUNT (CWCNT)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0
BYTE 1, BIT 0	CWCNT BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

Note: This bit configuration is applicable only for 3705 Models J, K, and L in non-IPL mode.

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 2/TYPE 3 CHANNEL ADAPTER
X'50'-X'5C'

INPUT X'53'	TYPE 2/TYPE 3 CA-SENSE REGISTER (CASNSR)	
Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	Command Reject	
BIT 1	Intervention Required	
BIT 2	Bus Out Check	
BIT 3	Equipment Check	
BIT 4	Data Check	
BIT 5	0	
BIT 6	Not Initialized	
BIT 7	Abort	
BYTE 1, BIT 0	0	
BIT 1	0	
BIT 2	0	
BIT 3	0	
BIT 4	CSAR Byte X, Bit 4	20-bit EA only
BIT 5	CSAR Byte X, Bit 5	
BIT 6	CSAR Byte X, Bit 6	
BIT 7	CSAR Byte X, Bit 7	

OUTPUT X'53'	TYPE 2/TYPE 3 CA-SENSE REGISTER (CASNR)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Set CMD Reject and Unit Check
BIT 1	Set Interventian Required
BIT 2	*
BIT 3	*
BIT 4	Set Data Check
BIT 5	*
BIT 6	*
BIT 7	Set Abort
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'54'	TYPE 2/TYPE 3 CA-STATUS REGISTER (CASTR)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Attention (ATT)
BIT 1	Status Modifier (SM)
BIT 2	0
BIT 3	Busy
BIT 4	Channel End (CE)
BIT 5	Device End (DE)
BIT 6	Unit Check (UC)
BIT 7	Unit Exception (UE)
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0

OUTPUT X'54'	TYPE 2/TYPE 3 CA-STATUS REGISTER (CASTR)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Set Attention (ATT)
BIT 1	Set Status Modifier (SM)
BIT 2	*
BIT 3	Set Busy
BIT 4	Set Channel End (CE)
BIT 5	Set Device End (DE)
BIT 6	*
BIT 7	Set Unit Exception (UE)
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'55'	TYPE 2/TYPE 3 CA-CONTROL REGISTER (CACR)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Diagnostic Wrap Mode
BIT 1	Zero Count Override
BIT 2	INCWAR Valid
BIT 3	OUTCWAR Valid
BIT 4	Prog Requested L3 Interrupt
BIT 5	Prog Requested Abort/L3 Interrupt
BIT 6	Prog Requested Attention
BIT 7	CA Active
BYTE 1, BIT 0	Command Chaining
BIT 1	Write Breok Command Remember
BIT 2	Channel Stop/Intf Disconnect
BIT 3	Selective/System Reset
BIT 4	0
BIT 5	Channel I/O Read Command Remembrance
BIT 6	Type 2/Type 3 CA 2 Selected
BIT 7	Type 2/Type 3 CA 1 Selected

OUTPUT X'55'	TYPE 2/TYPE 3 CA-CONTROL REGISTER (CACR)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	Set INCWAR Valid
BIT 3	Set OUTCWAR Valid
BIT 4	*
BIT 5	*
BIT 6	Set Prog Requested Attention
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'56'	TYPE 2/TYPE 3 CA-CHECK REGISTER (CACHKR)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Invalid CWAR Address
BIT 1	Invalid CW Format
BIT 2	Cycle Steal Address Check
BIT 3	CWAR/Data Buffer Check
BIT 4	CCU OUTBUS Check
BIT 5	CCU INBUS Check (cycle steal)
BIT 6	Chan Bus Out Check (Sense Bit 2)
BIT 7	0
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	Channel Bus In Check (Intf A)
BIT 5	Channel Bus In Check (Intf B)
BIT 6	0
BIT 7	0

OUTPUT X'56'	TYPE 2/TYPE 3 CA-RESET CONTROL REGISTER
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	Reset INCWAR Valid
BIT 3	Reset OUTCWAR Valid
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	Command-Reject Invalid Commands
BIT 7	Accept Invalid Commands

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused-may be 1 or 0.

OUTPUT X'57' — TYPE 2/TYPE 3 CA-CHNL ADAPTER MODE REGISTER (CAMR)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Set IPL Attention (Note)
	Set Sense Unit Exception Latch (initialized state only)
BIT 1	Set IPL Channel End (Note)
BIT 2	*
BIT 3	Set IPL Device End (Note)
BIT 4	Set IPL Unit Check (Note)
BIT 5	Rest Sense Unit Exception Latch (diagnostic mode only)
BIT 6	1 = Set IPL Unit Exception (Note), 0 = Reset IPL Unit Exception
BIT 7	Set IPL Not-Initialized (Note)
BYTE 1, BIT 0	Set Type 2/Type 3 CA L3 Interrupt
BIT 1	Set Program Abort
BIT 2	Reset Type 2/Type 3 CA L1 Reg
BIT 3	Reset Type 2/Type 3 CA L3 Reg
BIT 4	1 = Select Type 2/Type 3 CA-1, 0 = Type 2/Type 3 CA-2
BIT 5	Reset Selective/System Reset
BIT 6	Reset Channel Stop/Inf Disconnect
BIT 7	1 = Set; 0 = Rst Diagnostic Wrap Mode

Note: This Bit is meaningful only if the 3705 is not initialized or if the channel adapter is in diagnostic wrap mode.

INPUT X'58' — TYPE 2/TYPE 3 CA-CHANNEL BUS OUT DIAG REG (CBODR)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Channel Bus Out BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	Parity Bit
BIT 1	0
BIT 2	Transfer Byte 1
BIT 3	Transfer Byte 2
BIT 4	Channel Intf A Enabled
BIT 5	Channel Intf B Enabled
BIT 6	CSAR Byte X, Bit 6 } 18-bit EA only
BIT 7	CSAR Byte X, Bit 7 }

OUTPUT X'58' — TYPE 2/TYPE 3 CA-CHANNEL BUS OUT DIAGNOSTIC REG (CBODR)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Channel Bus Out BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	Parity Bit
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	Reset CA

INPUT X'59' — TYPE 2/TYPE 3 CA-CYCLE STEAL ADDRESS REGISTER (CSAR)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	CSAR BYTE 0, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	CSAR BYTE 1, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

OUTPUT X'59' — TYPE 3 CA DIAGNOSTIC BUSY

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Set Interface A Busy
BIT 1	Set Interface B Busy
BIT 2	*
BIT 3	*
BIT 4	Reset Interface A Busy
BIT 5	Reset Interface B Busy
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'5A' — TYPE 2/TYPE 3 CA-DATA BUFFER (CADB)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Data Buffer BYTE 0, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	Data Buffer BYTE 1, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

OUTPUT X'5A' — TYPE 2/TYPE 3 CA-DATA BUFFER (CADB)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Data Buffer BYTE 0, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	Data Buffer BYTE 1, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 2/ TYPE 3 CHANNEL ADAPTER
X'50'-X'5C'

INPUT X'5B'	TYPE 2/TYPE 3 CA-TAG DIAGNOSTIC REGISTER (CTDR)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Select Out/Hold Out Inbound
BIT 1	Address Out
BIT 2	Command Out
BIT 3	Service Out
BIT 4	Operational Out
BIT 5	Suppress Out
BIT 6	0
BIT 7	0
BYTE 1, BIT 0	Select Out Outbound
BIT 1	Request In
BIT 2	Operational In
BIT 3	Address In
BIT 4	Status In
BIT 5	Service In
BIT 6	0
BIT 7	Generate Busy

OUTPUT X'5B'	TYPE 2/TYPE 3 CA-TAG DIAGNOSTIC REGISTER
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Select Out/Hold Out Inbound
BIT 1	Address Out
BIT 2	Command Out
BIT 3	Service Out
BIT 4	Operational Out
BIT 5	Suppress Out
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'5C'	TYPE 2/TYPE 3 CA-COMMAND REGISTER (CMDR)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Test I/O X'00'
BIT 1	Write Command X'01'
BIT 2	Read Command X'02'
BIT 3	No-op Command X'03'
BIT 4	Sense Command X'04'
BIT 5	0
BIT 6	Write Break Command X'09'
BIT 7	0
BYTE 1, BIT 0	OUT Control Word
BIT 1	OUT STOP Control Word
BIT 2	IN Control Word
BIT 3	TIC Control Word
BIT 4	Nonstandard Command
BIT 5	Interface A (Type 3 CA Only)
BIT 6	Interface B (Type 3 CA Only)
BIT 7	Write IPL Command X'05'

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 1 CHANNEL ADAPTER
X'60'-X'67'

INPUT X'60'	TYPE 1 CA-INITIAL SELECTION CNTRL
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Initial Selection Interrupt
BIT 1	Interface Discannect
BIT 2	Selective Reset
BIT 3	Channel Bus Out Check
BIT 4	0
BIT 5	Stacked Initial Status
BIT 6	NSC Status Byte Cleared
BIT 7	System Reset
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0

OUTPUT X'60'	TYPE 1 CA-RESET INITIAL SELECTION
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'61'	TYPE 1 CA-INITIAL SELECTION ADDRESS and COMMAND
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	Address Byte BIT 0 (Initial Sel)
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	I/O Cmd Byte BIT 0 (Initial Selectian Cmd.)
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

INPUT X'62'	TYPE 1 CA-DATA/STATUS CNTRL
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	Outbaund Data Transfer Seq
BIT 1	Inbaund Data Transfer Seq
BIT 2	ESC Final Status Transfer Seq
BIT 3	NSC Chan End Status Transfer Seq
BIT 4	NSC Final Status Transfer Seq
BIT 5	Channel Stop/Intf Discannect
BIT 6	Suppress Out Manitar Interrupt
BIT 7	Prag Requested Interrupt
BYTE 1, BIT 0	Channel Bus Out Check
BIT 1	Selective Reset
BIT 2	Suppress Out
BIT 3	Stacked Ending Status
BIT 4	I/O Command Chaining
BIT 5	Transferred Byte Caunt BIT 0
BIT 6	BIT 1
BIT 7	BIT 2

OUTPUT X'62'	TYPE 1 CA-DATA/STATUS CNTRL (Nate)
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	1 = Set; 0 = Rst Outbaund Data Transfer Seq
BIT 1	1 = Set; 0 = Rst Inbaund Data Transfer Seq
BIT 2	1 = Set; 0 = Rst ESC Final Status Transfer Seq
BIT 3	1 = Set; 0 = Rst NSC Chan End Status Transfer Seq
BIT 4	1 = Set; 0 = Rst NSC Final Status Transfer Seq
BIT 5	Reset Initial Selectian
BIT 6	Reset Data/Status Interrupt
BIT 7	*
BYTE 1, BIT 0	Set Manitar far Circle B
BIT 1	*
BIT 2	Set Manitar far 2848 ETX
BIT 3	Set Suppressible Status
BIT 4	Set ESC Test I/O Status Available
BIT 5	*
BIT 6	Request Byte Caunt BIT 1
BIT 7	BIT 2

Nate: This autput resets a program requested interrupt and Suppress out manitar

INPUT X'63'	TYPE 1 CA-ADDR. & ESC STATUS BYTES
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	Addr. Byte BIT 0 (Data/Status Transfer)
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	ESC Status Byte BIT 0 (Attn)
BIT 1	BIT 1 (SM)
BIT 2	BIT 2 (CUE)
BIT 3	BIT 3 (Busy)
BIT 4	BIT 4 (CE)
BIT 5	BIT 5 (DE)
BIT 6	BIT 6 (UC)
BIT 7	BIT 7 (UE)

OUTPUT X'63'	TYPE 1 CA-ADDR. & ESC STATUS BYTES
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Addr. Byte BIT 0 (Data/Status Transfer)
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	ESC Status Byte BIT 0 (Attn)
BIT 1	BIT 1 (SM)
BIT 2	BIT 2 (CUE)
BIT 3	BIT 3 (Busy)
BIT 4	BIT 4 (CE)
BIT 5	BIT 5 (DE)
BIT 6	BIT 6 (UC)
BIT 7	BIT 7 (UE)

With Extended Addressing, Byte X is set ta zera for input instructians, ignared far autput instructions.
* = Bit pasitions unused - may be 1 or 0.

TYPE 1 CHANNEL ADAPTER
X'60'-X'67'

INPUT X'64'	TYPE 1 CA-DATA BUFFER BYTES 1,2	OUTPUT X'64'	TYPE 1 CA-DATA BUFFER BYTES 1,2
Gen Reg (R)	Reg/Function (E)	Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Data Buffer Byte 1, BIT 0	BYTE 0, BIT 0	Data Buffer Byte 1, BIT 0
BIT 1	BIT 1	BIT 1	BIT 1
BIT 2	BIT 2	BIT 2	BIT 2
BIT 3	BIT 3	BIT 3	BIT 3
BIT 4	BIT 4	BIT 4	BIT 4
BIT 5	BIT 5	BIT 5	BIT 5
BIT 6	BIT 6	BIT 6	BIT 6
BIT 7	BIT 7	BIT 7	BIT 7
BYTE 1, BIT 0	Data Buffer Byte 2, BIT 0	BYTE 1, BIT 0	Data Buffer Byte 2, BIT 0
BIT 1	BIT 1	BIT 1	BIT 1
BIT 2	BIT 2	BIT 2	BIT 2
BIT 3	BIT 3	BIT 3	BIT 3
BIT 4	BIT 4	BIT 4	BIT 4
BIT 5	BIT 5	BIT 5	BIT 5
BIT 6	BIT 6	BIT 6	BIT 6
BIT 7	BIT 7	BIT 7	BIT 7

INPUT X'65'	TYPE 1 CA-DATA BUFFER BYTES 3,4	OUTPUT X'65'	TYPE 1 CA-DATA BUFFER BYTES 3,4
Gen Reg (R)	Reg/Function (E)	Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Data Buffer Byte 3, BIT 0	BYTE 0, BIT 0	Data Buffer Byte 3, BIT 0
BIT 1	BIT 1	BIT 1	BIT 1
BIT 2	BIT 2	BIT 2	BIT 2
BIT 3	BIT 3	BIT 3	BIT 3
BIT 4	BIT 4	BIT 4	BIT 4
BIT 5	BIT 5	BIT 5	BIT 5
BIT 6	BIT 6	BIT 6	BIT 6
BIT 7	BIT 7	BIT 7	BIT 7
BYTE 1, BIT 0	Data Buffer Byte 4, BIT 0	BYTE 1, BIT 0	Data Buffer Byte 4, BIT 0
BIT 1	BIT 1	BIT 1	BIT 1
BIT 2	BIT 2	BIT 2	BIT 2
BIT 3	BIT 3	BIT 3	BIT 3
BIT 4	BIT 4	BIT 4	BIT 4
BIT 5	BIT 5	BIT 5	BIT 5
BIT 6	BIT 6	BIT 6	BIT 6
BIT 7	BIT 7	BIT 7	BIT 7

INPUT X'66'	TYPE 1 CA-NSC STATUS BYTE	OUTPUT X'66'	TYPE 1 CA-NSC STATUS BYTE
Gen Reg (R)	Reg/Function (E)	Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	NSC Status Byte BIT 0 (Attn)	BYTE 0, BIT 0	*
BIT 1	NSC Status Byte BIT 1 (SM)	BIT 1	*
BIT 2	0	BIT 2	*
BIT 3	0	BIT 3	*
BIT 4	NSC Status Byte BIT 4 (CE)	BIT 4	*
BIT 5	NSC Status Byte BIT 5 (DE)	BIT 5	*
BIT 6	NSC Status Byte BIT 6 (UC)	BIT 6	*
BIT 7	NSC Status Byte BIT 7 (UE)	BIT 7	*
BYTE 1, BIT 0	0	BYTE 1, BIT 0	Set NSC Status Byte BIT 0 (Attn)
BIT 1	0	BIT 1	Set NSC Status Byte BIT 1 (SM)
BIT 2	0	BIT 2	*
BIT 3	0	BIT 3	*
BIT 4	0	BIT 4	Set NSC Status Byte BIT 4 (CE)
BIT 5	0	BIT 5	Set NSC Status Byte BIT 5 (DE)
BIT 6	0	BIT 6	Set NSC Status Byte BIT 6 (UC)
BIT 7	0	BIT 7	Set NSC Status Byte BIT 7 (UE)

INPUT X'67'	TYPE 1 CA-CONTROLS	OUTPUT X'67'	TYPE 1 CA-CONTROLS
Gen Reg (R)	Reg/Function (E)	Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	NSC Address Byte BIT 0 (Hdw)	BYTE 0, BIT 0	*
BIT 1	BIT 1	BIT 1	*
BIT 2	BIT 2	BIT 2	*
BIT 3	BIT 3	BIT 3	*
BIT 4	BIT 4	BIT 4	CA Diagnostic Reset
BIT 5	BIT 5	BIT 5	*
BIT 6	BIT 6	BIT 6	*
BIT 7	BIT 7	BIT 7	*
BYTE 1, BIT 0	Channel Bus In Check	BYTE 1, BIT 0	Set Suppress Out Manitor Interrupt
BIT 1	In/Out Instruction Accept Check	BIT 1	Set Prag Requested Interrupt
BIT 2	CCU OUTBUS Check	BIT 2	Reset Type 1 CA LI Checks
BIT 3	Local Store Check	BIT 3	Reset System Reset/NSC Address Active/NSC Status Register
BIT 4	Channel Interface Enabled	BIT 4	Set Allow Channel Interface Enable
BIT 5	NSC Address Active	BIT 5	Set ESC Operational
BIT 6	0	BIT 6	Set ESC Command Free
BIT 7	0	BIT 7	Set Allow Channel Interface Disable

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 4 CHANNEL ADAPTER
X'60'-X'6F'

INPUT X'60' — TYPE 4 CA-INITIAL SELECTION CNTRL

Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	Initial Selection Interrupt
BIT 1	Interface Discannect
BIT 2	Selective Reset
BIT 3	Channel Bus Out Check
BIT 4	0
BIT 5	Stacked Initiol Stotus
BIT 6	NSC Status Byte Cleared
BIT 7	System Reset
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0

OUTPUT X'60' — TYPE 4 CA-RESET INITIAL SELECTION

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'61' — TYPE 4 CA-INITIAL SELECTION ADDRESS and COMMAND

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Address Byte BIT 0 (Initiol Selection Addr)
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	I/O Cmd Byte BIT 0 (Initial Selection Cmd)
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

INPUT X'62' — TYPE 4 CA-DATA/STATUS CONTROL

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Outbound Data Transfer Seq
BIT 1	Inbound Dato Transfer Seq
BIT 2	ESC Final Status Transfer Seq
BIT 3	NSC Chan End Status Tronsfer Seq
BIT 4	NSC Final Status Transfer Seq
BIT 5	Channel Stap/Intf Disconnect
BIT 6	Suppress Out Monitar Interrupt
BIT 7	Prog Requested Interrupt
BYTE 1, BIT 0	Chonnel Bus Out Check
BIT 1	Selective Reset
BIT 2	Suppress Out
BIT 3	Stacked Ending Status
BIT 4	I/O Command Chaining
BIT 5	Tronsferred Byte Count BIT 0 (Non-EB Mode)
BIT 6	BIT 1
BIT 7	BIT 2

OUTPUT X'62' — TYPE 4 CA-DATA/STATUS CONTROL (Note 1)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	1 = Set; 0 = Rst Outbound Data Transfer Seq
BIT 1	1 = Set; 0 = Rst Inbound Dato Transfer Seq
BIT 2	1 = Set; 0 = Rst ESC Final Status Transfer Seq
BIT 3	1 = Set; 0 = Rst NSC Chon End Stotus Transfer Seq
BIT 4	1 = Set; 0 = Rst NSC Final Status Transfer Seq
BIT 5	Reset Initiol Selection Interrupt
BIT 6	Reset Data/Status Interrupt
BIT 7	Reset EB Made
BYTE 1, BIT 0	Set Monitor for Circle B
BIT 1	*
BIT 2	Set Monitar for 2B48 ETX
BIT 3	Set Suppressible Status
BIT 4	Set ESC Test I/O Status Available
BIT 5	Set Priority Outbound Data Tronsfer Seq.
BIT 6	Request Byte Count BIT 1 } Non-EB or Non-CS Mode
BIT 7	BIT 2 } (Note 2)

Notes:
1. This Output resets a program requested interrupt and Supress out monitor interrupt.
2. In EB or CS mode, bits 6 and 7 represent SYN count.

INPUT X'63' — TYPE 4 CA-ADDRESS & ESC STATUS BYTES

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Addr. Byte BIT 0 (Doto/Stotus Tronsfer)
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	ESC Stotus Byte BIT 0 (Attn)
BIT 1	BIT 1 (SM)
BIT 2	BIT 2 (CUE)
BIT 3	BIT 3 (Busy)
BIT 4	BIT 4 (CE)
BIT 5	BIT 5 (DE)
BIT 6	BIT 6 (UC)
BIT 7	BIT 7 (UE)

OUTPUT X'63' — TYPE 4 CA-ADDRESS & ESC STATUS BYTES

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Addr. Byte BIT 0 (Data/Status Transfer)
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	ESC Status Byte BIT 0 (Attn)
BIT 1	BIT 1 (SM)
BIT 2	BIT 2 (CUE)
BIT 3	BIT 3 (Busy)
BIT 4	BIT 4 (CE)
BIT 5	BIT 5 (DE)
BIT 6	BIT 6 (UC)
BIT 7	BIT 7 (UE)

With Extended Addressing, Byte X is set to zera fro input instructions, ignored for output instructions.
* = Bit Positians unused - may be 1 or 0.

TYPE 4 CHANNEL ADAPTER
X'60'-X'6F'

INPUT X'64'	TYPE 4 CA-DATA BUFFER BYTES 1 and 2 (Non-EB Mode)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Data Buffer Byte 1, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	Data Buffer Byte 2, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

OUTPUT X'64'	TYPE 4 CA-DATA BUFFER BYTES 1 and 2 (Non-EB Mode)
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	Data Buffer Byte 1, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	Data Buffer Byte 2, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

INPUT X'65'	TYPE 4 CA-DATA BUFFER BYTES 3 and 4 (Non-EB Mode)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Data Buffer Byte 3, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	Dato Buffer Byte 4, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

OUTPUT X'65'	TYPE 4 CA-DATA BUFFER BYTES 3 and 4 (Non-EB Mode)
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	Data Buffer Byte 3, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	Dato Buffer Byte 4, BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

INPUT X'66'	TYPE 4 CA-NSC STATUS BYTE
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	NSC Status Byte BIT 0 (Attn)
BIT 1	NSC Status Byte BIT 1 (SM)
BIT 2	0
BIT 3	0
BIT 4	NSC Status Byte BIT 4 (CE)
BIT 5	NSC Stotus Byte BIT 5 (DE)
BIT 6	NSC Status Byte BIT 6 (UC)
BIT 7	NSC Stotus Byte BIT 7 (UE)
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0

OUTPUT X'66'	TYPE 4 CA-NSC STATUS BYTE
Gen Reg (R)	Reg/Functian (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	Set NSC Long Busy
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	Set NSC Status Byte BIT 0 (Attn)
BIT 1	Set NSC Status Byte BIT 1 (SM)
BIT 2	*
BIT 3	*
BIT 4	Set NSC Status Byte BIT 4 (CE)
BIT 5	Set NSC Status Byte BIT 5 (DE)
BIT 6	Set NSC Status Byte BIT 6 (UC)
BIT 7	Set NSC Status Byte BIT 7 (UE)

INPUT X'67'	TYPE 4 CA-CONTROLS
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	NSC Address Byte BIT 0 (Hdw)
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	Channel Bus In Check
BIT 1	In/Out Instruction Accept Check
BIT 2	CCU OUTBUS Check
BIT 3	Local Store Check
BIT 4	Channel Interface Enabled
BIT 5	NSC Address Active
BIT 6	Type 4 CA Selected (Note)
BIT 7	Type 4 CA Selected (Note)
Note:	00=CA-1, 01=CA-2, 10=CA-3, 11=CA-4

OUTPUT X'67'	TYPE 4 CA-CONTROLS (Note 1)
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Diag Force Initial Select Interrupt
BIT 1	Diag Force Byte Transfer in Cycle Steal Mode
BIT 2	*
BIT 3	Execute Output X'67' on Type 4 CA indicated by bits 0.6-0.7 (Note 2)
BIT 4	CA Diagnostic Reset
BIT 5	Select Type 4 CA indicated by bits 0.6-0.7
BIT 6	Type 4 CA Selected (Note 3)
BIT 7	Type 4 CA Selected (Note 3)
BYTE 1, BIT 0	Set Suppress Out Monitor Interrupt
BIT 1	Set Prog Requested Interrupt
BIT 2	Reset Type 4 CA L1 Checks
BIT 3	Reset System Reset/NSC Address Active
BIT 4	Set Allow Channel Interface Enable
BIT 5	Set ESC Operational
BIT 6	Set ESC Command Free
BIT 7	Set Allow Channel Interface Disable
Note 1:	Executing this Output instruction with all bits 0 primes the Type 4 CA priority selection circuit.
Note 2:	Type 4 CA selection is not changed.
Note 3:	00=CA-1, 01=CA-2, 10=CA-3, 11=CA-4

With Extended Addressing, Byte X is set to zero for input instruction, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

TYPE 4 CHANNEL ADAPTER
X'60'-X'6F'

INPUT X'6C' — TYPE 4 CA-Extended Buffer/Cycle Steal Mode Ctl Reg

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Extended Buffer Mode
BIT 1	Cycle Steal Mode
BIT 2	0
BIT 3	0
BIT 4	SYN Monitor Control Latch
BIT 5	DLE Remember Latch
BIT 6	ASCII Monitor Control Latch
BIT 7	EBCDIC Monitor Control Latch
BYTE 1, BIT 0	Transferred Byte Count Bit 0
BIT 1	(EB/Cycle Steel Mode) Bit 1
BIT 2	Bit 2
BIT 3	Bit 3
BIT 4	Bit 4
BIT 5	Bit 5
BIT 6	Bit 6
BIT 7	Bit 7

OUTPUT X'6C' — TYPE 4 CA-Extended Buffer/Cycle Steal Mode Ctl Reg

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	1=Set, 0=Reset EB Mode
BIT 1	1=Set, 0=Reset Cycle Steal Mode
BIT 2	0
BIT 3	0
BIT 4	1=Set, 0=Reset SYN Monitor Control Latch
BIT 5	1=Set, 0=Reset DLE Remember Latch
BIT 6	1=Set, 0=Reset ASCII Monitor Control Latch
BIT 7	1=Set, 0=Reset EBCDIC Monitor Control Latch
BYTE 1, BIT 0	Reg Byte Count Bit 0
BIT 1	(EB/Cycle Steel Mode) Bit 1
BIT 2	Bit 2
BIT 3	Bit 3
BIT 4	Bit 4
BIT 5	Bit 5
BIT 6	Bit 6
BIT 7	Bit 7

INPUT X'6D' — TYPE 4 CA-Extended Buffer/Cycle Steal Mode Date Buffer

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Data Buffer Even Byte Bit 0
BIT 1	Bit 1
BIT 2	Bit 2
BIT 3	Bit 3
BIT 4	Bit 4
BIT 5	Bit 5
BIT 6	Bit 6
BIT 7	Bit 7
BYTE 1, BIT 0	Data Buffer Odd Byte Bit 0
BIT 1	Bit 1
BIT 2	Bit 2
BIT 3	Bit 3
BIT 4	Bit 4
BIT 5	Bit 5
BIT 6	Bit 6
BIT 7	Bit 7

OUTPUT X'6D' — TYPE 4 CA-Extended Buffer/Cycle Steal Mode Data Buffer

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Data Buffer Even Byte Bit 0
BIT 1	Bit 1
BIT 2	Bit 2
BIT 3	Bit 3
BIT 4	Bit 4
BIT 5	Bit 5
BIT 6	Bit 6
BIT 7	Bit 7
BYTE 1, BIT 0	Data Buffer Odd Byte Bit 0
BIT 1	Bit 1
BIT 2	Bit 2
BIT 3	Bit 3
BIT 4	Bit 4
BIT 5	Bit 5
BIT 6	Bit 6
BIT 7	Bit 7

INPUT X'6E' — TYPE 4 CA-Cycle Steal Error Register and CSAR Byte X

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	Cycle Staal Outbus Error	
BIT 1	Cycle Steal Inbus Error	
BIT 2	Cycle Steal Address Bus Error	
BIT 3	Cycle Steal Address Exception Error	
BIT 4	0	
BIT 5	0	
BIT B	0	
BIT 7	0	
BYTE 1, BIT 0	0	
BIT 1	0	
BIT 2	0	
BIT 3	0	
BIT 4	CSAR Byte X bit 4	with 20-bit EA only
BIT 5	CSAR Byte X bit 5	
BIT B	CSAR Byte X bit 6	with 1B or 20-bit EA
BIT 7	CSAR Byte X bit 7	

OUTPUT X'6E' — TYPE 4 CA-CSAR Byte X

Gen Reg (R)	Reg/Function (E)	
BYTE 0, BIT 0	*	
BIT 1	*	
BIT 2	*	
BIT 3	*	
BIT 4	*	
BIT 5	*	
BIT 6	*	
BIT 7	*	
BYTE 1, BIT 0	*	
BIT 1	*	
BIT 2	*	
BIT 3	*	
BIT 4	CSAR Byte X bit 4	with 20-bit EA only
BIT 5	CSAR Byte X bit 5	
BIT 6	CSAR Byte X bit 6	with 1B or 20-bit EA
BIT 7	CSAR Byte X bit 7	

INPUT X'6F' — TYPE 4 CA-Cycla Steal Mode CSAR Bytes 0 and 1

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	CSAR Byte 0, Bit 0
BIT 1	Bit 1
BIT 2	Bit 2
BIT 3	Bit 3
BIT 4	Bit 4
BIT 5	Bit 5
BIT 6	Bit 6
BIT 7	Bit 7
BYTE 1, BIT 0	CSAR Byte 1, Bit 0
BIT 1	Bit 1
BIT 2	Bit 2
BIT 3	Bit 3
BIT 4	Bit 4
BIT 5	Bit 5
BIT 6	Bit 6
BIT 7	Bit 7

OUTPUT X'6F' (See Note) — TYPE 4 CA-Cycle Steal Mode CSAR Bytes 0 and 1

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	CSAR Byte 0, Bit 0
BIT 1	Bit 1
BIT 2	Bit 2
BIT 3	Bit 3
BIT 4	Bit 4
BIT 5	Bit 5
BIT 6	Bit B
BIT 7	Bit 7
BYTE 1, BIT 0	CSAR Byte 1, Bit 0
BIT 1	Bit 1
BIT 2	Bit 2
BIT 3	Bit 3
BIT 4	Bit 4
BIT 5	Bit 5
BIT 6	Bit B
BIT 7	Bit 7

Note: Executing this instruction causes reset of CSAR Byte X.

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
*Bit position unused — may be 1 or 0.

REMOTE PROGRAM LOADER
X'68'-X'6B'

INPUT X'68' REMOTE PROGRAM LOADER-LEVEL 1 STATUS

Gen Reg (R)	Reg/Function (E)
BYTE 0 BIT 0	*
BIT 1	Outbus Parity Error
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1 BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	Write Command Issued When Write Not Enabled
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

OUTPUT X'68' REMOTE PROGRAM LOADER-CONTROL

Gen Reg (R)	Reg/Function (E)
BYTE 0 BIT 0	Set Low Current For Write
BIT 1	*
BIT 2	Reset Low Current For Write
BIT 3	Reset Head Access Counter to Access 0
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1 BIT 0	Reset Interrupt On Index Latch
BIT 1	Move Head
BIT 2	0 = Reverse, 1 = Forword
BIT 3	Set Diagnostic Status Latches
BIT 4	Set Head Engage Latch
BIT 5	Disk Controller Reset
BIT 6	Reset L1, L3 Interrupt and Disk Controller Latches
BIT 7	Set L3 Interrupt On Index

INPUT X'69' REMOTE PROGRAM LOADER-LEVEL 3 STATUS

Gen Reg (R)	Reg/Function (E)
BYTE 0 BIT 0	Index and Interrupt on Index
BIT 1	In Sync on Read Operation (diagnostic)
BIT 2	Access 0 Active
BIT 3	Access 1 Active
BIT 4	Access 2 Active
BIT 5	Access 3 Active
BIT 6	Head Engage Latch is set
BIT 7	Data Service Request Input/Output Operation
BYTE 1 BIT 0	Head Automatically Disengaged or Motor Current Dropped
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	I/O Overrun Condition
BIT 5	*
BIT 6	*
BIT 7	*

OUTPUT X'69' REMOTE PROGRAM LOADER-READ/WRITE

Gen Reg (R)	Reg/Function (E)
BYTE 0 BIT 0	*
BIT 1	Input/Output Write
BIT 2	Input/Output Read
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1 BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'6A' REMOTE PROGRAM LOADER-PARALLEL DATA REGISTER

Gen Reg (R)	Reg/Function (E)
BYTE 0 BIT 0	PDR BYTE 0 BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1 BIT 0	PDR BYTE 1 BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

OUTPUT X'6A' REMOTE PROGRAM LOADER-PARALLEL DATA REGISTER

Gen Reg (R)	Reg/Function (E)
BYTE 0 BIT 0	PDR BYTE 0 BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1 BIT 0	PDR BYTE 1 BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7

INPUT X'6B' REMOTE PROGRAM LOADER-CONTROL PROGRAM LOAD REGISTER

Gen Reg (R)	Reg/Function (E)
BYTE 0 BIT 0	Preserve Storage Contents for Dump
BIT 1	Control Program Initiated IPL
BIT 2	Reserved
BIT 3	Control Program Initiated IPL Via Host Command
BIT 4	Control Program Initiated IPL from Remota Program Loader (Bit=1) or from Channel (Bit=0)
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1 BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

OUTPUT X'6B' REMOTE PROGRAM LOADER-CONTROL PROGRAM LOAD REGISTER

Gen Reg (R)	Reg/Function (E)
BYTE 0 BIT 0	Preserve Storage for Dump
BIT 1	Control Program Initiated IPL
BIT 2	Reserved
BIT 3	Control Program Initiated IPL Via Host Command
BIT 4	IPL source: 1=local-remote link, 0=channal
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1 BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

* = Bit positions unused - may be 1 or 0.

CCU
X'70'-X'7F'

INPUT X'70' — STORAGE SIZE INSTALLED

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	144, 176, 208, 240
BIT 1	64, 80, 112, 208, 240
BIT 2	32, 48, 112, 176, 240, 512
BIT 3	16, 48, 80, 112, 144, 176, 208, 240, 256, 320, 384, 448
BIT 4	128, 160, 192, 224, 384, 448
BIT 5	64, 96, 192, 320, 448
BIT 6	32, 96, 160, 224
BIT 7	0
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	20-bit Extended Addressing installed

OUTPUT X'70' — HARDSTOP

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'71' — PANEL ADDR/DATA ENTRY DIGITS

Gen Reg (R)	Reg/Function (E)	
BYTE X, BIT 4	DIGIT A, BIT 0	with 20-bit EA only
BIT 5	BIT 1	
BIT 6	BIT 2	with 18 or 20-bit EA
BIT 7	BIT 3	
BYTE 0, BIT 0	DIGIT B, BIT 0	
BIT 1	BIT 1	
BIT 2	BIT 2	
BIT 3	BIT 3	
BIT 4	DIGIT C, BIT 0	
BIT 5	BIT 1	
BIT 6	BIT 2	
BIT 7	BIT 3	
BYTE 1, BIT 0	DIGIT D, BIT 0	
BIT 1	BIT 1	
BIT 2	BIT 2	
BIT 3	BIT 3	
BIT 4	DIGIT E, BIT 0	
BIT 5	BIT 1	
BIT 6	BIT 2	
BIT 7	BIT 3	

EA = Extended Addressing

OUTPUT X'71' — DISPLAY REGISTER 1 (DR 1) (Note)

Gen Reg (R)	Reg/Function (E)	
BYTE X, BIT 4	DR1 BYTE X, BIT 4	with 20-bit EA only
BIT 5	BIT 5	
BIT 6	BIT 6	with 18 or 20-bit EA
BIT 7	BIT 7	
BYTE 0, BIT 0	DR1 BYTE 0, BIT 0	
BIT 1	BIT 1	
BIT 2	BIT 2	
BIT 3	BIT 3	
BIT 4	BIT 4	
BIT 5	BIT 5	
BIT 6	BIT 6	
BIT 7	BIT 7	
BYTE 1, BIT 0	DR1 BYTE 1, BIT 0	
BIT 1	BIT 1	
BIT 2	BIT 2	
BIT 3	BIT 3	
BIT 4	BIT 4	
BIT 5	BIT 5	
BIT 6	BIT 6	
BIT 7	BIT 7	

Note: Sets Program Display Light — EA = Extended Addressing

INPUT X'72' — PANEL DISPLAY/FUNCTION SELECT SWITCH CONTROLS

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	Storage Address
BIT 4	Register Address
BIT 5	0
BIT 6	0
BIT 7	0
BYTE 1, BIT 0	0
BIT 1	Function Select 1
BIT 2	Function Select 2
BIT 3	Function Select 3
BIT 4	Function Select 4
BIT 5	Function Select 5
BIT 6	Function Select 6
BIT 7	0

DUTPUT X'72' — DISPLAY REGISTER 2 (DR 2) (Note)

Gen Reg (R)	Reg/Function (E)	
BYTE X, BIT 4	DR2 BYTE X, BIT 4	with 20-bit EA only
BIT 5	BIT 5	
BIT 6	BIT 6	with 18 or 20-bit EA
BIT 7	BIT 7	
BYTE 0, BIT 0	DR2 BYTE 0, BIT 0	
BIT 1	BIT 1	
BIT 2	BIT 2	
BIT 3	BIT 3	
BIT 4	BIT 4	
BIT 5	BIT 5	
BIT 6	BIT 6	
BIT 7	BIT 7	
BYTE 1, BIT 0	DR2 BYTE 1, BIT 0	
BIT 1	BIT 1	
BIT 2	BIT 2	
BIT 3	BIT 3	
BIT 4	BIT 4	
BIT 5	BIT 5	
BIT 6	BIT 6	
BIT 7	BIT 7	

Note: Sets Program Display Light — EA = Extended Addressing

INPUT X'73' — INSERT KEY

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	Key Bit 0
BIT 6	Key Bit 1
BIT 7	Key Bit 2

OUTPUT X'73' (Part 1) — SET KEY (For 20-bit EA see DUTPUT X'73' Part 2)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	SKA Bit 0
BIT 1	SKA Bit 1
BIT 2	SKA Bit 2
BIT 3	SKA Bit 3
BIT 4	SKA Bit 4 or PKA Bit 0
BIT 5	SKA Bit 5 or PKA Bit 1
BIT 6	SKA Bit 6 or PKA Bit 2
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	Key Address Select 1 = SKA; 0 = PKA
BIT 4	Set Key
BIT 5	Key Bit 0
BIT 6	Key Bit 1
BIT 7	Key Bit 2

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

OUTPUT X'73' SET KEY (For 3705s with 20-bit EA only)
(Part 2)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Reserved
BIT 1	Reserved
BIT 2	Reserved
BIT 3	SKA Bit 3
BIT 4	SKA Bit 4 or PKA Bit 0
BIT 5	SKA Bit 5 or PKA Bit 1
BIT 6	SKA Bit 6 or PKA Bit 2
BIT 7	SKA Bit 7
BYTE 1, BIT 0	SKA Bit B
BIT 1	SKA Bit 9
BIT 2	SKA Bit 10
BIT 3	Key Address Select 1 = SKA; 0 = PKA
BIT 4	Set Key
BIT 5	Key Bit 0
BIT 6	Key Bit 1
BIT 7	Key Bit 2

EA = Extended Addressing

INPUT X'74' LAGGING ADDRESS REGISTER (LAR)

Gen Reg (Reg)	Reg/Function (E)	
BYTE X, BIT 4	LAR BYTE X, BIT 4	with 20-bit EA only
BIT 5	BIT 5	
BIT 6	BIT 6	with 1B or 20-bit EA
BIT 7	BIT 7	
BYTE 0, BIT 0	LAR BYTE 0, BIT 0	
BIT 1	BIT 1	
BIT 2	BIT 2	
BIT 3	BIT 3	
BIT 4	BIT 4	
BIT 5	BIT 5	
BIT 6	BIT 6	
BIT 7	BIT 7	
BYTE 1, BIT 0	LAR BYTE 1, BIT 0	
BIT 1	BIT 1	
BIT 2	BIT 2	
BIT 3	BIT 3	
BIT 4	BIT 4	
BIT 5	BIT 5	
BIT 6	BIT 6	
BIT 7	BIT 7	

EA = Extended Addressing

INPUT X'76' ADAPTER LEVEL 1 INTERRUPT REQUESTS

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Type 4 CA L1
BIT 1	Type 1/2/3 Scan-1 L1
BIT 2	Type 2/3 Scan-2 L1
BIT 3	Type 2/3 Scan-3 L1
BIT 4	Type 2/3 Scan-4 L1
BIT 5	Type 2/3 CA-1, Type 1 CA, or Selected Type 4 CA L1
BIT 6	Type 2/3 CA-2 L1
BIT 7	Remote Program Loader L1 Request
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions except where noted.
* = Bit positions unused - may be 1 or 0.

CCU
X'70'-X'7F'

INPUT X'77' — ADAPTER LEVEL 2 or 3 INTERRUPT REQUESTS (Note 1)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	Type 1/2/3 Scon L2
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0
BYTE 1, BIT 0	Type 4 CA L3
BIT 1	Remote Progrom Loader L3 Request
BIT 2	Type 2/Type 3 CA-2 L3
BIT 3	Type 1 or Selected Type 4 CA Doto/Status L3
BIT 4	Type 1/2/3 CA-1 or Selected Type 4 CA L3
BIT 5, BIT 6	Type 4 CA Selected (Note 2)
BIT 7	0

Note 1: Executing this instruction following an Output X'67' instruction in which all bits=0 automatically selects the Type 4 CA having highest L3 priority.
Note 2: 00=CA-1, 01=CA-2, 10=CA-3, 11=CA-4

OUTPUT X'77' — MISCELLANEOUS CONTROL

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Reset IPL L1 ond not-initiolized bit
BIT 1	Reset CCU Checks
BIT 2	Reset Ponel Interrupt Reg L3
BIT 3	0
BIT 4	0
BIT 5	*
BIT 6	Set Diognostic L2
BIT 7	Reset Diognostic L2 (note)
BYTE 1, BIT 0	*
BIT 1	Reset Intervol Timer L3
BIT 2	Reset PCI L3
BIT 3	*
BIT 4	Reset Address Compare L1
BIT 5	Reset Progrom Checks L1
BIT 6	Reset PCI L4
BIT 7	Reset SVC L4

Note: Ignored if not in Test Mode.

OUTPUT X'78' — FORCE CCU CHECKS (3705) (Ignored if not in Test Mode)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Complement Byte 0,1 -- Bit 0
BIT 1	Complement Byte 0,1 -- Bit 1
BIT 2	Complement Byte 0,1 -- Bit 2
BIT 3	Complement Byte 0,1 -- Bit 3
BIT 4	Complement Byte 0,1 -- Bit 4
BIT 5	Complement Byte 0,1 -- Bit 5
BIT 6	Complement Byte X,0,1 -- Bit 4
BIT 7	Complement Byte X,0 1 -- Bit 5
BYTE 1, BIT 0	Complement Storage Pority
BIT 1	Complement Z Bus Pority
BIT 2	A-Reg Check
BIT 3	INDATA Bus Check
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

OUTPUT X'78' — FORCE CCU CHECKS (3704) (Ignored if not in Test Mode)

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	Instruction Cycle Select
BIT 6	Instruction Cycle Select
BIT 7	Instruction Cycle Select
BYTE 1, BIT 0	Complement Storoge Pority
BIT 1	Complement Z Bus Pority
BIT 2	A-Reg Check
BIT 3	B-Reg Pority Error
BIT 4	SAR Pority Error
BIT 5	Op Reg Parity Error
BIT 6	*
BIT 7	*

INPUT X'79' — UTILITY

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	900 nanosecond cycle time
BIT 6	Prog Level 5 C Condition
BIT 7	Prog Level 5 Z Condition
BYTE 1, BIT 0	Prog Level 2 Interrupted (note)
BIT 1	Prog Level 3 Interrupted (note)
BIT 2	Prog Level 4 Interrupted (note)
BIT 3	Prog Level 5 Interrupted (note)
BIT 4	FET memory
BIT 5	0
BIT 6	0
BIT 7	IPL Escope Control

Note: This bit=0 if not Level 1 or if entered immediotely ofter exiting Level 1.

OUTPUT X'79' — UTILITY

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	Set IPL
BIT 3	Set FET Diognostic Mode
BIT 4	Remote Power Off
BIT 5	Inhibit Prog Level 5 C, Z Replocement
BIT 6	Prog Level 5 C Condition
BIT 7	Prog Level 5 Z Condition
BYTE 1, BIT 0	Reset CCU Check Hord Stop Mode
BIT 1	Reset Load Light
BIT 2	Set Test Mode
BIT 3	Reset Test Mode
BIT 4	Set Bypass CCU Check Stop Mode (note)
BIT 5	Reset Byposs CCU Check Stop Mode (note)
BIT 6	Scope Sync Pulse 1
BIT 7	Scope Sync Pulse 2

NOTE: Ignored if not in Test Mode.

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

INPUT X'7A' CYCLE UTILIZATION COUNTER

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	CUC Flag
BIT 1	– 16384
BIT 2	– 8192
BIT 3	– 4096
BIT 4	– 2048
BIT 5	– 1024
BIT 6	– 512
BIT 7	– 256
BYTE 1, BIT 0	– 128
BIT 1	– 64
BIT 2	– 32
BIT 3	– 16
BIT 4	– 8
BIT 5	– 4
BIT 6	– 2
BIT 7	– 1

OUTPUT X'7A' CYCLE UTILIZATION COUNTER RESET

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'7B' BSC CRC REGISTER

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	BSC CRC BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	BIT 8
BIT 1	BIT 9
BIT 2	BIT 10
BIT 3	BIT 11
BIT 4	BIT 12
BIT 5	BIT 13
BIT 6	BIT 14
BIT 7	BIT 15

INPUT X'7C' SDLC CRC REGISTER

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	SDLC CRC BIT 0
BIT 1	BIT 1
BIT 2	BIT 2
BIT 3	BIT 3
BIT 4	BIT 4
BIT 5	BIT 5
BIT 6	BIT 6
BIT 7	BIT 7
BYTE 1, BIT 0	BIT 8
BIT 1	BIT 9
BIT 2	BIT 10
BIT 3	BIT 11
BIT 4	BIT 12
BIT 5	BIT 13
BIT 6	BIT 14
BIT 7	BIT 15

OUTPUT X'7C' SET PCI L3

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

INPUT X'7D' CCU CHECK REGISTER

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Byte X Check
BIT 1	Byte 0 Check
BIT 2	Byte 1 Check
BIT 3	Program Check in Level 1
BIT 4	SAR Check
BIT 5	SDR Check
BIT 6	OP Reg Check
BIT 7	INDATA Bus Check
BYTE 1, BIT 0	Cycle Counter Check
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0 = No CCU Checks; 1–CCU Check(s)
BIT 6	TYPE 2 Attach Base Clock Check
BIT 7	CCU Clock Check

OUTPUT X'7D' SET PCI L4

Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

INPUT X'7E'	CCU LEVEL 1 INTERRUPT REQUESTS
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	0
BIT 7	0
BYTE 1, BIT 0	Address Compare Interrupt L1
BIT 1	Address Exception (note)
BIT 2	In/Out Check (note)
BIT 3	Protection Check (note)
BIT 4	Invalid Op Check (note)
BIT 5	0
BIT 6	IPL L1
BIT 7	0
Note: Prog Check	

OUTPUT X'7E'	SET MASK BITS
Ger Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	Adapter Requests L1 (note)
BIT 2	Program Level 2
BIT 3	Program Level 3
BIT 4	Program Level 4
BIT 5	Program Level 5
BIT 6	*
BIT 7	*
Note: Ignored if not in Test Mode	

INPUT X'7F'	CCU LEVEL 2, 3, or 4, INTERRUPT REQUESTS
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	Diagnostic L2
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	0
BIT 6	Panel Interrupt Request L3
BIT 7	PCI L4
BYTE 1, BIT 0	0
BIT 1	0
BIT 2	0
BIT 3	0
BIT 4	0
BIT 5	Interval Timer L3
BIT 6	PCI L3
BIT 7	SVC L4

OUTPUT X'7F'	RESET MASK BITS
Gen Reg (R)	Reg/Function (E)
BYTE 0, BIT 0	*
BIT 1	*
BIT 2	*
BIT 3	*
BIT 4	*
BIT 5	*
BIT 6	*
BIT 7	*
BYTE 1, BIT 0	*
BIT 1	Adapter Requests Level 1 (note)
BIT 2	Program Level 2
BIT 3	Program Level 3
BIT 4	Program Level 4
BIT 5	Program Level 5
BIT 6	*
BIT 7	*
Note: Ignored if not in Test Mode	

With Extended Addressing, Byte X is set to zero for input instructions, ignored for output instructions.
* = Bit positions unused - may be 1 or 0.

Glossary

Asterisked (*) definitions are reproduced with permission from the American National Dictionary for Information Processing, copyright 1977 by the Computer and Business Equipment Manufacturers Association, copies of which may be purchased from the American National Standard Institute, 1430 Broadway, New York, N.Y. 10018.

Access method. A data management technique for transferring data between storage and an input/output device.

Addressing. The means whereby the originator or control unit selects the teleprocessing device to which it is going to send a message.

Address substitution. A Type 2 Attachment Base feature that modifies the scan counter output to replace certain pairs of interface addresses with one other address.

Attachment base. A communications controller hardware feature that provides the interface controls to the Central Control Unit for the 3705 adapters.

Bit service. The process of character assembly or disassembly.

Buffer. A temporary storage area for data.

Central Control Unit. The communications controller hardware unit that contains the circuits and data flow paths needed to execute the instruction set and to control storage and the attached adapters.

Channel adapter (CA). A communications controller hardware unit that provides attachment of the controller to a System/360 or System/370 channel.

Channel-attached controller. Equivalent to *local controller.*

Character assembly. The process by which bits are put together to form characters as the bits arrive on a communication line. In the communications controller, character assembly is performed either by the control program or by the communication scanner, depending on the type of scanner installed.

Character disassembly. The process by which characters are broken down into bits for transmission over a communication line. In the communications controller, character disassembly is performed either by the control program or by the communication scanner, depending on the type of scanner installed.

Character service. The process by which a character is moved to a buffer from the storage area where it was assembled.

Clock. A device that generates periodic signals used for synchronization.

Communication line. The means of connecting one location to another for the purpose of transmitting and receiving data. In this publication, the term refers to any communication facility of the communications common carrier, whether it is actually a wire or some other means of communication, such as radio or satellite.

Communication scanner. A controller hardware unit that provides the connection between line interface bases and the central control unit. The communication scanner monitors the communication lines for service requests.

Communication unit. A unit of data communications equipment linked to the controller via a communication line and identified as a cluster, terminal, or component at the time the control program is generated.

Component. An independently addressable part of a station that performs either an input or an output function for the terminal, but not both.

Control character. (See line control character.)

Cycle steal. The process by which a type 2, a type 3, or a type 4 channel adapter acquires machine cycles from the 3705 control program for data transfer.

***Data communication.** The transmission and reception of data.

Data communication network. The stations that are controlled by a single access method (or, in controllers, by a single control program), and the communication lines by which they are linked to the communication control unit.

Data communication subsystem. The part of a data processing system devoted to the transfer of data across communication lines. The subsystem consists of the stations, modems (data sets), communication lines, and the communication control unit.

Device. (See Teleprocessing device.)

Extended Addressing. The addition of two or four high order bits to the basic addressing scheme to permit installation of larger storage capacities.

Hard stop. Immediate termination of controller operation without the execution of orderly closedown procedures.

Hardware check. A failure in a hardware unit that halts operation.

Host processor. The central processing unit to which the communications controller is attached by a channel and that executes the teleprocessing access method that supports the controller.

Interrupt. A break in the normal sequence of instruction execution. It causes an automatic transfer to a preset storage location where appropriate action is taken.

*American National Standard Definition

Interrupt priority. The order in which the control program processes interrupts received sumultaneously from two or more communication lines.

Line. Equivalent to *communication line.*

Line control character. A special character that controls transmission of data over a communication line. For example, line control characters are used to start or end a transmission, to cause transmission-error checking to be performed, and to indicate whether a terminal has data to send or is ready to receive data.

Line group. A group of communication lines by which stations supported by the same line-control discipline are connected to the communications controller.

Line interface base (LIB). A communications controller hardware unit that provides for the attachment of up to 16 communication lines to the controller.

Line scanner. (see Communication scanner.)

Line set. A communications controller hardware unit through which one or two lines are attached to a line interface base.

Multiprocessor. A computer employing two or more processing units under integrated control. A tightly-coupled multiprocessor is a computer employing two or more processing units that are controlled by the same operating system and share all of main storage and most of auxiliary storage.

Program check. An error in a program that suspends execution.

Shoulder-tap interrupt. A multiprocessing technique that enables one central processing unit to communicate with another multiprocessing unit.

Subchannel. The channel facility required for sustaining a single I/O operation.

Symmetrical I/O unit. A unit that is attached to two processors, appears as the same I/O unit to each processor, and can be accessed in the same manner by each processor.

Synchronous Data Link Control (SDLC). A discipline for the management of synchronous, transparent, serial-by-bit information transfer over a communications channel. SDLC includes comprehensive detection and recovery procedures for transmission errors introduced by the communications channel.

Teleprocessing. A form of information handling in which a data processing system utilizes communication facilities.

Teleprocessing device. A unit of teleprocessing equipment connected to the communications controller via a communication line and identified as a cluster, terminal, or component.

Teleprocessing network. The stations that are controlled by a single access method and the communication lines by which they are connected to the transmission control unit.

Terminal. A teleprocessing device capable of transmitting or receiving data (or both) over a communication line.

Transmission code. The character code used for data transmissions across a communication line.

Transmission control unit (TCU). A unit that provides the interface between communication lines and a computer. The TCU interleaves the transfer of data from many lines across a single channel to the computer.

Two-channel switch. A feature that allows the communications controller to be attached to two channels through one channel adapter.

Uniprocessor. A computer employing one processing unit.

Upper scan limit. A Type 2 Communication Scanner feature that allows the control program to limit the maximum number of lines that a particular scanner addresses.

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